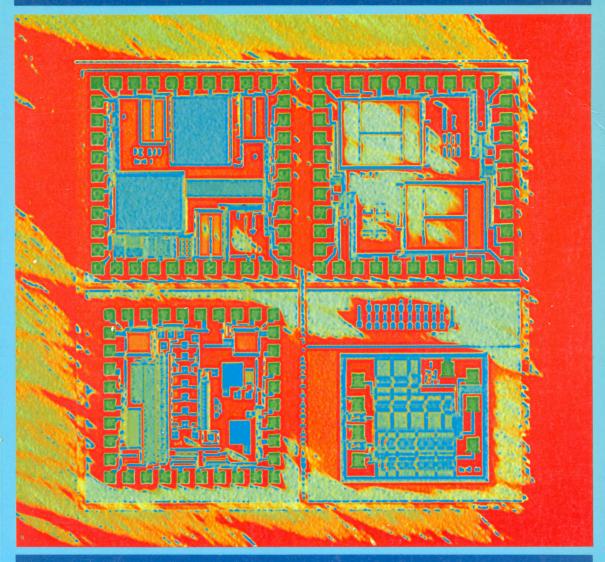


MOTOROLA Semiconductors



CMOS DATA MANUAL VOLUME 2

SPECIAL FUNCTIONS

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Selection Guides

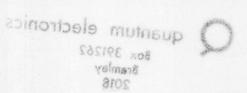
Data Sheets 2

Mechanical Data

Handling Precautions 4

Reliability and Quality Assurance

Publications and Applications



Selection Guides

Data Sheets

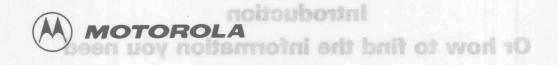
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Reliability and Quality Assurance

Publications and Applications



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Volume 1 contains data on Code-11 Will: 1 AV as the following functions:

- Inverters / Buffers / Level Translators
- SPECIAL FUNCTIONS T STATE OF THE PROPERTY OF T
 - Shift Registers
 - Adders / Comparators
 - Parity Generators / Checkers
 - ALU's / Rate Multipliers
 - Engoders / Decoders
 - Multiplexers / Demultiplexers / Bilateral Switches
 - Multivibrators / Oscillators / Timers

Volume 2 contains data on Special Functions which are defined as the following functions:

- PLL Frequency Synthesizers
 - Display Decoders / Drivers
- A/D, D/A Converters / Logic Functions
 - Operational Amplifiers / Comparators
 - Remote Control Functions
 - Radio / TV Functions
 - Miscellaneous Functions

This information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein. No license is conveyed under patent rights in any form. When this document contains information on a new product, specifications herein are subject to change without notice.

in the Telecommunications Data Manual.

Microprocessors and peripherals are listed in the Selection Guide, but data is to be found in the Microprocessors Data Manuals (8 and 16-Bit).

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First Edition 1983 - B0028
Printed in Switzerland

Introduction Or how to find the information you need

The European CMOS Data Manuals Volumes 1, 2 and 3 contain all the relevant data required to design and use Motorola CMOS Functions. The first two volumes replace the European CMOS Selection Data Book which was published in 1979.

Volume 1 contains data on Standard Logic which is defined as the following functions:

- NAND / NOR / AND / OR / Complex Gates
- Inverters / Buffers / Level Translators
- Schmitt Triggers
- Flip Flops / Latches
- Shift Registers
- Counters
- Adders / Comparators
- Parity Generators / Checkers
- ALU's / Rate Multipliers
- Encoders / Decoders
- Multiplexers / Demultiplexers / Bilateral Switches
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- Radio / TV Functions
- Miscellaneous Functions

Volume 3 contains data on High Speed CMOS. All and make the state of t

Telecommunications functions are listed in the Selection Guide but data is to be found in the Telecommunications Data Manual.

Microprocessors and peripherals are listed in the Selection Guide, but data is to be found in the Microprocessors Data Manuals (8 and 16-Bit).

Memories are also listed in the Selection Guide. This book contains data on the smaller memories. The data for larger memories is to be found in the Memory Data Manual. See the selector guides for details.

The contents of each section of this book are:

1. SELECTION GUIDES

Ordering Information (page 1-2) — defines the numbering system and suffixes and gives details of processing options.

Selection Guide by Part Number (page 1-4) — contains a human alphanumeric listing of all functions with details of suffixes and pins, and where to find detailed technical data. This section can also be used as a cross reference to find equivalents for other suppliers' functions.

Selection Guide by Function (page 1-12) — lists all devices which are capable of performing broadly defined functions, and where to find detailed technical data.

PLL Frequency Synthesizer Selector Tables (page 1-15) — give comparative data for key characteristics of PLL Frequency Synthesizers.

HSCMOS Selector Guide (page 1-16) — gives key family characteristics and ordering information. Lists devices by function and shows equivalent LSTTL and CMOS functions.

 ${\bf Gate\ Arrays}$ (page 1-23) - a brief outline of the MOS Gate Arrays and the design system.

2. DATA SHEETS

Technical data for all special functions. Where parts are still at the design and development stage, then the data consists of either Product Previews or Advance Information.

3. MECHANICAL DATA

Package dimensions for all devices in this book.

4. HANDLING PRECAUTIONS

The static and latch-up problems associated with MOS are now well understood. This section lists the precautions to be taken during shipment, assembly and test to avoid these problems. It is recommended that this section be read thoroughly.

5. RELIABILITY AND QUALITY ASSURANCE

This section describes the key elements of Motorola's reliability and quality assurance activities, and gives the results of the 1982 tests.

6. PUBLICATIONS / APPLICATIONS

Lists the publications available from Motorola Semiconductors.

On the back cover, there is a list of Motorola Sales Offices and Distributors.

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Ordering Information

1

Selection Guides

STANDARD PRODUCTS

```
MC14001BAL
—denotes — Operating Voltage Range
— Operating Temperature Range
— Package Material
—denotes Function
```

SUFFIXES

```
AL 3 to 18 V, -55 to +125°C, Ceramic Package
CL 3 to 18 V, -40 to +85°C, Ceramic Package
CP 3 to 18 V, -40 to +85°C, Plastic Package
Limited Voltage Range, Limited Temperature Range, Ceramic Package
Limited Voltage Range, Limited Temperature Range, Plastic Package
EFL 3 to 18 V, -55 to +125°C, Ceramic Package
FL 3 to 18 V, -40 to +85°C, Ceramic Package
FP 3 to 18 V, -40 to +85°C, Plastic Package
EVL 3 to 6 V, -40 to +85°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Ceramic Package
VL 3 to 6 V, -40 to +85°C, Plastic Package
VP 3 to 6 V, -40 to +85°C, Plastic Package
```

OPTIONS

1. Burn-in

Motorola CMOS integrated circuits are manufactured under strict quality control. Inprocess screens and tight out-going inspection result in a high order of quality and reliability.

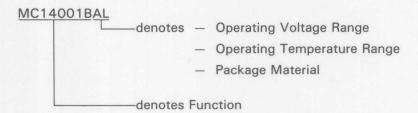
In addition, Burn-In is an option available on all CMOS packaged products. The benefits of this option are:

- reduced infant mortality (typically 0.2% of the product is screened out);
 - reduced board and system rework
 - reduced equipment downtline
 - reduced field failures.

Ordering Information

1

STANDARD PRODUCTS



SUFFIXES

```
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- reduced equipment downtime;
- reduced field failures.

1

Additional processing of these burnt-in circuits is as follows:

Burn-In Device Flow Normal Flow Electrical Electrical Test Test Mark Mark Burn-in Outgoing quality control Test. D.C. sample Parameters electrical at 25°C GAOOMBOOM test Outgoing quality control sample electrical test

Motorola Burn-in is performed under the following conditions:

V_{DD} 15 V
Temperature 125°C ambient
Time 168 hours
Bias Dynamic for Memories and Analog Circuits, Static for all others

Ordering Information:

The Burn-in option is selected by adding the suffix D to the part number, for example:

MC14001BALD qualify bau0

2. Chips and Wafers

Chips and wafers are available for all CMOS types. For further information, consult your Motorola Sales Office or authorized Motorola Distributor.

3. HI-REL

Various options are available, including parts qualified to BS9000, CECC and MIL STD883B Class B type processed. For further information, consult your Motorola Sales Office or authorized Motorola Distributor.

Selection Guide by Part Number | Solition A

Device		Function	Suffix	Pins	Page
MC54HCXXX	High Speed C	MOS Series	J		lottioo
MC68HC04P2 MC68HC04P3 MC68HC05C4 MC68HC09E	8-Bit CMOS I 8-Bit Single C	Chip Microcomputer Microcomputer EPROM Chip Microcomputer ocessor	L,P,Z L,P,Z L,P,Z L,P,Z	28 28 40 40	× × × ×
MC74HCXXX	High Speed C	MOS Series	J,N		
MC6172 MC6173 MC6220	2400 Baud D	PSK Modulator PSK Demodulator Omputer with PLL Frequency	L,P none,psi ni-	24 24	Metorol
MC6860 MC6862	Synthesizer (Low Speed N	NMOS Device)lodemchanged to MC6172	P V _{DD} Q,J	28 24	§ •
MC14000UB		NOR Gate Plus Inverter	AL,CL,CP	14	*
MC14001B		NOR Gate	AL,CL,CP	14	*
MC14001UB		NOR Gate	AL,CL,CP	14	*
MC14002B		NOR Gate	AL,CL,CP	14	*
MC14002UB		NOR Gate	AL,CL,CP	14	*
MC14006B		Shift Register	AL,CL,CP	14	*
MC14007UB		nentary Pair Plus Inverter	AL,CL,CP	14	*
MC14008B	4-Bit Full Add	der	AL,CL,CP	16	Orderino
4009 4010	See MC140	49UB - Pin for Pin Equivalent 50B - Pin for Pin Equivalent	tion is select		
MC14011B	Quad 2-Input	NAND Gate	AL,CL,CP	14	*
MC14011UB	Quad 2-Input	NAND Gate	AL,CL,CP	14	*
MC14012B	Dual 4-Input	NAND Gate	AL,CL,CP	14	*
MC14012UB	Dual 4-Input	NAND Gate	AL,CL,CP	14	*
MC14013B	Dual D Flip-Fl	op	AL,CL,CP	14	*
MC14014B	8-Bit Static S	hift Register	AL,CL,CP	16	100* 0
MC14015B	Dual 4-Bit Sta	atic Shift Register	AL,CL,CP	16	* .2
MC14016B	Quad Analog	Switch/Multiplexer	AL,CL,CP	14	*
MC14017B	Decade Cour	iter/Divider	AL,CL,CP	16	lount and
MC14018B	Presettable D	livide-By-N Counter	AL,CL,CP	16	*
4019B		19B - Normally Pin for Pin			

3. HI-REL

[×] See the 8-Bit Microprocessors Data Manual.
§ See Data Sheet.
★ See the CMOS Data Manual, Volume 1, Standard Logic.
□ See the CMOS Data Manual, Volume 3, High Speed CMOS.
● See the Telecommunications Data Manual.

Device	Suffix	Function		Suffix	Pins	Page
MC14020B	14-Bit Binary Count	ter		AL,CL,CP	1670	M#140
MC14021B	8-Bit Static Shift Re	egister	alva AlOR Gate	AL,CL,CP	16	MG140
MC14022B	Octal Counter/Divid	der		AL,CL,CP	16	MG+140
MC14023B	Triple 3-Input NANI	D Gate	era a Gitta au c	AL,CL,CP		M@140
MC14023UB	Triple 3-Input NANI	D Gate		AL,CL,CP	1480	MG140
MC14024B	7-Stage Ripple Cou				14	* 40
MC14025B	Triple 3-Input NOR	Gate		AL,CL,CP	14	*
MC14025UB	Triple 3-Input NOR	Gate	out NAND Schmitz	AL,CL,CP		MC140
MC14027B	Dual J-K Flip-Flop			AL,CL,CP	16	MC140
MC14028B	BCD-to-Decimal/Bir	nary-to-Oct	al Decoder	AL,CL,CP	16	MC140
MC14029B	Binary/Decade Up/[Down Coun	ter	AL,CL,CP	16	*
4030B 4031B	See MC14070B - I See MC14557B - I		Equivalent		8880	
				8-Bit Addr		
MC14032B	Triple Serial Adder (M@141
MC14034B	8-Bit Universal Bus					M@141
MC14035B	4-Bit Shift Register				16	*
MC14038B	Triple Serial Adder (M@141
MC14040B	12-Bit Binary Count					MG+141
MC14042B	Quad Transparent L			AL,CL,CP	16	*
MC14043B	Quad NOR R-S Lato					MG141
MC14044B	Quad NAND R-S La					MG 141
MC14046B	Phase-Locked Loop					2-2
4047B	See MC14528B - I	Functionally	/ Equivalent	PCM Mono		MC144
MC14049UB	Hex Inverter/Buffer			AL,CL,CP	16	MC144
MC14050B	Hex Buffer			AL,CL,CP	16	MUT 44
MC14051B	8-Channel Analog N			AL,CL,CP	16	MC144
MC14052B	Dual 4-Channel An			PCIVI Mions		IVIC 144
	Demultiplexer			AL,CL,CP	16	MC144
MC14053B	Triple 2-Channel A	nalog Multi	plexer/			
16 0	Demultiplexer	1911	none Pulse Conve	AL,CL,CP	16	MC144 MC144
4055B	See MC14543B - I	Functionally	/ Equivalent	Bit-Rate Fr		MC144
4056B	See MC14543B - I	Normally Pi	n for Pin			
						MC144
4057B	See MC14581B - I	Functionally	/ Equivalent			
MC14060B	14-Bit Binary Count	ter and Osc	illator	AL,CL,CP	14	MQ144
4061	See MCM14537 -	Functionall	y Equivalent			
4063	See MC14585B - I	Functionally	/ Equivalent			MC144
MC14066B	Quad Analog Switc	h/Multiplex	er	AL,CL,CP	14	MC144
MC14067B	16-Channel Analog			AL,CL,CP	24	MC144
MC14068B	8-Input NAND Gate		Construction Const	AL,CL,CP	14	MC144
MC14069UB	Hex Inverter			AL,CL,CP	14	MC144
MC14070B	Quad Exclusive OR	Gate		AL,CL,CP	14	MC144
MC14071B	Quad 2-Input OR Ga	ate	man grand 1 opsic	AL,CL,CP	14	MC144
MC14072B	Dual 4-Input OR Ga	te	CONTROL VIOLEN	AL,CL,CP	14	*
MC14073B	Triple 3-Input AND	Gate		AL,CL,CP	14	*
MC14075B	Triple 3-Input OR G	ate		AL,CL,CP	14	*
				S Data Manual, V		& See

^{*} See the CMOS Data Manual, Volume 1, Standard Logic.

See the Telecommunications Data Manual.

	Device			Function		Suffix	Pins	Page
	MC140	76B	Quad D-Type	Register	ry.Counter	AL,CL,CP	16	MG140
	MC140	77B	Quad Exclusi	ve NOR Gate	Shift Bagister	AL,CL,CP	14	MC140
	MC140	78B			ter/Divider		14	MQ140
ı	MC140	81B			ut NAND Gate		14	MG140
ı	MC140	82B			ut.NAND Gata		14	MQ140
	40	85B	MO 10 15	06B - Functional		7-Stage Rip		
	MC140	93B	Quad 2-Input	NAND Schmitt	Trigger			MONTHS
	MC140				ore Latch			04 PM
	MC140	97B			plexer/			
							0.4	M(*140
	40	98B	See MC145	28B - Normally F	Pin for Pin			
	MC140	199R	8-Rit Address	sable Latch	5578 - Functional	AL,CL,CP	16	40
	MC141		Synchronous	Programmable [Decade Counter	AL CL CP		MC140
	MC141				4-Bit Binary			MC140
	IVIC 141	16			+-Dit Dillary			MC140
	MC141	62B			Decade Counter			MC140
	MC141	The second second			4-Bit Binary			MC140
	IVIC 141	036	Counter	riogrammable 4	+-DIL DILIALY	ALCL CD		MC140
	MC141	7/10						MC140
	MC141		Ouad D Elia E	Jp	dota.l.a	AL,CL,CP		MC140
	MC141		4 Pit Univers	al Chift Bagister		AL,CL,CP		MC140
	MC141							_
	MC144	12020	PCM Monoci	rcuit	indonation - educ	Sec-INIC 14		• 40
	MC144		PCM Monoci	rcuit		Hex Inverte	18	MC140
	IVIC 144	021				rettue kell		MC140
	MC144	02	DCM Manasi	/Demultiplexer	Analog Multiplexer Anel Analog Multi	8-Channel	28	MC140
	MC144		PCM Managi	rcuit	nnet Analog Mutt	Duel 4-Che	16 16	MC140
	MC144		PCIVI IVIONOCI	rcuit		Demyittiples		•
			Binary-to-Pho	one Pulse Conver	ter	L,P	16	MC 140
	MC144				ter		16	•
	MC144 MC144				SARR Functional	L,P	16	010.7
	MC144				Isnouncia - 84 Ad I Vilsimoli - 86 Ad	L,P	200.00	2-7
	MC144	rana i	DCM Cample	v Speed Wodern	Note A	FL,FP,VL,VP	16	
	IVIC 144	.13	r Civi Sample	u Data Filter, See	581B - Functional	L,F,	16 18	ON ·
	MC144	14	DCM Cample		Note A			
	1010144	14	r Civi Sample			7		Me140
	MC144	15	Ound Propini	Timor/Driver		TEL EL ED	18	
	1010144	15	Quad Frecisio	on Timer/Driver	lenumonov - 8086		16	OA *
	MC144	16	DCM Time CI	-	it allul videtiwe po	EVL, VL, VP	100	
	MC144		PCIVI Time Si	ot Assigner Circu	IT	L,P	16	MC 140
		1. P	PCM Time Si	ot Assigner Circu	itelgisluM golsna I	AM BOD-8	18	MCLAG
	MC144	T. P.			it	L,P	22	140
	MC144	30.00			der	ulox3 Lpu0	16	*
	MC144	B. 9.	8 × 14-Bit St	atic runing iviem	ory		16	2-10
	MC144	29	i uning iviemo	ory Control, See I	Note B	Drugt 4-Inpu	18	2-13
								MC140

 [★] See the CMOS Data Manual, Volume 1, Standard Logic.
 See the Telecommunications Data Manual.

Note A: Add Suffix 1 or 2. Example MC14413L2. Note B: Add Suffix B. Example MC14429PB.

Device		Function		Suffix	Pins	Page
MC14430	Innut Addre	ss Encoder		Dug 5-In	16	2-17
MC14433	3-1/2 Digit A	A/D Converter	eerTivtin	1911Pa	24	
MC14442		ssor Compatible A/D			28	
MC14443		A/D Converter Subsys			16	
MC14444	Microproces	ssor Compatible A/D	Converter	Prquam	408	
MC14447		A/D Converter Subsys			16	2-42
4449UB	See MC140	1491IR Pin for Pin F	quivalent	Dual 4-Ch	398	MC145
MC14457	Remote Cor	ntrol Transmitter	nable Oscillator-1	nmsigora Poo	16	2-57
MC14458	Remote Cor	ntrol Receiver	Minner mentiges-	Pos	24	
MC14466	Low Cost S	moke Detector	Amorati mempes-	P.	16	2-68
MC14467	Low Cost S	moke Detector	o F	with Ripp		2-68
MC14468	Interconnec	t Smoke Detector	96-1-63-1-0-5-97-9	P P	16	2-73
MC14469	Addressable	Asynchronous Recei	ver/Transmitter	L,P	40	2-74
MC14490		t Bounce Eliminator			16	2-82
MC14493	Binary-to-7	-Segment Latch Deco	der/Driver	L,P	16	2-89
MC14494		-Segment Latch Deco			dea	2-89
MC14495		-Segment Hexade			16	2-89
		iver, See Note C			16	
MC14497		te Control Transmitte			18	2-99
MC14499		egment LED Display		snia Paud	18	2-104
MC14500B		ontrol Unit		AL,CL,CP	16	2-110
MC14501UB	Triple Gate.		immad aktabak/ ti	AL,CL,CP	16	MC*145
MC14502B	Strobed Hex	x Inverter/Buffer	danailitaman.2.	AL,CL,CP		MC 45
MC14503B	Hex 3-State	Buffer	mitaminami s	AL,CL,CP	16	MC145
MC14504B	Hex TTL c	or CMOS to CMOS	Level Shifter	AL,CL,CP	16	MC*145
MC14506UB	Dual Expand	dable AOI Gate		AL,CL,CP	16	MC*145
MC14508B	Dual 4-Bit L	atch		AL,CL,CP	24	MC*145
MC14510B	BCD Up/Do	wn Counter	tenebession T	AL,CL,CP	16	NC*145
MC14511B	BCD-to-7-S	egment Latch/Decod	er/Driver	AL,CL,CP	188	
MC14512B	8-Channel [Data Selector		AL,CL,CP	16	*
MC14513B	BCD-to-7-S	egment Latch/Decod	ler/Driver	Dual Progi		MC145
16 *	with Ripple	Blanking		AL,CL,CP	18	2-131
MC14514B	4-Bit Trans	parent Latch/4-to-16	Line oldernmen	Quad Prog		
16 2-199	Decoder (Hi	gh)	gmo0 eldsmms i	AL,CL,CP	24	MC145
MC14515B		parent Latch/4-to-16			75	MC145
24 2-208	Decoder (Lo	ow)	noteige@modi	AL,CL,CP	248	MC*145
MC14516B	Binary Up/D	own Counter	imetic bogic Unit	AL,CL,CP	168	MC*145
MC14517B		Static Shift Register			168	MC*145
MC14518B	Dual BCD U	p Counter	nite Friggermann	AL, CL, CP		MC*145
MC14519B		r Selector				MC*145
MC14520B	Dual Binary	Up Counter	nitude Comparet	AL,CL,CP	16	MC*145
MC14521B		requency Divider		AL,CL,CP	100	MC*145
MC14522B		ble BCD Divide-by-N			10	MC*145
MC14526B MC14527B		ble Binary Divide-by-l		AL,CL,CP		MC145
MC14527B	Dual Manag	lultiplier table Multivibrator	4513B - Nomal	AL,CL,CP	16	* 47
MC14528B		nnel Analog Data Sele		AL,CL,CP AL,CL,CP	16	*
WIC 14323B	Dual 4-Chai	inel Analog Data Sele		AL, CL, CP	16	*

[★] See the CMOS Data Manual, Volume 1, Standard Logic.

Note C: There are two versions of this device, with different electrical and switching characteristics. To order, one has suffix L or P and the other L1 or P1. See data sheets for details.

Device and	Function noisonuT	Suffix	Pins	Page
MC14530B	Dual 5-Input Majority Logic Gate	AL,CL,CP	16	M ® 144
MC14531B	12-Bit Parity Tree		16	M#144
MC14532B	8-Bit Priority Encoder		16	M#144
MC14534B	5-Decade Counter			M@144
MC14536B	Programmable Timer			M#144
MC14538B	Dual Precision Monostable Multivibrator			M#144
MC14539B	Dual 4-Channel Data Selector/Multiplexer		16	
MC14541B	Programmable Oscillator-Timer		14	*
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver	AL CL CP	16	2-153
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver	Remote Co	58	MC144
16 2-68	with Ripple Blanking	ALCI CP	18	2-158
MC14547B	High Current BCD-to-7-Segment	Low Cost	178	MC144
16 2-73	Docador/Driver	ALCI CD	16	2-164
MC14548B	Dual Monostable Multivibrator	Addressabl		MC144
1010145466	(Retriggerable/Recettable)	Her Conta	168	MC144
MC14549B	(Retriggerable/Resettable)	AL,CL,CP	16	2-169
MC14551B	Quad 2-Channel Analog Multipleyer/	Binary-to-	94	MC144
16 2-89	Demultiplexer 3-Digit BCD Counter 2 × 2-Bit Parallel Binary Multiplier	AL,CL,CP	16	MC144
MC14553B	3-Digit BCD Counter 2 9 9 9 19 4 998 19 41	AL,CL,CP	16	
MC14554B	2 × 2-Rit Parallel Ripary Multiplier	AL,CL,CP		MC144
MC14555B	Dual Binary to 1-of-4 Decoder	AL,CL,CP		MC144
MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)		16	MC145
MC14557B	46.10.10	AL,CL,CP	8160	MC145
MC14557B	1-to-64 Bit Variable Length Shift Register	AL,CL,CP	16	2-183
MC14558B	BCD-to-7-Segment Decoder	AL,CL,CP	0.00	2-169
0.7	Successive Approximation Register	AL,CL,CP	16	2-169
MC14560B	NBCD Adder	AL,CL,CP	16 14	*
MC14561B		AL,CL,CP	14	MC145
MC14562B	128-Bit Static Shift Register	AL,CL,CP	16	MC145
MC14566B	Industrial Time-Base Generator	AL,CL,CP		MC145
MC14568B	Phase Comparator and Programmable			2-189
MC14ECOR	Counters	AL,CL,CP	16	2-189
MC14569B	Dual Programmable BCD/Binary Counter	AL,CL,CP	16	
MC14572UB	Hex Gate	AL,CL,CP	16	*
MC14573	Quad Programmable Op Amp	CL,CP	16	2-199
MC14574	Quad Programmable Comparator	CL,CP	16	2-199
MC14575	Programmable Dual Op Amp/Dual Comparator	CL,CP	16	2-199
MC14580B	4 × 4 Multiport Register	AL,CL,CP	24	2-209
MC14581B	4-Bit Arithmetic Logic Unit	AL,CL,CP	24	MC1 4.6
MC14582B	Look-Ahead Carry Block	AL,CL,CP	16	MC145
MC14583B	Dual Schmitt Trigger	AL,CL,CP	16	MC146
MC14584B	Hex Schmitt Trigger	AL,CL,CP	14	MC145
MC14585B	4-Bit Magnitude Comparator	AL,CL,CP	10	MC145
MC14597B	8-Bit Bus Compatible Counter Latch		16	MC145
MC14598B	8-Bit Bus Compatible Addressable Latch	AL,CL,CP	18	MC145
MC14599B	8-Bit Addressable Latch	AL,CL,CP		MC145
4734B	See MC14513B - Normally Pin for Pin			MC145
16 *	Equivalent Selector			
	and the second second second second second second			

^{*} See the CMOS Data Manual, Volume 1, Standard Logic.

& See the CMOS Data Manual, Volume 1, Standard Logic.

Device	Pins		Function		Suffix	Pins	Page
885-40	014B	See MC14584B -	Normally P	in for Pin			MC145
2-269		Equivalent		ncy Synthesizer	PLL Freque		
282 40		See MC14585B -				112	
2-275		Equivalent		ncy Synthesizer	PLL Freque	143	
40	097B	See MC14503B -	Normally P	in for Pin	4-Bit Data	144	MC145
	The same of the sa	Equivalent			Synthesize		
40	101B	See MC14531B -	Functionall	y Equivalent		145	MC145
04 284	106B	See MC14106B -	Pin for Pin	Equivalent			
40	108B	See MC14580B -	Normally P	in for Pinugal aug			MC145
		Equivalent					
408-40	160B	See MC14160B -	Pin for Pin	Equivalent		151	
218 40	161B	See MC14161B -	Pin for Pin	Equivalent	Parallel Inp		
028 40		See MC14162B -	Pin for Pin	Equivalent	Serial Input		
828-40	163B	See MC14163B -	Pin for Pin	Equivalent	Serial Input		
868 40		See MC14174B -	Pin for Pin	Equivalent			
888 40	175B	See MC14175B -	Pin for Pin	Equivalent			
40		See MC14581B -	Pin for Pin	Equivalent			
40	182B	See MC14582B -	Pin for Pin	Equivalent	Dual Tunea		MC145
40	192B	See MC14510B -	Functionall	y Equivalent	Dual Tuner	415	
0 40	193B	See MC14516B -	Functionall	y Equivalent			
	194B	See MC14194B -	Normally P	in for Pin		420	MC145
	24	Equivalent					
40	208B	See MC14580B -	Normally P	in for Pin			MC145
		Equivalent					
MC142	100	4 × 4 Cross Point S	witch	iiversal Digital-Loo	AL,CL,CP	16	MC145
MC144	100	Duplex Mode 32-S	egment LEI	Driver	(2- Aire Ma	24	2-214
MC144	104	High Performance	Remote Co	introl Fransmitter	P	24	2-225
MC144	105	Remote Control Tr. Hex D/A Converter	ansmitter	(9V	(4-Vaire Sia	20	2-226
MC144	110	Hex D/A Converter	p Transcen	iversal Digital-Loo	MDESK U	18	2-227
MC144	111	()uad I)/A Convert	er		P	14	2-227
MC144	115	16-Segment LCD I 4-Digit Duplex Mod	Driver		Date Set In	24	2-232
MC144	117	4-Digit Duplex Mod	de LCD Dec	oder/Driver	Teler Aud	24	2-237
MC144	122	Remote Control Re	ceiver		P	16	2-244
MC144	124	High Performance	Remote Cor	ntrol Receiver	26Q Hz T	24	2-245
MC144	130	High Performance TV Stereo Decoder			A elds Pour	28	2-246
MC145	000	48-Segment Multip	olexed LCD	Driver (Master)	L, P	2	2-247
MC145	001	44-Segment Multi				18	2-247
MC145	026	Remote Control En	coder		L,P	16	2-257
MC145	027	Remote Control De	coder		L,P	16	2-257
MC145	028	Remote Control De	coder	processor, Expand	L,P L,P	16	2-257
MC145	029	Remote Control De	coder	Chip Microcompu	L,P	16	2-257
MC145	040	Remote Control De Remote Control De Serial A/D Convert Serial A/D Convert	er	Chip Microcompu	P P	20	2-268
MC145	041	Serial A/D Convert	er		emi L,Pen	20	2-268
MC145	100	4 × 4 Cross Point S PLL Frequency Syr	witch	90614	L,P	16	IVIC
MC145	104	PLL Frequency Syr	thesizer	Chip Microcompu	2 8-Bd Single	16	2-269
MC145	106	PLL Frequency Syr	thesizer	3it Static RAM	25 q × 4-E	180	2-269

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	Device and		Function		Suffix	Pins	Page
	MC145107	PLL Frequency	Synthesizer	SGABNormaliy	SeePMC14	8160	2-269
	MC145109					16	2-269
ı	MC145112	PLL Frequency	Synthesizer	SSSSNormally	See9MC14	8180	2-269
ı	MC145143					16	2-275
ı	MC145144			uency of - 8603			
						16	2-277
	MC145145			uencymua - 8188			
				1.068 Pin.toc.Pin		18	2-284
	MC145146			uency of - 8088			
						20	2-294
	MC145151	Parallel Input PL	LL Frequency S	ynthesizer	Seq, Jecia	28	2-304
	MC145152			ynthesizer			2-312
	MC145155			thesizer			2-320
	MC145156			nthesizer		20	2-328
	MC145157			nthesizer			2-338
	MC145158			nthesizer			2-338
	MC145159			nthesizer			2-347
	MC145414			ed Data Filters			2-348
	MC145415			ow Pass		1928	
						16	
	MC145420			Transceiver		1948	_
						24	
	MC145422			Transceiver		8800	0.0
		(2-Wire Master))		England and	22	
	MC145423	MDPSK Univers	sal Digital-Loon	Transceiver	A LOUIS TOP A		
	100	(2-Wire Master))			20	MC142
	MC145425	MDSPK Univer	cal Digital Loop	Transcoiver	Duplex Mo		MC144
	1101.101.20	(4-Wire Slave)	our Digital Loop	Transceiver	High Partor	22	MC144
	MC145426	MDPSK Univers	sal Digital-Loon	Transceiver	Rentote Co	100	MC144
	427.70.90	(2-Wire Slave)	odi Digital Loop		Hex D/A C	22	MC144
	MC145428	Data Set Interfa	ace		L,P	20	MC144
	MC145429	Telset Audio Int	terface	16VMQ QQ23r	L,P L,P	18	MC144
	MC145431	Tuneable Lown	ass/Bandnass F	ilter	L,P	16	MC144
	MC145432	2600 Hz Tone :	Signalling Filter	1501000011011	L,P	18	MC144
	MC145433	Tuneable Notch	/Bandnass Filte	er	L,P	16	MC144
	MC145440				L.P	18	MC144
	MC145441	Low Speed Mod	dem Filter	nt Multiplexed LCC	empi ep8 4	18	MC145
	MC145445	300 Baud FSK I	Modem	nt Multiplexed LCD	4 14,1 gme	220	MC145
	MC145450	1200 Baud ESK	Modem	ntrol Encoder	Require Co	22	MCIAS
	16 2-257	0 0:04:	C WOODON'T	able	L,P,Z		MC145
	MC146805E2	8-Bit Microproc	essor, Expanda	ible		40	MC145
	MC146805F2	8-Bit Single Chi	p Microcomput	er	L,P,Z	28	MC145
	MC146805G2	Book Time Chi	p wiicrocomput	er	L,P,Z	40	MCIAS
	MC146818	Real-Time Clock	K/RAIVI	Converte	L,P,Z	24	MCLAS
	MC146823			- Lab EDDOM	L,P,Z	40	MC145
	MC1468705G2	8-Bit Single Chi	piviicrocomput	er with EPROM	Super P	40	MCIAS
					The state of the s	(-17-6)	

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See the Telecommunications Data Manuel.

See the 8-Bit Microprocessors Data Manual. See the Memory Data Manual. See the Telecommunications Data Manual.

Device	noisonual Function bina riols	Suffix	Pins	Page
MCM145 MCM145 MCM145 MCM145	24 256 × 4-Bit ROM, See Note D	AL,CL,CP AL,CL,CP AL,CL,CP AL,CL,CP	14 16 16 24	2-116 2-139 2-145 2-176
MCM651 MCM651 MCM652 MCM655	47	C,P C,P P L,P	18 28	tand tord tod
+ See the I	102 16 × 16-Bit Static RAM			Inverse Schm Slip-F Coun Adde Parity Alu's Encos Multi
	1-Bit Static RAM 1-Bit Static RAM 4 Multiport Register 4-Bit Static RAM 4-Bit Static RAM 4-Bit Static Tuning Memory 6-Bit Static RAM		14505 14537 45808 14552 14524 4426 144102	MCM MC1 MCM MCM MC1
				PLL Fre
2-2 2-189 2-269 2-269 2-269 2-269				MC1 MC1 MC1

Selection Guide by Function

			VIAH DIBIS HU-I X 40	
2-139			256 x 4-Bit ROM, See Note D	
2-145				MCM14537
Logic F	unction	AL,CL,CP 2		
Nand	Gates	C.P	2048 × 8-Bit Static RAM	MCMB5116
Nor C	Gates	C,P	4088 x 1-8it Static RAM	MCM65147
And	Gates	9	22788 × 8-8t ROM	MCM6525t
Or Ga	ates	9.J	3 2048 x 8-Bit Multiplexed Bus ROM	MCM6551
Com	plex Gate	es)2	MC#//14416
			nslators	
Schn	nitt Trigg	ers		*
Flip-F	lops/Lat	ches		+ She the Mer
Shift	Register	s		*
Coun	iters		ble only by special order.	Note U: Availa
Parity	y Genera	tor/Checker		*
Alu's	/Rate Mi	ultipliers		*
Enco	ders/Dec	oders		*
Multi	plexers/l	Demultiplexer	s/Bilateral Switches	*
			imers	
Micro	process	ors/Periphera	ls	×

Device	Function	Page
Memories (1)		
MCM14505	64 × 1-Bit Static RAM	2-116
MCM14537	256 × 1-Bit Static RAM	2-145
MC14580B	4 × 4 Multiport Register	2-209
MCM14552	64 × 4-Bit Static RAM	2-176
MCM14524	256 × 4-Bit Read Only Memory	2-139
MC14426	8 × 14-Bit Static Tuning Memory	2-10
MCM144102	16 × 16-Bit Static RAM	2-220
PLL Frequency S	ynthesizer	
MC14046B	Phase-Locked Loop	2-2
MC14568B	Phase Comparator and Programmable Counters	2-189
MC145104	PLL Frequency Synthesizer	2-269
MC145106	PLL Frequency Synthesizer	2-269
MC145107	PLL Frequency Synthesizer	2-269
MC145109	PLL Frequency Synthesizer	2-269
MC145112	PLL Frequency Synthesizer	2-269

⁽¹⁾For details of larger CMOS Memories, see the Memory Data Book.

★ See the CMOS Data Manual, Volume 1, Standard Logic.

× See the 8-Bit Microprocessor Data Manual.

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§ See Data Sheet.

MC14573 Quad Programmable Op Amp. MC14574 Quad Programmable Comparator MC14575 Programmable Dual Op Amp/Dual Comparator. MC14575 Programmable Dual Op Amp/Dual Comparator. Remote Control Functions MC144104 High Performance Remote Control Transmitter. MC144105 Remote Control Transmitter MC14457 Remote Control Transmitter. MC14497 Remote Control Transmitter. MC144122 Remote Control Transmitter MC144124 High Performance Remote Control Receiver. MC14458 Remote Control Receiver. MC14469 Adressable Asynchronous Receiver/Transmitter.	Page
Remote Control Functions MC144104 High Performance Remote Control Transmitter	
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MC144104 High Performance Remote Control Transmitter	
MC144104 High Performance Remote Control Transmitter	MC1
MC144105 Remote Control Transmitter MC14457 Remote Control Transmitter MC14497 Remote Control Transmitter MC144122 Remote Control Receiver. MC144124 High Performance Remote Control Receiver MC14458 Remote Control Receiver.	2-225
MC14457 Remote Control Transmitter MC14497 Remote Control Transmitter MC144122 Remote Control Receiver. MC144124 High Performance Remote Control Receiver. MC14458 Remote Control Receiver.	
MC14497 Remote Control Transmitter	
MC144122 Remote Control Receiver	
MC14458 Remote Control Receiver	2-244
MC14458 Remote Control Receiver	2-245
MC14469 Adressable Asynchronous Receiver/Transmitter	2-57
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MC145026 Remote Control Encoder	2-257
MC145026 Remote Control Encoder	2-257
MC145028 Remote Control Decoder	2-257
MC145029 Remote Control Decoder	2-257
Radio/TV Functions Sevind(sebosed) dotal memore 7-of-yrani8	
MC6220 4-Bit Microcomputer Unit with PLL Frequency Synthesizer	
MCM144102 16 × 16-Bit Static RAM	
MC14426 8 × 14-Bit Static Tuning Memory	
MC14429 Tuning Memory Control	2-13
MC14430 Input Address Encoder	2-17
MC144104 High Performance Remote Control Transmitter	2-225
MC144105 Remote Control Transmitter	2-226
MC14457 Remote Control Transmitter	2-57
MC14497 Remote Control Transmitter	2-99
MC144122 Remote Control Receiver	2-244
MC144124 High Performance Remote Control Receiver	
MC14458 Remote Control Receiver	2-58
MC144130 TV Stereo Decoder	2-246
Miscellaneous Compatible A/D Converter Microprocessor Compatible A/D Converter	
MC14411 Bit Rate Frequency Generator	
MC14466 Low Cost Smoke Detector	
MC14467 Low Cost Smoke Detector	2-68
MC14468 Interconnectable Smoke Detector	
MC14469 Addressable Asynchronous Receiver/Transmitter	
MC14490 Hex Contact Bounce Eliminator	
MC14500B Industrial Control Unit	2-110
MC145414 Dual Tuneable Lowpass Filter	2-348

PLL FREQUENCY SYNTHESIZER SELECTOR TABLES

TABLE 1

	MC145104	MC145106	MC145107	MC145109	MC145112	MC145143
Device Programming	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
Modulus	Single	Single	Single	Single	Single	Single
Programmable N Divider Bits	OS ingegrat	-Speed CM	1914 8 991-1	nebrigits to	new earnily	9+4 Fixed Bits
Reference Divider	2 ¹⁰ or 2 ¹¹	None				
Single-Ended PDout (Three State)	Yes	Yes	Yes	Yes	Yes	Yes
Double-Ended OV, OR	No	No	No	No	No	No
Lock Detect Output	Yes	Yes	Yes	Yes	Yes	Yes
Band Switch Outputs	No	No	No	No	No	No
Package (Pins)	16	18	7 8 11 16	ysis 16 noin	gsqc18-1. bas	1118 116 D
Frequency Tripling Capability	No	Yes	Yes	1ge -oN 2-6	ISA Nolleys	gO sNoW
10.24 MHz Oscillator Circuit	Yes	Yes	No	No	Yes	No
External Frequency Reference Only	No	No	Yes	Yes A.	No	Yes
Typical Max. F.in at 5 V, 25°C	10 MHz	10 MHz	10 MHz	10 MHz	0 10 MHz	30 MHz

TABLE 2

Input Logic Compatible with CMOS Parts (HCXXXX or HC4XXX)

· Proven Reliability and Process

	MC145144	MC145145	MC145146	MC145151	MC145152	MC145155	MC145156	MC145157	MC145158	MC145159
Device Programming	4-Bit Data bus	4-Bit Data bus	4-Bit Data bus	Parallel	Parallel	Serial	Serial	Serial	Serial	Serial
Modulus	Single	Single	Dual	Single	Dual	Single	Dual	Single	Dual	Dual
Number of N Divider Values A	512 —	16,380	1,021 128	16,380	1,021 64	16,380	1,021 128	16,380	1,021 128	1,021
Range of Divider Values N	4- 4,092 —	3- 16,383 —	3- 1,023 0- 127	3- 16,383 —	3- 1,023 0- 63	3- 16,383 —	3- 1,023 0- 127	3- 16,383	3- 1,023 0- 127	3- 1,023 0- 127
Range of Reference Divider Values	3,584- 3,839	3- 4,095	3- 4,095	8- 8,192	8- 2,048	16- 8,192	8- 2,048	3- 16,383	3- 16,383	3- 16,383
Single-Ended PDout (three state)	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
Double-Ended OV, OR	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Lock Detect Output	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Band Switch Outputs	No	No	No	No	No	Yes	Yes	No	No	No
Package (pins)	16	18	20	28	28	18	20	16	16	20
Typical Max. F.in at 5 V, 25°C	30 MHz	30 MHz	30 MHz	30 MHz	30 MHz	30 MHz	30 MHz	30 MHz	30 MHz	30 MHz
	25.25	277 1				1 200 200 20				

^{*} Preview Data

Introducing a new dimension in CMOS¹

Motorola's new family of standard-logic High-Speed CMOS integrated circuits provides the designer with a complete series of functions which approaches the ideal in performance.

All of the present CMOS logic family features, including low power dissipation and high noise immunity, combine with LSTTL speeds, pinouts and drives to offer the marketplace a new dimension in CMOS standard logic.

- Guaranteed Propagation Delay 15 ns for 74HC00
- Wide Operating Range 2-6 V Recommended
- High Noise Immunity Typically 45% of Supply Voltage
- Low Quiescent Power Dissipation
- Diode Protection All Inputs
- High Fanout 10 LSTTL Loads (4 mA Drive)
- Direct Pin Compatibility with LSTTL Parts (HCXXX or HCTXXX) and CMOS Parts (HC4XXX)
- Input Logic Compatible with CMOS Parts (HCXXX or HC4XXX) and/or LSTTL Parts (HCTXXX)
- Proven Reliability and Process

	MC145159			BASIC	NUMB	ERING PA	ARAMETE	RS			
				MC	VV	www	XXXX Y				
Example	: Isu0			Single	Bust	Single	Bud				
Motorola	Circuit	Identifier	1,021	16,380	1,021	16,380	1,021				Reminer of Divider Values
Tempera		- 000,00	3-	O°C to 8	25.90	3-16,383	3-				Range of Divider Values
				C to 125			127			(A	
High-Spe	eed CMC	S Specif		16- 8-192	8- 2 048	8,192	4,025	don a	ckage Ty N for Pla		74 Series Only
HC fo		ed High-S	Speed CN	/IOS			Yes	29¥ •	J for Ce	ramic	Slegte-Emiré Pilost (three etate)
• HCU	for Unbu	ffered Hi	gh-Spee	d CMOS	SBA		Yes	——Ва	sic Devic	е Тур	Deable-Ended FV. 90
• HCT	for TTL I	nput Con	npatible	CMOS*		* Not Av	ailable On	All Devi	ces		
					No						
1 For ful	informa	tion see	the CM	OS Data I	Manual	Volume	3, High S	need CN	105		

HIGH SPEED CMOS FUNCTION SELECTOR GUIDE

- Parts shown are functional equivalent except when preceded by an asterisk (*), indicating a suggested alternative
- Device numbers preceded by a "★" are new proprietary designs

High-Speed		Functional	Functional Equivalent	Direct Pin	Number o
Device Number	Function	Equivalent LSTTL Device	CMOS Device MC1XXXX or	Compatibility	Pins
MC74/MC54	LS242 LS	74/54	CDXXXX	Quad Bu	HC242
BATES	21 01021	nint2.c.	ng Output	19 hand	CROSS
HC00	Quad 2-Input NAND Gate	LS00	4011	LS	14
HC02	Quad 2-Input NOR Gate	LS02	4001	LS	ACT14
HC03	Quad 2-Input NAND	LS03	*4011	LS	48014
20	with Open Drain Outputs	r, 3-State	s Transceive	Octal Bu	HC643
HC08	Quad 2-Input AND Gate	LS08	4081	LS	14
HC10	Triple 3-Input NAND Gate	LS10	4023	LS	14
HC11	Triple 3-Input AND Gate	LS11	4073	LS	14
HC20	Dual 4-Input NAND Gate	LS20	4012	LS	14
HC27	Triple 3-Input NOR Gate	LS27	4025	LS	14
HC30	8-Input NAND Gate	LS30	4068	LS	14
HC32	Quad 2-Input OR Gate	LS32	4071	MILS	8314
HC51	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	LS51	*4506	LS	14
★ HC58	2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates	*LS51	*4506	9-Bit Ob Gener	14
HC86	Quad 2-Input Exclusive OR Gate	LS86	4070	LS	14
HC132	Quad 2-Input Schmitt-Trigger NAND Gate	LS132	4093		41:881 HC456
HC133	13-Input NAND Gate	LS133		LS	16
HC266	Quad 2-Input Exclusive NOR Gate (Non Open Drain)	LS266	4077	LS/CMOS	es 14
HC4002	Dual 4-Input NOR Gate	*LS25	4002	CMOS	14
HC4075	Triple 3-Input OR Gate	Danialo Anus	4075	CMOS	14
HC4078	8-Input NOR Gate		4078	CMOS	14
BUFFERS / IN	IVERTERS			SHOTALLS	on raugura
HC04	Hex Inverter	LS04	*4069	LS/CMOS	14
HCU04	Hex Unbuffered Inverter	LS04	4069	LS/CMOS	14
HC14	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HC240/	Octal Buffer/Line Driver/Line Receiver,	LS240	Type Latch	LS	20
HCT240	3-State, Inverting Output	A hos to 2 d	Flip-Flop wit	L leud	NC 218
HC241/	Octal Buffer/Line Driver/Line Receiver,	LS241	Flia-Flag wit	LS	20
HCT241	3-State		the day of the		0.000
HC244/ HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244	riip-rop wii re-Edge Trigg	LS	20
HC365	Hex 3-State Bus Driver with Common 2-Input NOR Enable	LS365A	Flip-Flop will ive-Edge Trig	LS	16
HC366	Hex 3-State Bus Driver with Common 2-Input NOR Enable,	LS366A	Flip-Flop wit ive-Edge Trig	LS	16
	Inverting Output			Hex D-	HC174
HC367	Hex 3-State Bus Driver with Separate 2-Bit	LS367A	4503	LS/CMOS	16
	and 4-Bit Sections	riot			HC259
HC368	Hex 3-State Bus Driver	LS368A		LO	16
	with Separate 2-Bit and 4-Bit Sections, Inverting Output	k/Reset trent Latch,		with D-	HC373
HC540	Octal Buffer/Line Driver/Line Receiver, 3-State Inverting Outputs	LS540	e Type Filp-Flo	LS	20
HC541	Octal Buffer/Line Driver/Line Receiver, 3-State	LS541		LS	20
HC4049	Hex Inverting Buffer	Jugru	4049	CMOS	16
HC4050	Hex Buffer		4050	CMOS	16

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			1
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		н	

High-Speed Device Number MC74/MC54	Function hen preceded by an asteriak (*),	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number o
SCHMITT TR	IGGERS emplesh vistelingo	are new pri	"#" s yd bel	imbers preced	Davice nu
HC14 HC132	Hex Schmitt-Trigger Inverter Quad 2-Input Schmitt-Trigger NAND Gate	LS14 LS132	4584 4093	LS/CMOS LS	14 14
BUS TRANSO	CEIVERS # # CMO Device Transvision	not	Penet		Device
HC242	Quad Bus Transceiver, 3-State,	LS242		LS	14
110212	Inverting Output	LOZIZ		20	0.754.0
HC243	Quad Bus Transceiver, 3-State	LS243		LS	14
HC245/	Octal Bus Transceiver, 3-State	LS245	Input NAND	SJEE	20
HCT245	81	87.0	Input NOR G Input NAND	Quad 2-	HCOZ
HC640	Octal Bus Transceiver, 3-State	LS640	ngur namu Ipan Drain O	Delives	20
HC643	Octal Bus Transceiver, 3-State	LS643	a and made	-0-4	20
HC646	Octal Bus Transceiver and Register, 3-State	LS646	Input NAND	E elghs	01024
HC648	Octal Bus Transceiver and Register, 3-State, Inverting Output	LS648	Input AND C		24 0SOH
ARITHMETIC	CIRCUITS	916	to non rogni	-c eigitt	DEOL
HC85	4-Bit Magnitude Comparator	LS85	*4585	SILS	16
HC181	4-Bit Arithmetic Logic Unit	LS181	4581	LS/CMOS	24
HC182	Carry Lookahead Generator	LS182	4582	LS/CMOS	16
HC280	9-Bit Odd/Even Parity	LS280	*4531	LS	14
	Generator/Checker	sate	S SO GIVE P		GUITE
HC283	4-Bit Binary Full Adder with Fast Carry	LS283	4008	LS	16
HC888 HC4560	8-Bit Equality Comparator NBCD Adder	teggirT-t	4560	CMOS	20
MISCELLANE	OUS		NAND Gate	hugal-E F	HC133
HC292	Programmable Frequency Divider/	LS292	nput Exclusi	LS	16
110202	Digital Timer	20202	(pen Drain)	Non (Non C	
HC294	Programmable Frequency Divider/ Digital Timer	LS294	iput NOR Ga input OR Gar	LS	16
HC4046	Phase-Locked Loop	*LS297	4046	CMOS	16
FLIP-FLOPS /	LATCHES			INVERTERS	BREERS
HC73	Dual J-K Flip-Flop with Reset	LS73A	*4027	LS	14
HC74	Dual D-Type Flip-Flop with Set and Reset, Positive-Edge Triggered	LS74A	4013	LS	14
HC75	4-Bit D-Type Latch	LS75	*4042	LS	16
HC76	Dual J-K Flip-Flop with Set and Reset	LS76A	*4027	LS	16
HC107	Dual J-K Flip-Flop with Reset	LS107A	4027	LS	14
HC109	Dual J-K Flip-Flop with Set and Reset, Positive-Edge Triggered	LS109A	*4027	LS	16
HC112	Dual J-K Flip-Flop with Set and Reset, Negative-Edge Triggered	LS112A	*4027	LS	16
HC113	Dual J-K Flip-Flop with Set, Negative-Edge Triggered	LS113	*4027	LS	ваезн
HC174	Hex D-Type Flip-Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HC175	Quad D-Type Flip-Flop	LS175	4175	LS/CMOS	16
HC259	8-Bit Addressable Latch	LS259	*4099	LS	16
HC273	Octal D-Type Flip-Flop with Common Clock/Reset	LS273	*4175	S.E. LS	20
HC373/ HCT373	Octal D-Type Transparent Latch, 3-State	LS373	eparate 2-Bi Sit Sections,	A brits	20
HC374/ HCT374	Octal D-Type Flip-Flop, 3-State	LS374	Her/Line Orly a inversing C	LS	20
HC533	Octal D-Type Transparent Latch, 3-State Inverting Output	LS533	far/Line Driv	and the same of	20
			reing Suffer	The second secon	HC404

High-Speed Device Number MC74/MC54	Functional Equivalent Equivalent Service Pro- TAIST Device MCTXXXX or 7AISA CDXXXX	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
FLIP-FLOPS/L	LATCHES (continued)	RIVERS	MINSPLAY D	S/ENCODERS	DECODER
HC534	Octal D-Type Flip-Flop, 3-State,	LS534	-of-10 Deck ecoder/Dem	of CLS	20
HC563	Inverting Output Octal Transparent Latch, 3-State,		atched Input		20
HC564	Inverting Output Octal D-Type Flip-Flop, 3-State, Inverting Output	LS580	ecoder/Dem f-4 Decoder		20
HC573 HC574	Octal Transparent Latch, 3-State Octal D-Type Flip-Flop, 3-State	LS573 LS574	e-Low Outpt Priority Enco		20
SHIFT REGIS			Decoder	4-to-16	HC154
HC164	8-Bit Serial Input/Parallel Output	LS164	*4034	LS	14
HC165	Shift Register 8-Bit Serial or Parallel Input/Serial	LS165	*4021	-ot-G2S	16
HC173	Output Shift Register 4-Bit D-Type Register, 3-State	LS173	4076	LS/CMOS	16
HC194	4-Bit Bidirectional Universal Shift Register	LS194A	4194	LS/CMOS	16
HC195	4-Bit Universal Shift Register	LS195A	*4035	LS	16
HC299	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS -Q HB-A	20
★ HC589	8-Bit Parallel-to-Serial Shift Register with Input Latches, 3-State	*LS597	*4014 or*4021	Octal Bu 3-Star	16
HC595	8-Bit Serial-to-Parallel Shift Register, 3-State	LS595	*4034	S-Stat	61241 HCT24
HC597	8-Bit Parallel-to-Serial Shift Register with Input Latches	LS597	*4014 or *4021	E baLS	16
COUNTERS	61 01203	Tevledante	otate dus 11	-c bend	CPSUM
HC160	Programmable Decade Counter, Asynchronous Clear	LS160A	4160	LS/CMOS	16
HC161	Programmable 4-Bit Binary Counter, Asynchronous Clear	LS161A	4161	LS/CMOS	16
HC162	Programmable Decade Counter, Synchronous Clear	LS162A	4162	LS/CMOS	16
HC163	Programmable 4-Bit Binary Counter, Synchronous Clear	LS163A	4163	LS/CMOS	16
HC192	Presettable BCD Decade Up/Down Counter	LS192	4510	S-Stat	16
HC193	Presettable 4-Bit Binary Up/Down Counter	LS193	4516	LS	16
HC390	Dual Decade Counter	LS390	*4518	LS	16
HC393	Dual 4-Bit Binary Counter	LS393	*4520	LS	14
HC4017 HC4020	Decade Counter/Divider 14-Stage Binary Ripple Counter	put NOR Eni	4017 4020	CMOS	16 16
HC4024	7-Stage Binary Ripple Counter	na 2 della	4024	CMOS	14
HC4040	12-Stage Binary Ripple Counter	er with Sept	4040	CMOS	16
HC4060	14-Stage Binary Ripple Counter with Oscillator	er with Sepa	4060	CMOS	16
MONOSTABL	LE MULTIVIBRATORS		ing Output	Invert	
HC123	Dual Retriggerable Monostable Multivibrator	LS123	*4538 or *4528	LS Cotal Tr	16
HC221	Dual Monostable Multivibrator	LS221	*4538 or *4528	Q lat D	16
HC423	Dual Monostable Multivibrator	LS423	*4538 or *4528	sta-LS	16
HC4538	Dual Precision Retriggerable/Resettable Monostable Multivibrator	*LS221	4538	CMOS	16

High-Speed Device Number MC74/MC54	Functional Equivalent Direct Plu Equivalent Compatibili Compatibili Compatibili TA454 CDXXXX or TA454 CDXXXX	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins	
DECODERS/	ENCODERS/DISPLAY DRIVERS		(beunimoo	S/LATCHES (LIP-FLOP	
HC42 HC137	BCD to 1-of-10 Decoder 1-of-8 Decoder/Demultiplexer	LS42 LS137	*4028 *4028	-ClatLS	16	
HC138/	with Latched Inputs, Inverting Output	LS138	*4028	Octal Fr 21nvert	16	
HCT138 HC139	1-of-8 Decoder/Demultiplexer Dual 1-of-4 Decoder (Active-Low Outputs)	LS139	4555	LS/CMOS	16	
HC147	10-to-4 Priority Encoder	LS147	*4532	Octal Tr	16	
HC154	4-to-16 Decoder	LS154	*4514	LS	24	
HC237	1-of-8 Decoder/Demultiplexer with Latched Inputs	*LS137	*4028	8-Bit Se	16	
HC4511	BCD-to-7-Segment Latch/Decoder/Driver	*(LS46- LS49)	4511	LS/CMOS	16	
HC4514 HC4543	4-Bit Latch/4-to-16 Line Decoder BCD-to-7 Segment Latch/Decoder/Driver for Liquid-Crystal Displays	Line Decoder				
BUS-COMPA	TIBLE DEVICES	Register	Worsel Shift	hU sig A	661911	
HC173	4-Bit D-Type Register, 3-State	LS173	4076	LS/CMOS	16	
HC240/ HCT240 HC241/	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output Octal Buffer/Line Driver/Line Receiver,	LS240 LS241	allel-to-Seria rout Latches rial-to-Paralle	SJ _{ift} Parish In	20	
HCT241 HC242	3-State Quad 3-State Bus Transceiver,	LS242	e ellel-to-Seria	sta ES	23.14	
HC243	Inverting Output Quad 3-State Bus Transceiver	LS243	sput Latches	l diw	14	
HC244/	Octal Buffer/Line Driver/Line Receiver,	LS244		LS	20	
HCT244 HC245/	3-State	LS245	mable Decad hronous Cle	onys/LS	20	
HCT245 HC251	Octal Bus Transceiver, 3-State 8-Input Multiplexer, 3-State	LS251	*4512	onys/LS	16	
HC253 HC257	Dual 4-Input Multiplexer, 3-State Quad 2-Input Data Selector/Multiplexer, 3-State	LS253 LS257	*4539 *4519	LS/CMOS LS	16	
HC299	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS	20	
HC354	8-Input Multiplexer, 3-State	LS354	*4512	LS	20	
HC356 HC365	8-Input Multiplexer, 3-State Hex 3-State Bus Driver	LS356 LS365A	*4512	LS	20	
HC366	with Common 2-Input NOR Enable Hex 3-State Bus Driver	LS366A	ade Counts it Binary Cor	ed laud	88316	
ar	with Common 2-Input NOR Enable, Inverting Output	190	Counter/Divi e Binary Ripp	Decade 14-Stag	HC401	
HC367	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections	LS367A	4503	LS/CMOS	16	
HC368	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections,	LS368A	a Binary Ripp Iscillator	S1-Stag	80416	
UC272/	Inverting Output	10070		VBLE MULTIN		
HC373/ HCT373 HC374/	Octal Transparent Latch, 3-State	LS373 LS374	riggerable M ibrator	Pulling Res	20	
HCT374	Octal D-Type Flip-Flop, 3-State	tivibrator	nostable Mu	Dual Mo	00 HC22	
HC533	Octal D-Type Transparent Latch, 3-State, Inverting Output	LS533	nostable Mu	LS Dual Mo	02 HC423	

High-Speed Device Number MC74/MC54	Functional Equivalent Equivalent Compatibil Compatibil LETTL Device XXXX xx xx	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins			
BUS-COMPA	TIBLE DEVICES (continued) (bauni	inoo) (JATIE	DIG GIVA DO	EXERS (ANAL	MULTIPLE			
HC534	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS534	islog Switch evel Transla		84020			
HC540	Octal Buffer/Line Driver/Line Receiver, 3-State Inverting Outputs	LS540	alog Multipli atched Selec	A beLS	20			
HC541	Octal Buffer/Line Driver/Line Receiver, 3-State	LS541	hannel Anal lexer/Demult	2 SJal 4-C	E4020			
HC563	Octal Transparent Latch, 3-State, Inverting Output		atched Selec Channel Ana		20 * HC43			
HC564	Octal D-Type Flip-Flop, 3-State, Inverting Output		lexer/Demult atched Seler		20			
HC573	Octal Transparent Latch, 3-State	LS573		LS	20			
HC574	Octal D-Type Flip-Flop, 3-State	LS574		LS	20			
★HC589	8-Bit Parallel-to-Serial Shift Register	*LS597	*4014 or		16			
HC595	with Input Latches, 3-State 8-Bit Serial-to-Parallel Shift Register, 3-State	LS595	4021 *4034	LS	16			
HC640	Octal Bus Transceiver, 3-State	LS640		LS	20			
HC643	Octal Bus Transceiver, 3-State	LS643		LS	20			
HC646	Octal Bus Transceiver and Register, 3-State	LS646		LS	24			
HC648	Octal Bus Transceiver and Register, 3-State	LS648		LS	24			
TTL INPUT C	OMPATIBLE DEVICES			No. of the last of				
HCT138	1-of-8 Decoder/Demultiplexer	LS138	*4028	LS	16			
HCT240	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS240		LS	20			
HCT241	Octal Buffer/Line Driver/Line Receiver, 3-State	LS241		LS	20			
HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244		LS	20			
HCT245	Octal Bus Transceiver, 3-State	LS245		LS	20			
НСТ373	Octal D-Type Transparent Latch, 3-State	LS373		LS	20			
HCT374	Octal D-Type Flip-Flop, 3-State	LS374		LS	20			
MULTIPLEXE	RS (ANALOG AND DIGITAL)							
HC151	8-Channel Digital Multiplexer	LS151	*4512	LS	16			
HC153	Dual 4-Channel Digital Multiplexer	LS153	4539	LS/CMOS	16			
HC157	Quad 2-Input Data Selector/Multiplexer	LS157	*4519	LS	16			
HC158 HC251	Quad 2-Input Data Selector/Multiplexer, Inverting Output 8-Input Multiplexer, 3-State	LS158	*4512	LS	16			
		LS251			16			
HC253 HC257	Dual 4-Input Multiplexer, 3-State Quad 2-Input Data Selector/Multiplexer, 3-State	LS253 LS257	*4539 *4519	LS/CMOS LS	16 16			
HC298	Quad 2-Input Multiplexer with Storage	LS298		LS	16			
HC354	8-Input Multiplexer, 3-State	LS354	*4512	LS	20			
HC356	8-Input Multiplexer, 3-State	LS356	*4512	LS	20			
HC4016	Quad Analog Switch		4016	CMOS	14			
HC4051	8-Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16			
HC4052	8-Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16			
HC4053	8-Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16			
HC4066	Quad Analog Switch	1-1/4 - 184	4066	CMOS	14			

High-Speed Device Number MC74/MC54		Func	LSTTL Device 74/54	1	Functional Equivalent CMOS Device LSTTL Device 74/54 CDXXXX Direct Pir Compatibili					
	_	OG AND DIG		ntinued)			ATTIBLE DEV	1		
★HC4316		nalog Switch		*4016				88016		
★HC4351	Quad A	with Level Translator Quad Analog Multiplexer/Demulti			ver/Line Rec	Octal Bu	048018			
★HC4352	Dual 4-0	with Latched Select Inputs Dual 4-Channel Analog Multiplexer/Demultiplexer with Latched Select Inputs Triple 2-Channel Analog			ver/Line Rec		81254			
★ HC4353	a with I				tch, 3-State		18			
20	8 Multip	olexer/Demulation	tiplexer		p, 3-State,		нсьва			
20	LS		LS573		tch, 3-State	ansparent Le		HC573		
		*4014 or 4021								
16										
					Octal Bus Transceiver, 3-State					
24										
								TURRUT		
		*4028					1-of-8 D			
								HCT241		
						a Transcelve				
								HC153		
		*4519								
						nput Data Seng Output				
		*4512								

1-22

8-Channel Analog

1

MOS GATE ARRAYS

Motorola is introducing a range of 3μ High-Density CMOS Gate Arrays, with gate counts from 600 to 6000 gates. 4 parts will be introduced in 1983 and 2 more in 1984.

Key features of the range are:

- System speed similar to LSTTL
- Low power consumption
- Option of CMOS or LSTTL compatible inputs
- Output drive capability of 10 LSTTL loads
- Simple design procedure

Design of the gate arrays is a very simple procedure, using the Motorola CAD system. This system has all of the design aids necessary for the designer to simulate his design, automatically place and route the circuit, complete an accurate timing analysis and prepare a test program for testing the finished product.

The CAD system is an improved version of the system which has been successfully used for several years for the design of Motorola ECL and TTL Macrocell Arrays. The same design system can be used for all three technologies. The designer needs no knowledge of I.C. design or computer programming to design a Motorola Gate Array.

The designer works in his own office using a simple printing terminal with Modem or acoustic coupler, and connects to the Motorola computer by dialling the nearest Motorola Sales Office. From here, connection to the Motorola computer in Phoenix, Arizona, is over the Motorola worldwide communications network.

Using a comprehensive library of SSI and MSI functions, the designer describes his circuit as a list of functions and interconnections which then becomes the input to the CAD system.

Future plans include the addition of analog and memory functions, and using a 2μ HCMOS process which will increase speed.

For further information on the Motorola range of CMOS, TTL and ECL Arrays, contact your nearest Motorola Sales Office.

mos care arrays

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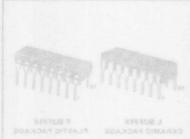
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Data Sheets and maintains PCT out, and maintains

- Low Dynamic Power Dissipation 70 µW Typical ® fg = 10 kHz.
- - · Pin-for-Pin Replacement for CD40468





advised that normal precautions be taken to avoid application of any voltage higher



MC14046B

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs. PCAin and PCBin. Input PCAin can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1_{Out}, and maintains 900 phase shift at the center frequency between PCAin and PCBin signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals PC2_{Out} and PCP_{Out}, and maintains a 00 phase shift between PCAin and PCBin signals (duty cycle is immaterial). The linear VCO produces an output signal VCOout whose frequency is determined by the voltage of input VCOin and the capacitor and resistors connected to pins C1A. C1R. R1, and R2. The source-follower output SFout with an external resistor is used where the VCO in signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

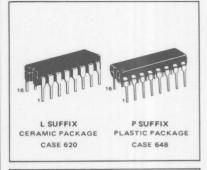
Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- VCO Frequency = 1.4 MHz Typical @ VDD = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/OC Typical
 VDD = 10 Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation 70 μ W Typical @ f₀ = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 M Ω , R2 = ∞ , RSF = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

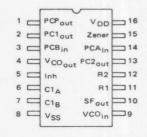
CMOS MSI

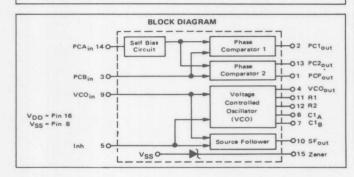
(LOW-POWER COMPLEMENTARY MOS)

PHASE-LOCKED LOOP



PIN ASSIGNMENT





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range AL Device CL/CP Device	ТА	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

	V _{DD} .		ow*	25°C T _h					
Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
VOL	5.0	308	0.05		0	0.05	Charac	0.05	Vdc
00	10	-	0.05	-	0	0.05	-	0.05	R tob
1 1	15	<u>5.0</u>	0.05	-	0	0.05	0+200	0.05	HUTT
Vou	5.0	4.95	_	4.95	5.0	80.6	4.05	10/201_E-11	Vdc
*OH	7.17	1000		1000000				glan J. f)	HUT
						_			ST June
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-		55 or 21		-			-	-	μAdc
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	-								
IDD			2000	-	1000000		-	150	μAdo
					S2000				(00A)
	15	0.L	20	-	0.015	20	-	600	
IDD	5.0	-	20	-	0:005	20	-	150	μAdo
	10		40	-	0.010	40	4 0E.D t	300	(VCO)
	15		80	-	0.015	80	· 2 60 V	600	1,000
IT	5.0	er i		IT = (1	.46 µA/kHz	f+ Ipp	A 00'S F	A 09'L = 1	μAdo
	10			IT = (2	2.91 µA/kHz	f + IDD			0 R360
63	15	-		IT = (4	.37 µA/kHz) f + IDD			loV ier
	VOL VOH VOH VIL VIH VIH VION VOH VIC VIH VIN VIH VIN VIH VIN VIN VIN VIH VIN	VOL 5.0 10 15 VOH 5.0 10 15 VOH 5.0 10 15 VIL 5.0 10 15 I VIH 5.0 10 15 I OH 5.0 10 10 10 10 10 10 10 10 10 10 10 10 10	VOL 5.0 - 10 - 15 - 10 - 15 - 10 - 15 - 15 - 1	VOL 5.0 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.05 10 - 0.02 10 - 0.02 10 - 0.02 15 - 1.8 - 10 10 - 0.62 15 - 1.8 - 10 10 - 0.62 15 - 1.8 - 10 10 - 0.62 15 - 1.8 - 10 10 - 0.62 15 - 1.4 - 10 10 - 0.5 10 - 0.0 10 -	VOL 5.0 - 0.05 -	VOL 5.0	VOL 5.0	VOL 5.0 - 0.05 - 0 0	VOL 5.0

[†]To Calculate Total Current in General:

$$\begin{split} &I_{T}\approx 2.2\times V_{DD} \ \left(\frac{\text{VCO}_{in}-1.65}{\text{R1}} + \frac{\text{V}_{DD}-1.35}{\text{R2}}\right)^{3/4} \ + \ 1.6\times \left(\frac{\text{VCO}_{in}-1.65}{\text{R}_{SF}}\right)^{3/4} + 1\times 10^{-3} \, (\text{C}_{L}+9) \, \text{V}_{DD} \, \, \text{f} + \\ &1\times 10^{-1} \, \text{V}_{DD}^{2} \left(\frac{100\cdot \% \, \text{Duty Cycle of PCA}_{in}}{100}\right) + I_{Q} \\ &\qquad \qquad \text{where: } I_{T} \, \text{in } \mu\text{A, C}_{L} \, \text{in pF, VCO}_{in}, \, \text{V}_{DD} \, \text{in Vdc, f in KHz, and} \\ &\qquad \qquad \text{R1, R2, R}_{SF} \, \text{in M}\Omega, \, \text{C}_{L} \, \text{on VCO}_{out}. \end{split}$$

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

26°00 Thinh°			1	7]	Minimum			Maximum		
Characteristic			Symbol	V _{DD} Vdc	AL Device	CL/CP Device	Typical All Types	AL Device	CL/CP Device	Units
Output Rise Time	0		ITLH		10	30			January .	ns
tTLH = (3.0 ns/pF) CL + 30 ns			80.0	5.0	20	-	180	350	400	
tTLH = (1.5 ns/pF) C1 + 15 ns				10	0.7	100 Tr	90	150	200	
tTLH = (1.1 ns/pF) CL + 10 ns				15	07	ROV	65	110	160	1.0
Output Fall Time	16	14.88	THL	74.95	16					ns
tTHL = (1.5 ns/pF) CL + 25 ns				5.0		JIV.	100	175	200	/ Jugol
tTHL = (0.75 ns/pF) CL + 12.5 ns			1.5	10	0.0	-	50	75	100	5.1/3
tTHL = (0.55 ns/pF) CL + 9.5 ns			2.0	15	07	-	37	55	80	5.071
PHASE COMPARATORS 1 and 2	6.76	-	0.34		-18		No.	.5 Vde)	13.5 or 1	0.90
Input Resistance - PCA _{in}			Rin	5.0	1.0	1.0	2.0		1	MΩ
			- in	10	0.2	0.2	0.4		A 10 0.0 ×	OV)
			1 -	15	0.1	0.1	0.2	(B)(A)	1.0 or 9	DA9
- PCB _{in}			Rin	15	150	15	1500	(30 V 0:	1 10 6 1	Ms
Minimum Input Sensitivity			Vin	5.0		110	200	300	400	mV p-
AC Coupled - PCAin			Vin	10	5.0		400	600	800	Lucy D.
C series = 1000 pF, f = 50 kHz				15	5.0		700	1050	1400	DV3
		8.1-		5 to 15	- 81	1				- 101
DC Coupled PCA _{in} , PCB _{in} VOLTAGE CONTROLLED OSCILLATOR (VCO)			-	18.0	0.8		See Noise Immunity			2.63
	JR (VCO)	6.7		_		301	700	10	50 V P.O.S.	P. AN.
Maximum Frequency			fmax	5.0	0.50	0.35	0.70	-	= 1,5 Vd	MHz
(VCO _{in} = V _{DD} . C1 = 50 pF,				10	1.0	0.7	1.4	O(JQ) III	mwD.evinG	THEODING:
R1 = 5 kΩ, and R2 = ∞)		- 80		15	1.4	1.0	1.9			
Temperature Frequency Stability				5.0	0.8	-	0.12	- 1	DV 83 - 1	%/°C
(R2 = ∞) E.O-			-	10	OT	-	0.04	- 6	+9.5 Ve	59)
Linearity (R2 = ∞)	- 3.5	-0.1		15	- 05	-	0.015	100	2 0.01	%
(VCO _{in} = 2.50 V ± 0.30 V, R1 > 10	0880			5.0	5.0	Jol	1 30	2 1	DV A0=	76
$(VCO_{in} = 5.00 \text{ V} \pm 2.50 \text{ V}, R1 \ge 400 \text{ k}\Omega)$		- 1	10	5.0 10 16		1	- 1	= 0.5 Vdc	(Vo	
(VCO _{in} = 7.50 V ± 5.00 V, R1 ≥ 1000 kΩ)		- 1	15	16		i	- 1	- 1.5 Vdc	OV)	
Output Duty Cycle	0 1027		100	5 to 15		100	50	Taurence	JAF HIER	%
Input Resistance - VCO in	10000-01		P	15	150	50	1500	WINES TO	2-21 20 97 11	Msz
	-0.0		R _{in}	15	150	50	1500		WOTHER TO SERVICE	10125
SOURCE-FOLLOWER									10	UI
Offset Voltage			0.8	5.0	0.8	agr	1.65	2.2	2.5	Vdc
(VCO _{in} minus SF _{out} , R _{SF} > 500 ks			10:	10	01		1.65	2.2	2.5	1993
20 - 600	0.016		20	15	35	-	1.65	2.2	2.5	riet)
Linearity oar oc	809.0	1	20	- 1	5.0	DO	(gaive	CLICR D	it Curent	%
(VCO _{in} = 2.50 V ± 0.30 V, R _{SF} > 50			GP .	5.0	00		0.1	-	Pacifige)	10/31
(VCO _{in} = 5.00 V ± 2.50 V, R _{SF} > 50			08	10	ar	-	0.6	CONTRACTOR AS	"T" and PE	e dall
(VCO _{in} = 7.50 V ± 5.00 V, R _{SF} > 50	ι κΩ)	the et		15	0.5	71-	0.8	71.70	mui7 visc	E listo?
ZENER DIODE	HNAM TE	17 = 12.			10	,	.34 02 ·	0 kHz, C)	1-01,00	- Hotel
Zener Voltage (I _Z = 50 μA)	37 giA/kH	V) = 41	٧z	-	6.7	6.3	7.0	7.3	7.7	Vdc
Dynamic Resistance (I _Z = 1 mA)			RZ			-	100	-	respirate Asin	Ω
* The formulae given are for the typic	cal charac	teristics					Ce, +85°C 1 worst-use			
					ic min @ \ ic min @ \	1 - 1.0 Vu 2.0 Vd				

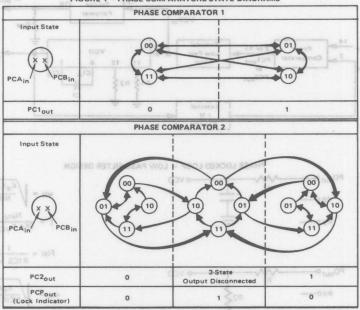
 $\begin{array}{lll} F_{1}=2.2\times V_{DD}& \frac{(VC)_{(1)}-1.65}{R1}+\frac{V_{DO}-1.35}{R2} \\ & +1.6\times \frac{(VC)_{(1)}-1.85}{R_{SF}}+1\times 10^{-3}\,(C_{L}+9)\,V_{DD}\,\,1+\frac{1}{10}\,(C_{L}+9)\,V_{D$

To Calculate Total Current in General:

Note: for further information, see:

(1) F. Gardner, "Prase-Lock Techniques", John Wiley and Soo, New York, 1956.
(2) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN 535, Morarola Inc.



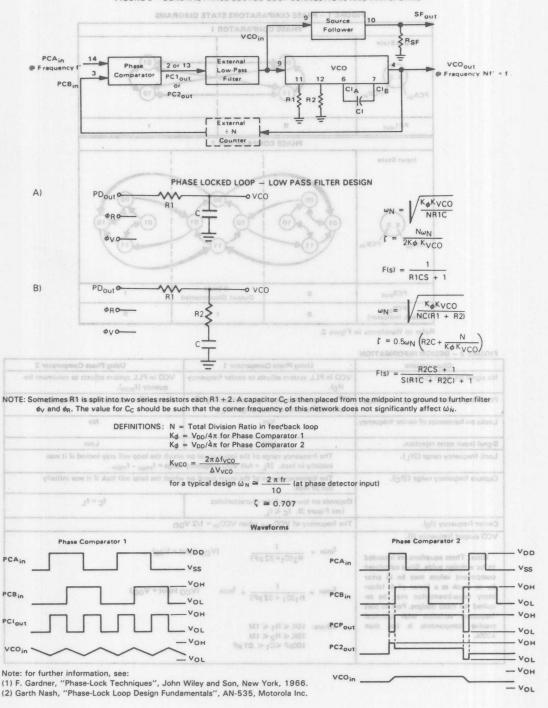


Refer to Waveforms in Figure 3.

FIGURE 2 - DESIGN INFORMATION

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2					
No signal on input PCA _{in} .	VCO in PLL system adjusts to center frequency (f ₀).	VCO in PLL system adjusts to minimum frequency (f _{min}).					
Phase angle between PCA in and PCB in.	90° at center frequency (f ₀), approaching 0° and 180° at ends of lock range (2f _L).	Always 00 in lock (positive rising edges).					
Locks on harmonics of center frequency.	Yes quoi son Retion Retion of the Company of the North Company of the Plant of the	ON DEPUNITIONS: N					
Signal input noise rejection.	VoolAn for Phase Chight arator 2	Low					
Lock frequency range (2f _L).	The frequency range of the input signal on initially in lock. 2f _L = full VCO frequency						
Capture frequency range (2f _C).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.						
	Depends on low-pass filter characteristics (see Figure 3). f _C ≤ f _L	fC = fL					
Center frequency (f ₀).	The frequency of VCO _{out} , when VCO _{in} = 1/2 V _{DD}						
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is less than ±20%.	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \qquad (V_{CO} \text{ inpropersist})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \qquad (V_{CO} \text{ inpropersist})$ $Where: 10K < R_1 < 1M$ $10K < R_2 < 1M$ $100pF < C_1 < .01 \mu F$	O input = VDD)					

FIGURE 3 - GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS





BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

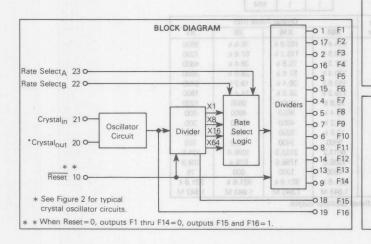
A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21
- Internal Pullup Resistor on Reset Input

MAXIMUM RATINGS (Voltages referenced to Vss. Pin 12.)

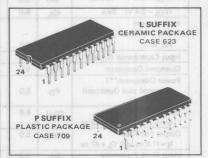
Rating	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	5.25 to -0.5	V
Input Voltage, All Inputs	V _{in}	V _{DD} +0.5 to V _{SS} -0.5	٧
DC Current Drain per Pin		10	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

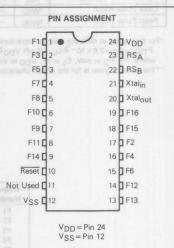


CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in})$ or $V_{out} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

DS-9386-R2

ELECTRICAL CHARACTERISTICS

		VDD	- 4	40°C	25°C			+8	5°C	Linia
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	x Unit
Supply Voltage	VDD	-	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level		5.0	-	0.05	-	0	0.05	_	0.05	V
"1" Level	Vout	5.0	4.95	_	4.95	5.0	ATE_GEN	4.95	-	٧
Input Voltage	WO 9 WO	3)		lomentary	with comp	batourrand	erator is c	nate ger	CLASTI E	The
$(V_0 = 4.5 \text{ or } 0.5 \text{ V})$	VIL	5.0	-	1.5	h yoneup	2.25	1.5	a ebom ti	1.5	a aVon
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$	VIH	5.0	3.5	-	3.5	2.75	e of o urge	3.5	pro v ide a	Vov
Output Drive Current			11	A phowis	n erb rol s	flock source		fled oscilla	stal contro	no A
(V _{OH} = 2.5 V) Source	ІОН	5.0	-0.23	put dock	-0.20	1.7	to select of	-0.16	ai aanliba	mA
(V _{OL} = 0.4 V) Sink	IOL	5.0	0.23	-	0.20	0.78		0.16	-	mA
Input Current Pins 21, 22, 23	lin	-	-	± 0.1	und "sien	± 0.00001	±0.1	cations n	±1.0	μΑ
Pin 10		5.0	-	_	- 1.5	-	-7.5	DE TABLE I	ALLE DE	μΑ
Input Capacitance (Vin = 0)	Cin	17-2	-	-	-	5.0	ddnp lawr	1 100 0 711	00 V V V V	pF
Quiescent Dissipation	PQ	5.0	-	2.5	50PO_17 Y	0.015	2.5	IDJEVIO 10	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C _L = 15 pF)	PD	5.0		te Retes	P _D = (7	7.5 mW/MHz) f+PQ	ny Cycle Time Base	Output Di ammable	mW
Output Rise Time** $t_{\Gamma} = (3.0 \text{ ns/pF}) \text{ CL} + 25 \text{ ns}$	× TLHa	5.0	-	-	-111	70	200	ts, Cempa	red-Outpu	ns i
Output Fall Time** tf = (1.5 ns/pF) CL + 47 ns	edTHE.	5.0	-	-	-	70	200	I-IIA no n	Projection	ns
Input Clock Frequency	fCL	5.0	-	1.85	-	-13.0	1.85	T DO YOU	1.85	MHz
Clock Pulse Width	tW(C)	_	200	-	200	- 19	gett toggatt f	200	Mrs. 1 1111	ns
Reset Pulse Width	tW(R)	_	500	_	500	_	_	500	_	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula: $P_T(C_L = P_D + 2.6 \times 10^{-3} (C_L - 15 \text{ pF}) \text{ V}_{DD}^2 f$

where: PT, PD in mW, CL in pF, VDD in Vdc, and f in MHz.

**The formula given is for the typical characteristics only.

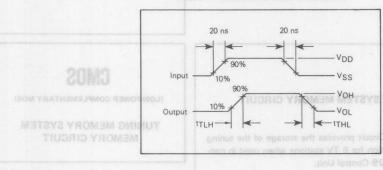
TABLE 1 - OUTPUT CLOCK RATES

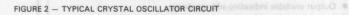
	Rate	Select	D
A	В	Α	Rate
3	0	0	- X1
3	0	+ 102	X8
	1	0	X16
	1	1	X64

Output	-	Output Ra	ites (Hz)	
Number	X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

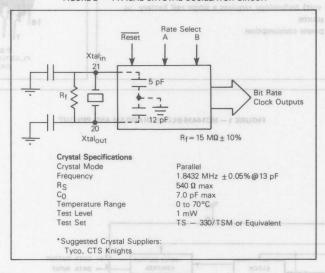
*F16 is buffered oscillator output.

FIGURE 1 - DYNAMIC SIGNAL WAVEFORMS





· Expansion of up to 32 channels possible without external logic



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

2

TUNING MEMORY SYSTEM MEMORY CIRCUIT

The MC14426 Memory Circuit provides the storage of the tuning voltage and band information for 8 TV stations when used in conjunction with the MC14429 Control Unit.

- 8 static shift registers of 14 bit length
- Expansion of up to 32 channels possible without external logic
- Output available indicating address change
- Low voltage (1 volt) technology requires a single cell battery as back up power source
- Extremely low power consumption

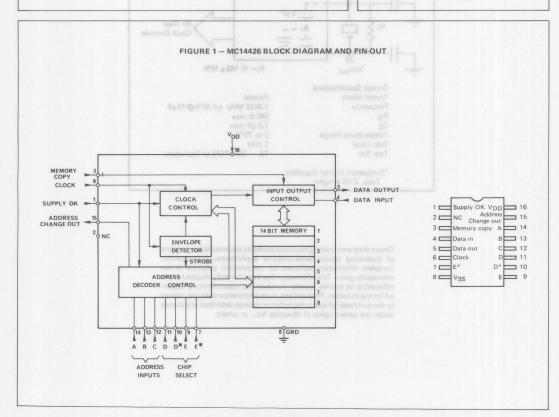
CMOS

(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM MEMORY CIRCUIT



P SUFFIX PLASTIC PACKAGE CASE 648



FILLINE 1 - DYNAMIC SIGNAL WAVEFORMS

MAXIMUM RATINGS (TA = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	+6 to -0.5	Vdc
Input Voltage, All inputs	Vin	V _{DD} to -0.5	Vdc
DC Current drain per pin	OK (pint	viqqua bab bataelea	mA
Operating Temperature Range	TA	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°c

ELECTRICAL CHARACTERISTICS (TA = 0 to 70 °C) Voltages referenced to VSS, pin 8

Characteristic		Symbol	Min.	Тур.	Max.	Unit
Operating Supply Voltage	several MC1/426	V _{DD}	4.0	5.2	6.0	Vdc
Standby Supply Voltage ¹		V _{DD}	1.2	1.5	6.0	Vdc
Quiescent Current	(V _{DD} = 1.5 V)	IDD	ny copy inf	0.008	2.0	μAdc
0 0 0 0 8 011	(V _{DD} = 5 V)	nsfer line	trial data tra	0.5	15.0	pin 3 inp
Input Voltage	(V _{DD} = 5 V)	VIL	T boineg pri	circuit duri	0.5	Vdc
17 10 24 0 0 1 1		VIH	4.5			
Input Voltage	(V _{DD} = 5 V)	Vii	rolled by co	nput is con	1.0	Vdc
None – Any other combination		VIH	4.0	which in t	s (ground),	S A of E
Input Current all Inputs Except Pin 3.	(V _{DD} = 5 V)	rdINger:	COURT OF THE PERSON NAMED IN	ntenotri in	nater the co	pAdc
Input Current ²	(V _{DD} = 5 V)	IIN	-1.5	-3.0	-6.0	μAdc
Input Capacitance all Inputs	(V _{IN} = 0 V)	CIN		5.0	12.0	pF
Output Current all Outputs (sinking)	(V _{OL} = 0.4 V)	lOL	0.4	ther than fi	d station ra	mAdc
Three State Output	ternal decoding.	ITL			-177.138	μА
Leakage Current (sinking)	$(V_{DD} = 5 V)$	different		±0.001	±5.0	r ygoo o'l
Clock Input Frequency	(V _{DD} = 5 V)	f _{max} .	400	700	ar philmana	kHz
	ADDRESS CHAN	fmin.		25	100	

¹ Standby mode is obtained by lowering Supply OK input to V_{SS} during a few read/write cycles. V_{DD} can then be lowered to its standby value, Pin 1 staying low.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

In Standby mode no read/write operation can be performed.

² An internal pull-up resistor is present on pin 3.

INPUT/OUTPUT FUNCTIONS: - AT SOMITAR MUMIXAM

DATA IN/OUT — The input/output control section provides the interface between the memory and the control circuit MC14429 via pins 5 and 4. The output network is active only when the chip is selected and supply OK (pin 1) is at 1. The relationship between clock and input/output signals is shown below:

ADDRESS INPUTS — To select the 8 memory words only three A, B, C address bits are required. (pins 14, 13, 12.)

CLOCK IN

DATA IN

ASSUMING
1010...

DATA OUT
ASSUMING
1010...

DATA OUT
ASSUMING
1010...

Internal
Delay
(20µS)

---- If memory copy is activated

It should be noted that the memory copy information on pin 3 input is inserted into the serial data transfer line which goes to the control circuit during period T₂.

MEMORY COPY — This input is controlled by connecting pin 3 to VSS (ground), which in turn holds down the memory output signal during period T2. This function allows to transfer the content of the 14 bit shift register of the control circuit MC14429 into any memory location as long as this command is present.

- To resume search for a TV station starting from the last selected station rather than from a random tuning voltage.
- To copy the content of a shift register into a different location. This permits to change the order of TV programs according to the user wish.

SUPPLY OK - In case of power failure this input (pin 1) is used to deactivate all functions of the chip so that no data is lost, rpovided that V_{DD} is held at 1 volt minimum. (See note 1.)

The supply OK signal is enabled in such a way that deactivation during transfer of information is prevented.

CHIP SELECT — To facilitate the parallel connection of several MC14426 memory circuits, four additional inputs D, D*, E, E* are provided for chip select.

The truth table of chip select inputs is given below.

Chip Selected	Channel	D	D*	E	E*
/8=010V)	1 to 8	0	0	0	0
2.	9 to 16	1	1,,,,,	0	0
3	17 to 24	0	0	1	- 1
4	24 to 32	1	1	1	1
None	-	Any other combination			tion

 D^{\ast} and E^{\ast} are programming inputs of the chip select network and are normally connected to VSS or VDD. The logic levels on these inputs specify the levels of the D and E inputs for chip selection.

The chip is selected if $D = D^*$ and $E = E^*$

As shown in the above truth table up to four circuits (32 channels) can be connected in parallel without external decoding.

CLOCK IN - (pin 6) See MC14429 data sheet.

ADDRESS CHANGE — An additional function (pin 15) is available to mute the sound section of the TV set during each address change. The 400msec. one-shot on the control circuit (MC14429) provides this feature. This one-shot is triggered by the address change signal supplied by the memory circuit. If the address is changed, the AC signal appears on the leading edge of the internal strobe pulse and lasts one (T1+T2) cycle.

2-12

NC14429



TUNING MEMORY SYSTEM CONTROL CIRCUIT

The MC14429PB control circuit will perform the following functions when used in conjunction with the MC14426 Memory and the UAA1008A/C Linear Processors:

- LC Clock generator
- Underflow protected UP/DOWN Counter providing information for memory
- Rate multiplier for D/A conversion
- Shift register for memory data access and storage of new data
- . 2.3 or 4 TV band counter with automatic or manual switching
- Control section for automatic or manual TV station search
- Automatic volume muting control during each search and programme change

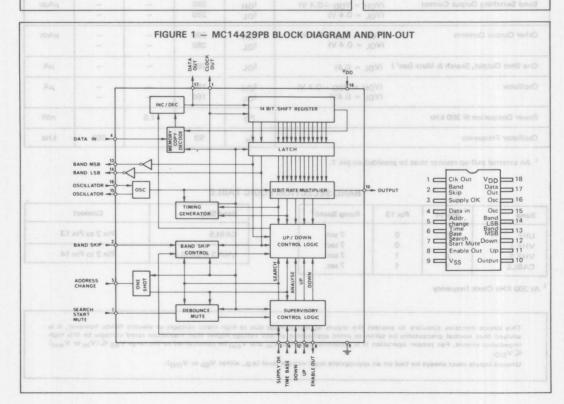
CMOS

(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM CONTROL CIRCUIT



PB SUFFIX
PLASTIC PACKAGE
CASE 707



A

MOTOROLA

MAXIMUM RATINGS (TA = 25 °C)

Rating	Symbol	Value	Unit
OC Supply Voltage	V _{DD}	+6 to -0.5	Vdc
Input Voltage, All inputs	Vin	V _{DD} to −0.5	Vdc
DC Current Drain per Pin	1	10	mA
Operating Temperature Range	TA	0 to +70	°c
Storage Temperature Range	T _{stg}	-65 to +150	°c

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ELECTRICAL CHARACTERISTICS (TA = 0 to 70 °C) Voltages referenced to VSS, pin 9

Charact	eristic	Symbol	Min.	Тур.	Max.	Unit
Power Supply Operating Range		V _{DD}	4.95	5.2	6	Vdc
Input Current, All Inputs (except pir	s 5, 7) gradeli	wadsuns (in 10 oi	emot <u>u</u> s ritir	10	or 4 TV ban	pAdd
Enable Output Current	$(V_{OH} = V_{DD} - 0.4 V)$ $(V_{OL} = 0.4 V)$	IOH	280 280	o meting c	omatie volun nme c hange	
Band Switching Output Current	$(V_{OH} = V_{DD} - 0.4 V)$ $(V_{OL} = 0.4 V)$	I _{OH}	280 280	-	-	μAdo
Other Output Currents	$(V_{OH} = V_{DD} - 0.4 V)$ $(V_{OL} = 0.4 V)$	IOL STOR	280 280	_ FIGU	-	μAdd
One Shot Output, Search & Mute (se	e^{1}) (V _{OL} = 0.4)	lor	280	-	-	μΑ
Oscillator	$(V_{OH} = V_{DD} - 0.4 V)$ $(V_{OL} = 0.4 V)$	IOH IOL	160 160	egrose T	1 -	μΑ
Power Dissipation @ 300 kHz		PD		7.5		mW
Oscillator Frequency	10000000	fo	50	8	350	kHz

¹ An external pull-up resistor must be provided on pin 7.

BAND SELECTION LOGIC TABLE

Band	Pin 14	Pin 13	Ramp Speed ¹
UHF	0	0	7 sec.
VHF 1	ampy tamis	0	7 sec.
VHF3	O O	1	7 sec.
CABLE	22 1	1	7 sec.

Band Skip	Connect
CABLE	Pin 2 to Pin 13
VHF 3 & CABLE	Pin 2 to Pin 14

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

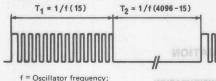
Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

¹ At 300 KHz Clock frequency

will interact with the system by stopping th ZNOITONUT TUPTUO/TUPNIE - Refer to band selection logic table for

CLOCK OUT - Clock pulses (PIN 1) control the transfer of data between the MC14429A control chip and the MC14426 memory chip via pins 4 and 17. For best system performance the oscillator circuit should generate a pulse train of approximately 300 KHz, however frequency value is not critical.

The clock out signal timing is shown below.



T₁ + T₂ = Rate Multiplier;

T₁ = Shift Cycle.

BRM OUTPUT - The binary rate multiplier output is available on pin 10.

The binary word cycle is approximately 13 msec for a clock frequency of 300 KHz (3.3 µsec pulse width). The output provides pulses symmetrically spaced to facilitate the filtering when doing D/A conversion.

In the block diagram of Figure 1, the least significant bit is to the right. Bits 13 and 14 represent band information, therefore overflow of the rate multiplier control word automatically increments band information.

SEARCH & MUTE - Search mode is initiated by presenting a 0 on pin 7. For trouble free operation the signal on pin 7 is debounced internally on both edges for 13 msec. As soon as search is initiated and the debounce cycle is terminated this pin becomes an output for the mute signal which is available during the whole cycle. The search cycle ends when a valid station is found and the one shot (R/C on pin 5) has timed out. The mute signal is available also at address change and during any other time the one shot is active. Each time the oneshot is reset the mute output will momentarily go to high and back to low for less than 13 msec. It is therefore recommended to introduce a proper time constant on this line to smooth out the mute function.

Mute is also provided when supply OK input (pin 3) is VSS.

Two ramp modes are present:

- 1. Search mode, with a rate of change of 8 steps per clock cycle and a scan time of 7 seconds.
- 2. Tracking mode, used for manual search or normal locked on conditions, with a rate of change of 1 step per clock cycle and a scan time of 56 seconds.

Search mode is terminated by the simultaneous presence of a 1 on both inputs UP (pin 11) and DOWN (pin 12).

SUPPLY OK - An input (pin 3) is provided to ensure that during power failures, flash-overs, low supply voltages, etc... no memory information can be modified or lost. In operating conditions it should receive a 1 from the linear processor UAA1008A. When at 0 the Search FF, analyse FF and Band skip FF are all reset. The UP/DOWN control logic is not inhibited and a 1 on the UP or DOWN inputs still could modify the content of the

However, due to the fact that the memory circuit does not send any information when Supply OK is at 0, no data can be modified. It is blow lesight of all agneds base

TIME BASE - This input (pin 6) receives a 1 whenever coincidence between fly-back and video sync signals has been detected by the linear processor circuit UAA1008A. In the search mode the presence of a 1 on pin 6 is checked by the analyse flip-flop set by the one shot. If time base information is present before the one shot is timed out (usually 400 msec. from ramp stop) the analyse FF is reset, search/mute ends and a stable situation reached. Should time base be 0 when the one shot times out,

search will resume If in Memory/Normal mode, the presence of a 1 on pin 6 will force Enable Out to low, if at 0 Enable Out will go to

the tristate condition. ENABLE OUT - This output (pin 8) is used to control the AFC OUT gate and UP/DOWN overlap in the linear

processor circuit UAA1008A. Its truth-table is the following:

Search FF (internal)	Analyse FF (internal)	Time Base IN (PIN 6)	(PIN 8)
0	0	0	Tristate
0	0	1	0
0	1	0	0
0	1	1	0
1	×	X	1
0	0	X	Tristate

X : Don't care

- The first line of the truth table indicates that the system is in its memory mode and that no TV station is received
- The second line indicates that a valid TV station is received and system is in its normal memory mode.
- The third line shows the states during the "oneshot" period, e.g. the search function has been interrupted temporarily and waits for Time Base signal.
- The fourth line is as above but Time Base is present.
- The fifth line represents Search mode, the search FF is set and enable out is forced to 1.
- The sixth line represents Address Change, enable out goes tristate during the on time of the one shot.

UP & DOWN - These two inputs (pin 11 & 12) have two modes of operation.

When the system is in search, only the simultaneous presence of an UP and a DOWN signal, both of them at 1, will interact with the system by stopping the search ramp. A 1 on only one of the two inputs does not stop search nor reduce search speed. Logic has been included to improve the "Stop process" by making it independent of the up and down width when both at 1.

When the circuit is not in search, a 1 on the UP or DOWN inputs results in adding or subtracting a one to or from the content of the 14 bit shift register during each rate multiplier cycle. Built-in underflow protection prevents a band change if the digital word is zero and a DOWN command is initiated.

will interact with the system by stopping the search ramp.

A 1 on only one of the two inputs does not stop search output code. (pin 13 MSB, pin 14 LSB).

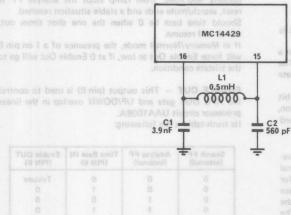
A maximum of four bands are available. Three or two bands only can be obtained by connecting pin 2 to pin 13 or 14 as per band selection logic table.

Note that no debounce network is included on pin 2 input. Therefore, if manual band skip is required, provision for a bounce-free input signal has to be made.

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CMOS

(LOW POWER COMPLEMENTARY MOS)

INPUT ADDRESS ENCODER

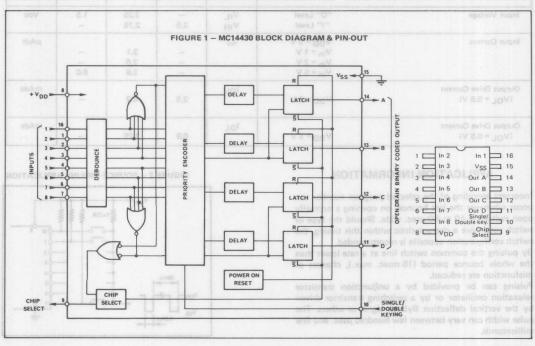
INPUT ADDRESS ENCODER

The MC14430 is an integrated circuit designed for program selection address in TV and radio receivers by means of push button switches.

- 8 program inputs aparlov yns to noiteologs blove at nexts ed and
 - Binary coded open drain latched output
 - Push button type keyboard allows for electrical isolation in live of chassis applications
 - Single or double keying operation possible
 - Up to four circuits can be cascaded
 - Normally closed or normally open switches can be used.



P SUFFIX
PLASTIC PACKAGE
CASE 648



E-049 - May 1979



MOTOROLA

MAXIMUM RATINGS (TA = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	+10 to -0.5	Vdc
Input Voltage, All Inputs	Vin	V _{DD} to −0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range	TA	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

ELECTRICAL CHARACTERISTICS (TA = 0 to 70 °C)

XIAUR 9 Characteristics		Symbol	Min.	Тур.	Max.	Unit
Operating Supply Voltage		V _{DD}	4	5.2	6	Vdc
Quiescent Current per Package (Pins 16,1,2, 3,4,5,6,7 open or grounded)	V _{DD} = 5 V	IDD	_	0.068	10	μAdd
Input Voltage	"O" Level	VIL VIH	- 3.5	2.25 2.75	1.5	Vdc
Input Current TUG-I	V _{DD} = 5 V V _{in} = 1 V V _{in} = 2 V V _{in} = 5 V	l _{in}	PIGURE -	2.1 2.6 2.6	6.0	μAdd
Output Drive Current (V _{OL} = 0.5 V)	V _{DD} = 5 V	loL	2.5	6.2	= 10	mAd
Output Drive Current (VOL = 0.5 V)	V _{DD} = 5 V	loL	0.9	2.25		mAd

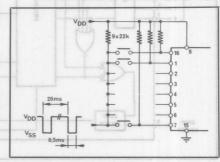
APPLICATION INFORMATION

Incorrect encoding of the selected program number can occur whenever the last bounce, on opening a normally open switch, is 40 to 60 µsec. wide. Should the type of switch used have a characteristic within this timing, the switch configuration opposite is recommended.

By pulsing the common switch line at a rate lower than the whole bounce period (15 msec. max.), chances of misfunction are reduced.

Pulsing can be provided by a unijunction transistor relaxation oscillator or by a switching transistor driven by the vertical deflection flyback signal or others. The pulse width can vary between few hundred µsec. and few milliseconds.

FIGURE 2 - BOUNCE IMMUNE APPLICATION



APPLICATION INFORMATION

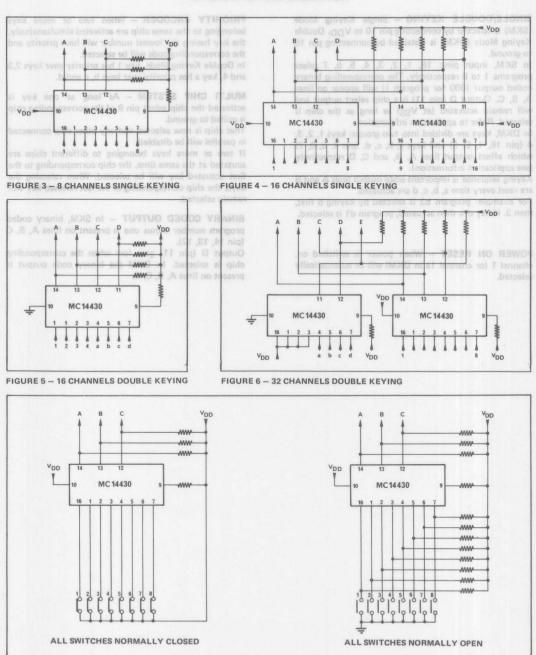


FIGURE 7 - PUSH BUTTON ELECTRICAL DIAGRAM

INPUT/OUTPUT FUNCTIONS

SINGLE/DOUBLE KEYING — Single Keying Mode (SKM) is selected by connecting pin 10 to V_{DD}. Double Keying Mode (DKM) is obtained by connecting pin 10 to ground.

In SKM, input pins: 16, 1, 2, 3, 4, 5, 6, 7 select programs 1 to 8 respectively. The corresponding binary coded output (000 for program 1) will appear on lines A, B, C. Output D (pin 11) is a chip select output and will remain activated (at VSS) as long as the chip is selected. Refer to application information.

In DKM, keys are divided into two groups: keys 1, 2, 3, 4 (pin 16, 1, 2, 3) and keys a, b, c, d, (pin 4, 5, 6, 7) which affect output lines A, B, and C, D respectively (see application information).

Keying sequence is important since output lines A and B are reset every time a, b, c, d are actuated.

For example: program b3 is selected by keying b first, then 3. If key d is then actuated, program d1 is selected.

POWER ON RESET — When power is switched on, channel 1 (or channel 1a in DKM) will be automatically selected.

PRIORITY ENCODER — When two or more keys belonging to the same chip are activated simultaneously, the key having the lowest number will have priority and the corresponding code will be selected.

In Double Keying Mode, key 1 has priority over keys 2,3 and 4, key a has priority over keys b, c and d.

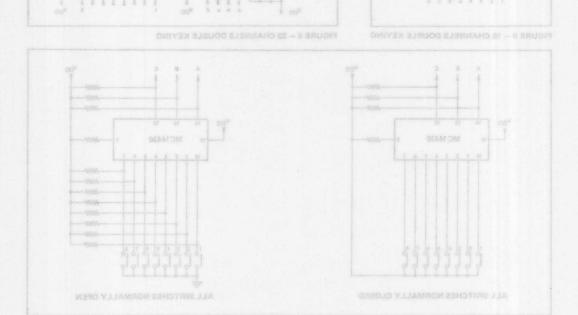
MULTI CHIP SYSTEM — As long as one key is activated the chip select pin 9 of the corresponding chip is pulled to ground.

That chip is now selected and any other chip connected in parallel will be disabled.

If two or more keys belonging to different chips are acutated at the same time, the chip corresponding to the first actuated key will be selected. When releasing the keys, the chip corresponding to the last released key will remain selected.

BINARY CODED OUTPUT — In SKM, binary coded program number minus one is present on lines A, B, C (pin 14, 13, 12).

Output D (pin 11) goes low when the corresponding chip is selected. In DKM the binary code output is present on lines A, B, C, D.





3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

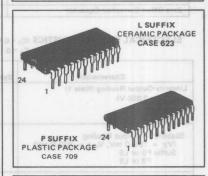
The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

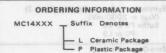
- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs—Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW typical @ ±5.0 V
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
 Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count
- See also Application Notes AN-769 and AN-770

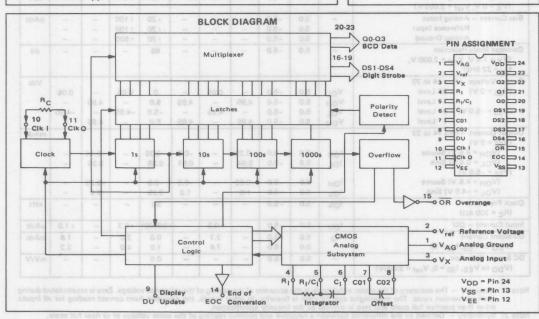
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3½ DIGIT A/D CONVERTER









MAYIMIM PATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD} to V _{EE}	-0.5 to +18	Vdc
Voltage, any pin, referenced to VEE	V	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10	mAdd
Operating Temperature Range	TANA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \le (V_{in})$ or $V_{out} \le V_{DD}$.

for ease of use with batteries, or with s

RECOMMENDED OPERATING CONDITIONS (VSS = 0 or VEE)

Parameter	Symbol	Value	Unit
DC Supply Voltage - VDD to Analog Ground	VDD	+5.0 to +8.0	Vdc
VEE to Analog Ground	VEE	-2.8 to -8.0	arlp
Clock Frequency	fClk	32 to 400	kHz
Zero Offset Correction Capacitor	Co	0.1±20%	μF

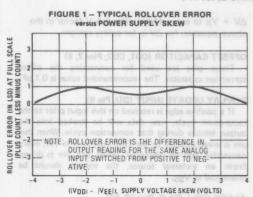
ELECTRICAL CHARACTERISTICS (C₁ = 0.1 μF mylar, R₁ = 470 kΩ @ V_{ref} = 2.000 V, R₁ = 27 kΩ @ V_{ref} = 200.0 mV, $C_0 = 0.1 \,\mu\text{F}$, $R_C = 300 \,\text{k}\Omega$; all voltages referenced to Analog Ground, pin 1.)

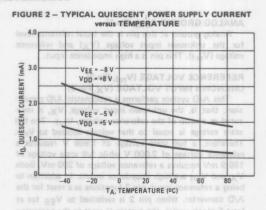
		VDD	VEE	-4	0°C	amože	25°C	o OlA	A 85	°C	scale
Characteristic	Symbol	Vdc	Vdc	Min	Max	Min	Тур	Max	Min	Max	Uni
Linearity-Output Reading (Note 1) (V _{ref} = 2.000 V)	-	5.0	-5.0	-	Vm 9.	-0.05	± 0.05		tage Ra Counve		%rd
(V _{ref} = 200.0 mV)		5.0	-5.0	-	-	-Count	± 0.05	+ Count	b M 00 s vaiss	in C ni	0
Stability — Output Reading (VX = 199.0 mV, V _{ref} = 200.0 mV) Suffix P5 or L5		5.0	-5.0	Low R	res Orra			2	Ucy La		
P9 or L9				v o.a.	9 Isol	gyt Wo	lock, or on: 8.0	3			
Symmetry — Output Reading (Note 2) (Vref = 2000 mV)		5.0	-5.0		V 0.8		nge Sign		bas a		LSI
Suffix P5 or L5 P9 or L9						its splays it	ng Circu LCD Ellent Int Cour	2 3	'n sastan		0 0 0
Zero-Output Reading (V _X = 0 V, V _{ref} = 2.000 V)	JE	5.0	-5.0	0774	A bas	892-1	0	0	ПодА	osla es	LSI
Bias Current - Analog Input	-	5.0	-5.0	рдіа	NOTO II	-	± 20	± 100	-	-	pAd
Reference Input	20-25	5.0	-5.0	-	-	-	± 20	± 100	-	-	
Analog Ground		5.0	-5.0 -5.0	-	_	-	± 20	± 500	_		dB
(V _X = 1.4 V, V _{ref} = 2.000 V, f _{oc} = 32 kHz)	21-81	3.0	-5.0	7600	Ngirigid		0.5				
Output Voltage - Pins 14 to 23	T	III			TI			TT			Vd
(V _{SS} = 0 V) "0" Level	VOL	5.0	-5.0 -5.0	4.95	0.05	4.95	5.0	0.05	4.95	0.05	, A
(V) FOV) "0" Lovel	VOL	5.0	-5.0	4.95	4.95	4.95	-5.0	-4.95	4.95	-4.95	in-
"1" Level	VOH	5.0	-5.0	4.95	-	4.95	5.0	-	4.95	17_	9.8
Output Current — Pins 14 to 23 (Vss = 0 V)	7 -		H	11,	H	4	1	44		2	mA
(V _{OH} = 4.6 V) Source (V _{OL} = 0.4 V) Sink	IOH	5.0 5.0	-5.0 -5.0	-0.25 0.64	- 10	-0.2 0.51	-0.36 0.88	et - -	-0.14 0.36	-	Gelo
(V _{SS} = -5.0 V) (V _{OH} = 4.5 V) Source	Іон	5.0	-5.0	-0.62	_ 1	-0.5	-0.9	1	-0.35	_	1
(VOL = -4.5 V) Sink	IOL	5.0	-5.0	1.6	7-	1.3	2.25	-	0.9	-	
Clock Frequency (R _C = 300 kΩ)	fClk	5.0	-5.0	-	-	-	66	-	-	-	kH
nput Current - DU	IDU	5.0	-5.0		± 0.3	-	± 0.00001	± 0.3	-	± 1.0	μΑσ
luiescent Current (VDD to VEE, ISS = 0)	Ia	5.0 8.0	-5.0 -8.0	-	3.7 7.4	cono l	0.9	2.0	-	1.6	mAd
OC Supply Rejection (VDD to VEE, ISS = 0, Vref = 2.000V)		5.0	-5.0	1-	-	-	0.5	4	-	-	mV.

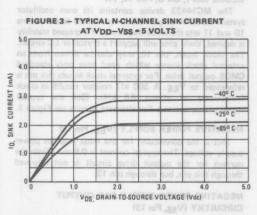
Note 1: Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

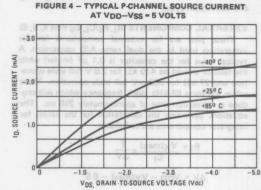
Note 2: Symmetry — Defined as the difference between a negative and positive reading of the same voltage at or near full scale.

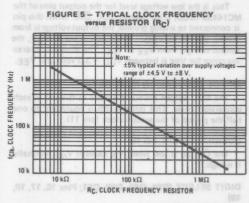
TYPICAL CHARACTERISTICS

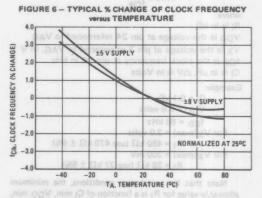












CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16,400} \pm 1.5\%$ MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$

DEVICE OPERATION

ANALOG GROUND (VAG, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}) . This pin is a high impedance input.

REFERENCE VOLTAGE (V_{ref}, Pin 2) UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, pin 2 functions as a reset for the A/D converter. When pin 2 is switched to V_{EE} for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (RI, RI/CI, CI; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is $0.1~\mu\text{F}$ (mylar) while the resistor should be 470 $k\Omega$ for 2.0 V full scale operation and 27 $k\Omega$ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_1 = \frac{V_X(max)}{C_1} \times \frac{T}{\Delta V}$$

 $\Delta V = V_{DD} - V_{X}(max) - 0.5$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

 R_I is in $k\Omega$

VDD is the voltage at pin 24 referenced to VAG VX is the voltage at pin 3 referenced to VAG, in V fClk is the clock frequency at pin 10 in kHz Cl is in μ F, Δ V is in Volts

Example:

 $C_I = 0.1 \mu F$ $V_{DD} = 5.0 \text{ volts}$ $f_{CIk} = 66 \text{ kHz}$ For $V_X(\text{max}) = 2.0 \text{ volts}$

 R_1 = 480 kΩ (use 470 kΩ ± 5%)

For $V_X(max) = 200 \text{ mV}$

 $R_1 = 28 k\Omega \text{ (use 27 } k\Omega \pm 5\%)$

Note that for worst case conditions, the minimum allowable value for R $_{I}$ is a function of C $_{I}$ min, V $_{DD}$ min, and f $_{CIk}$ max. The worst-case condition does not allow

 ΔV + V_X to exceed V_{DD} . The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (CO1, CO2; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is $0.1 \mu F$.

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to VSS.

CLOCK (CIk I, CIk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to VEE. A 300 k Ω resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (VEE, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through pin 13.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY (VSS, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, \overline{OR}). When this pin is connected to analog ground, the output voltage is from analog ground to VDD. When connected to VEE, the output swing is from VEE to VDD. The allowable operating range for VSS is between VDD - 3.0 volts and VEE.

END OF CONVERSION (EOC. Pin 14)

The EOC output produces a pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (pin 11).

OVERRANGE (OR. Pin 15)

The \overline{OR} pin is low when V_X exceeds V_{ref} . Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective

2

digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus, with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select ouptut and EOC signals is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the $\frac{1}{2}$ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (VDD, Pin 24)

The most positive supply voltage pin.

TRUTH TABLE

Coded Condition of MSD	03	Q2	Q1	00	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
-0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
-0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1) Hook up
-1	0	0	0	Q	0 → 1 only seg b
+1 OR	0	1	1	1	7 → 1 and c to
-1 OR	0	0	1	1	3 → 1 MSD

Notes for Truth Table

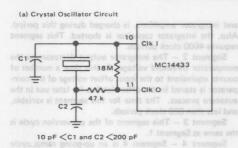
- Q3 1/2 digit, low for "1", high for "0"
- Q2 Polarity: "1" = positive, "0" = negative
- Q0 Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

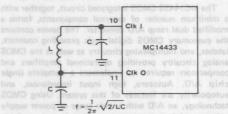
The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 - ALTERNATE OSCILLATOR CIRCUITS

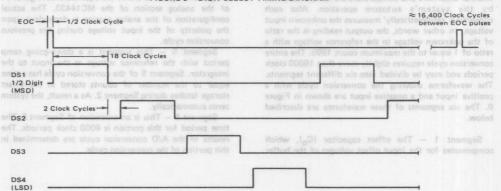


(b) LC Oscillator Circuit



For L = 5 mH and C = 0.01 µF, f ≅ 32 kHz

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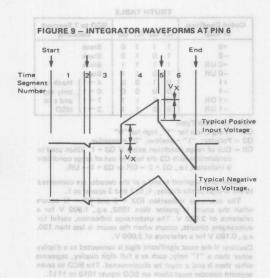
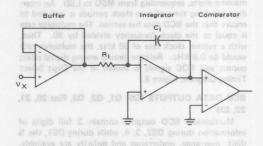


FIGURE 10 – EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 - The offset capacitor (C_0), which compensates for the input offset voltages of the buffer

and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

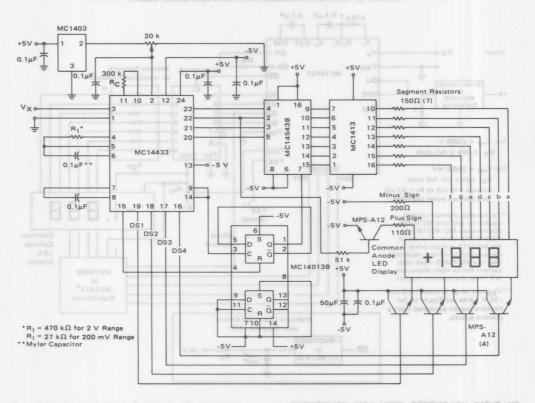
Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

FIGURE 11 - 3-1/2 DIGIT VOLTMETER-COMMON ANODE DISPLAYS, FLASHING OVERRANGE



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3½ DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using RC equal to 300 k Ω , the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to VEE via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and -5 V supplies is *not* required. See the recommended operating conditions and Figure 1, on pages 2 and 3.

470 k † 0.1 μF 0.1 μF C| C01 C02 RI/CI CIk Input 300 k CIk O VAG Resistor Network MC14511B MC14433 OR or Individual Resistors* DU Zener Diode R or MC1403 EOC 00 01 -Reference Vref 02 444 ~~ 03 +5 LT ~~ Vss Ŧ for V_{ref} = 2.000 V LE VDD ** VX: 1.999 V full scale VSS VDD VEE RDP for V_{ref} = 200.0 mV DS3 DS2 V_X: 199.9 mV full scale DS4 (change 470 k Ω to R_I = 27 k Ω RM and decimal point position) 88 VEF *To increase segment current (Minus) capability add two MC75491 ICs between MC14511B and Resistor Network. The use of Minus Common Control Cathode the MC1413 as digit driver LED increases digit current capability Display over the MC75492. Peak digit current for an eight displayed MC75492 is 7 times the segment current MC1413* **VEE can range between -2.8 and Digit Drivers -11 V. Also see Figure 18 for negative supply generated from a positive supply. Alternate Overrange Circuit with Separate LED

1/6MC75492

1/7 MC1413

OR

FIGURE 12 – 3% DIGIT VOLTMETER WITH LOW COMPONENT COUNT

3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC75492 or MC1413 provides sink for digit current. (The MC75492 or MC1413 are devices with 6 or 7 darlingtons respectively with common emitters.) The worst case digit current is 7 times the segment current at ½ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from VDD (+5 V) to ground and does not flow through the VEE (negative) supply. The minus sign is controlled by one section of the MC75492 or MC1413 and is turned off by shunting the current through RM to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor RDP. Since the brightness and the type and size of LED

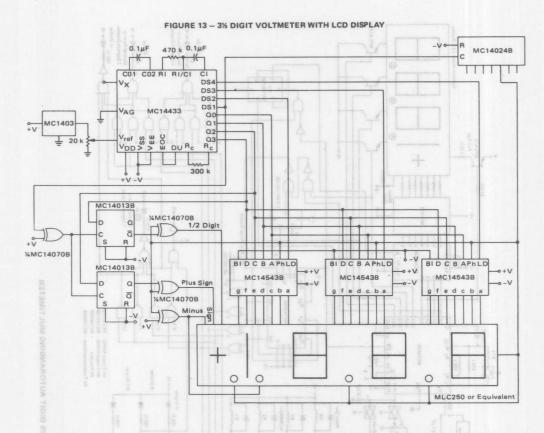
display are the choice of the designer, the values of resistors R, R_{M} , R_{DP} , and R_{R} that govern brightness are not given.

During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown. There are leftover sections in either the MC75492 or MC1413.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of



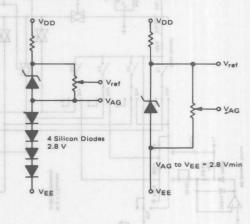
the LCD and to the individual segments through the combination of the output circuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when VSS is connected to VEE. In this case a level must be set for analog ground, VAG, which must be at least 2.8 V above VEE. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between VAG and VEE, leaving 6 V for VDD to VAG. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 – TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY



2-30

3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 k Ω to 2 M Ω fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits. For additional information, see Motorola Application Note AN-769, "Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter."

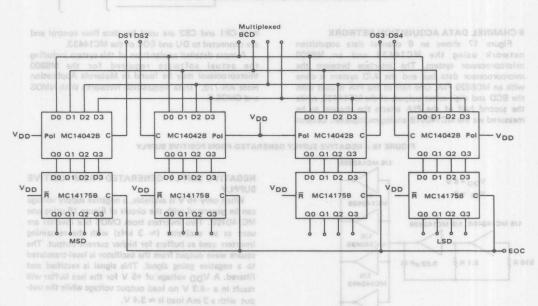
PARALLEL BCD DATA OIJTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16.

Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is VSS. In most cases, a two supply system with VSS connected to VAG is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 - DEMULTIPLEXING FOR MC14433 BCD DATA



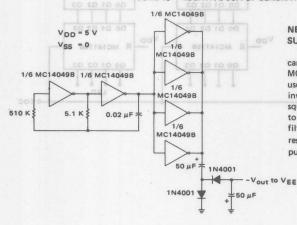
8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8 channel data acquisition network using the MC14433 and an M6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6820 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control

lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

A more detailed explanation of this system including the actual software required for the M6800 microprocessor may be found in Motorola Application Note AN-770, "Data Acquisition Networks With NMOS and CMOS."

FIGURE 18 - NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049B. Two inverters from CMOS hex inverter are used as an oscillator (≈ 3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A VDD voltage of +5 V for the hex buffer will result in a -4.3 V no load output voltage while the output with a 2 mA load is ≈ 3.4 V.



MC14442

Advance Information

ANALOG-TO-DIGITAL CONVERTER (ADC)

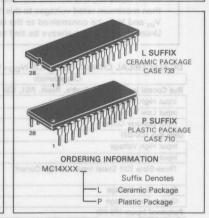
The MC14442 ADC is a 28-pin bus-compatible 8-bit A/D converter with additional digital input capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles and allows up to 11 analog inputs. In addition, the part can accept up to 6 digital inputs. These inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control and bus interface is in-

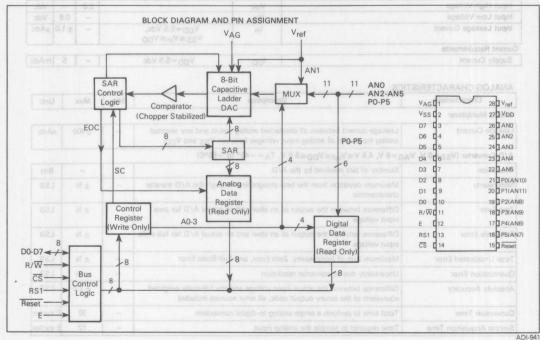
- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at f_E = 1.0 MHz
- Ratiometric Conversion
- Completely Programmable
- Completely Software Compatible with the MC14444 ADC
- 5 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%

CMOS LSI

(LOW-POWER SILICON GATE COMPLEMENTARY MOSI

MICROPROCESSOR-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER





M MOTOROLA

ARSOLLITE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V _{DD}	-0.5 to +6.5	Vdc
Input Voltage	Vin	-0.5 to $V_{DD} + 0.5$	Vdc
Input Current, Per Pin	lin	± 10	mA
Input Current, Per Package	lin	± 20	mA
Operating Temperature Range (Ambient)	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

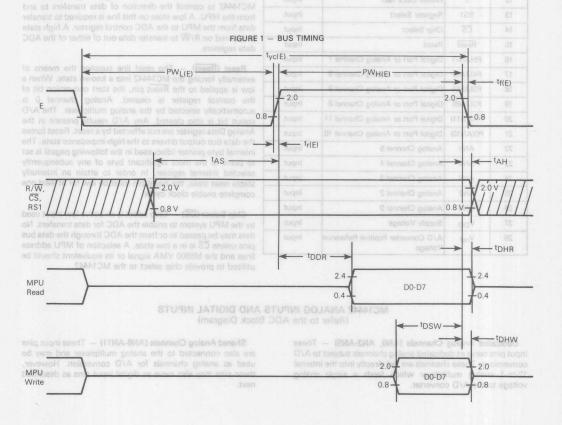
DC ELECTRICAL CHARACTERISTICS (VDD = 5.0 V ± 10%, VSS = 0 V, TA = TL to TH unless otherwise noted)

Characteristic		Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/W, Enable, Reset, RS1, CS)			(IVA anitsmixpino A svizseo:	ic Suc	mana	3.6
Input High Voltage		VIH	sion at fp= 1.0 MHz	2.0	200	Vdc
Input Low Voltage		VIL	Providence of Co.	- Table	0.8	Vdc
Input Leakage Current	Li Bhailid	lin	V _{in} = 0 to 5.5 Vdc	- Tor	±1	μAdd
Data Bus (D0-D7)			alconinario)	- Acces	- Contractor	
Input High Voltage		VIH	offware Compatible with the MC	2.0	dillico	Vdc
Input Low Voltage		VIL	Slugni golenik	Digital.	0.8	Vdc
Three-State (Off State) Input Leakage Current	Supply	ITSI	V _{DD} =5.5 Vdc, V _{SS} ≤V _{in} ≤V _{DD}	se <u>l</u> e	± 10	μAdo
Ouput High Voltage		Voн	IOH = - 1.6 mA	2.4	2040	V
Output Low Voltage		VOL	IOL = 1.6 mA	-	0.4	V
Peripheral Inputs (P0-P5)						-
Input High Voltage		VIH		2.0	_	Vdc
Input Low Voltage	7167	VIL	BLOCK DIAGRAM AND	-	0.8	Vdc
Input Leakage Current	tenV	lin a	V _{DD} =5.5 Vdc, V _{SS} ≤V _{in} ≤V _{DD}	-	±1.0	μAdd
Current Requirements						
Supply Current	4	IDD	V _{DD} =5.5 Vdc	-	5	mAdd

ANALOG CHARACTERISTICS OVA

Characteristic	PO-P5	Description 1900 B.	Min	Max	Unit
Analog Multiplexer		Chapper Stabilized	14		
Leakage Current		netween all deselected analog inputs and any selected all analog input voltages between VSS and VDD	-	± 400	nAdc
A/D Converter (VSS=0 V, V	AG=0 V, 4.5 V≤V _{re}	$_{ef} \le V_{DD} \le 5.5 \text{ V}, T_A = -40^{\circ} \text{ to } +85^{\circ}\text{C})$			
Resolution	Number of bits re	solved by the A/D	8	-	Bits
Nonlinearity	Maximum deviation	on from the best straight line through the A/D transfer	-	± ½	LSB
Zero Error	Difference between input voltage	en the output of an ideal and an actual A/D for zero	Contic	± ½	LSB
Full-Scale Error	Difference between input voltage	en the output of an ideal and an actual A/D for full-scale	*	± ½	LSB
Total Unadjusted Error	Maximum sum of	Nonlinearity, Zero Error, and Full-Scale Error	84	± ½	LSB
Quantization Error	Uncertainty due to	o converter resolution	-	± 1/2	LSB
Absolute Accuracy		en the actual input voltage and the full-scale weighted binary output code, all error sources included		± 1.0	LSB
Conversion Time	Total time to perfe	orm a single analog-to-digital conversion	-	32	E cycles
Sample Acquisition Time	Time required to s	sample the analog input	_	12	E cycles

Characteristic		Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time (1/f _E)	high	bncorDetolenA	t _{cyc(E)}	943	-	ns
Enable Clock Pulse Width, High	Input	E	PWH(E)	440	-	ns
Enable Clock Pulse Width, Low	Input/ Dutput	E (8SW)	PW _{L(E)}	410	-	ns
Clock Rise Time	Ingut/Output	E	t _{r(E)}	80	25	ns
Clock Fall Time	Input/Output	E	t _{f(E)}	20	30	ns
Address Setup Time at 500 A pdf to tuo pne of the anatonist	Ingun/Output	RS1, R/W, CS	tAS	145	-	ns
Data Delay (Read)	Input/Output	D0-D7	tDDR	02	335	ns
Data Setup (Write)	tugtiiO\tiuani	D0-D7	tDSW	185	-	ns
Address Hold Time (1997) 6 8 100 210 100 211 920 215	TugtoO\tegn(RS1, R/W, CS	THE ETAH ISO	10	-	ns
Input Data Hold Time	input/Output	D0-D7	tDHW	10	-	ns
Output Data Hold Time	Jugni	D0-D7	tDHR	10	-	ns



PIN FUNCTIONS

Pin No.	Pin Name	lodmy8 Function	Туре
an1	VAG	A/D Converter Analog Ground	Input
2	Vss	Digital Ground	Input
3	D7	Data Bus Bit 7 (MSB)	Input/Output
a (4	D6	Data Bus Bit 6	Input/Output
5	D5	Data Bus Bit 5	Input/Output
6	D4	Data Bus Bit 4 33 WAR 138	Input/Output
7	D3	Data Bus Bit 3	Input/Output
8	D2	Data Bus Bit 2	Input/Output
9	D1	Data Bus Bit 1 25 WAR 128	Input/Output
10	D0	Data Bus Bit 0 (LSB)	Input/Output
:1:1	R/W	Read/Write 50.00	Input
12	E	Enable Clock (ϕ 2)	Input
13	RS1	Register Select	Input
14	CS	Chip Select	Input
15	Reset	Reset	Input
16	P5(AN7)	Digital Port or Analog Channel 7	Input
17	P4(AN6)	Digital Port or Analog Channel 6	Input
18	P3(AN9)	Digital Port or Analog Channel 9	Input
19	P2(AN8)	Digital Port or Analog Channel 8	Input
20	P1(AN11)	Digital Port or Analog Channel 11	Input
21	P0(AN10)	Digital Port or Analog Channel 10	Input
22	AN5	Analog Channel 5	Input
23	AN4	Analog Channel 4	Input
24	AN3	Analog Channel 3	Input
25	AN2	Analog Channel 2	Input
26	ANO	Analog Channel 0	Input
27	V _{DD}	Supply Voltage	Input
28 RHQ1	V _{ref}	A/D Converter Positive Reference Voltage	Input

MC14442 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) — The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) — The enable clock provides two functions for the MC14442. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/\overline{W}) — The R/\overline{W} signal is provided to the MC14442 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/\overline{W} to transfer data out of either of the ADC data registers.

Reset (Reset) — The reset line supplies the means of externally forcing the MC14442 into a known state. When a low is applied to the Reset pin, the start conversion bit of the control register is cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the Reset pin must be low for at least one complete enable clock cycle.

Chip Select (\overline{CS}) — Chip select is an active low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless \overline{CS} is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14442.

MC14442 ANALOG INPUTS AND DIGITAL INPUTS (Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN5) — These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 12-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN6-AN11) — These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) — P0-P5 comprise a 6-bit — may be of digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is ed to the not programmed, but instead is simply assigned by the state of the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

MC14442 SUPPLY VOLTAGE PINS

Positive Supply Voltage (V_{DD}) — V_{DD} is used internally to supply, power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14442 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (VSS) - VSS should be tied to system digital ground or the negative terminal of the VDD power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high VSS rejection.

Positive A/D Reference Voltage (V_{ref}) — This is the voltage used internally to provide references to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD} , but degradation of absolute A/D accuracy may result due to switchingnoise on V_{DD} .

A/D Ground Reference Voltage (VAG) — This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy

may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

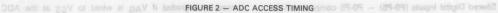
MC14442 INTERNAL REGISTERS

The MC14442 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

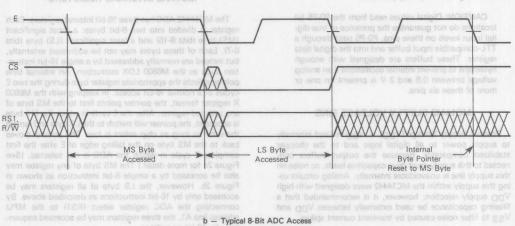
CAUTION: RS1 should **not** be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

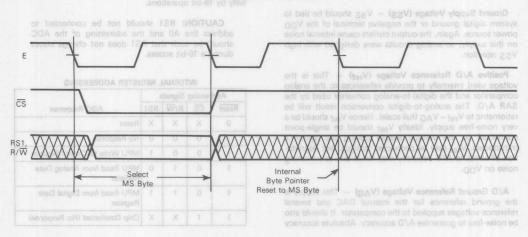
INTERNAL REGISTER ADDRESSING

Addressing Signals				/
Reset	CS	R/W	RS1	ADC Response
0	X	X	X	Reset
770	0	0	0	No Response
\1/)\	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

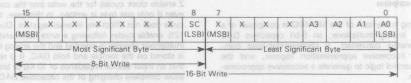


a - Typical 16-Bit ADC Access





MC14442 CONTROL REGISTER (Write Only)



Analog Multiplexer Address (A0-A3) — These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

Hexadecimal Address (A3 = MSB)		Select Select
	0	AN0
	See Figure 4 A/D	Vref
	2-5	AN2-AN5
	6-B	AN6-AN11
	C-F	Undefined

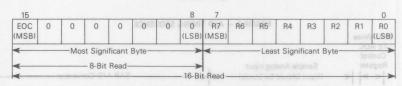
Start A/D Conversion (SC) — When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel

will begin immediately after the completion of the control register write.

Unused Bits (X) — Bits 4-7 and 9-15 of the ADC Control Register are not used internally.

NOTE: A 16-bit control register write is required to change the analog multiplexer address. However, 8-bit writes to the MC14442 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

MC14442 ANALOG DATA REGISTER (Read Only)

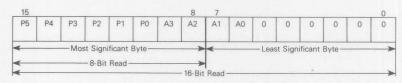


A/D Result (R0-R7) — The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of \$FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) — The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status

bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14442 DIGITAL DATA REGISTER (Read Only)



Logical Zero (0) — These bits are always read as logical zero.

Analog Multiplexer Address (A0-A3) - The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) — The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

2

ANALOG SUBSYSTEM (See Block Diagram)

General Description

The analog subsystem of the MC14442 is composed of a 12-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of twelve channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as VDD and VSS power supply rejection.

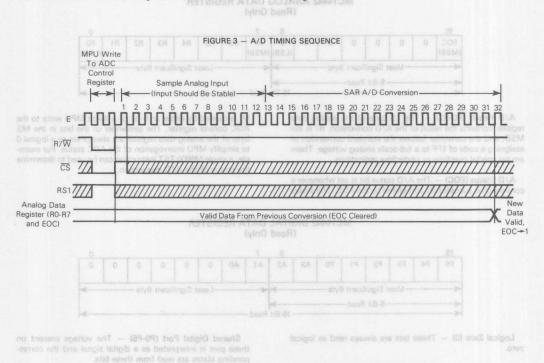
Device Operations no anoistevnou betseget nertw luteau

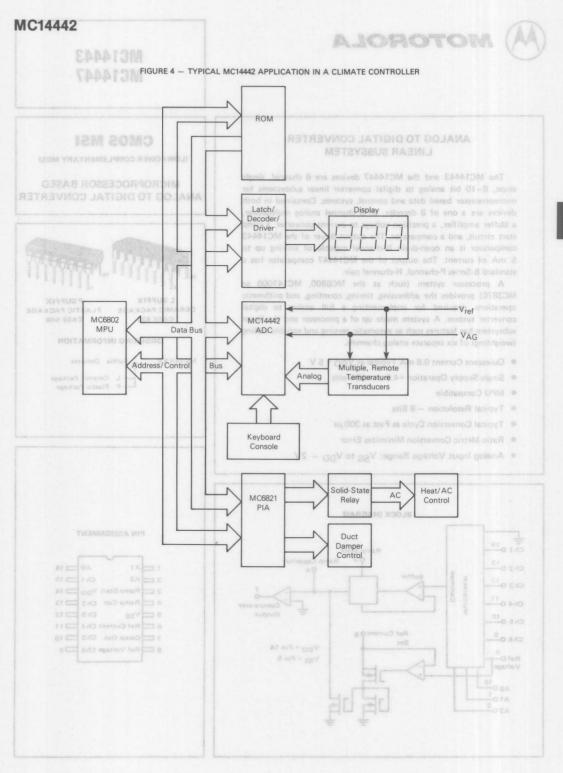
An A/D conversion is initiated by writing a logical 1 into the EOC bit will the SC bit of the ADC control register. The MC14442 allows progress.

2 enable clock cycles for the write into the control register even if only one byte is written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 $K\Omega$ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logic 0) if an A/D conversion is in progress.





MC14443 MC14447

ANALOG TO DIGITAL CONVERTER LINEAR SUBSYSTEM

RE 4 - TYP CAL MC14442 APPLICATION IN A CLIMATE CONTROLLER

The MC14443 and the MC14447 devices are 6 channel, single slope, 8–10 bit analog to digital converter linear subsystems for microprocessor based data and control, systems. Contained in both devices are a one of 8 decoder, an 8 channel analog multiplexer, a buffer amplifier, a precision voltage to current converter, a ramp start circuit, and a comparator. The output driver of the MC14443 comparator is an open-drain N-channel capable of sinking up to 5 mA of current. The output of the MC14447 comparator has a standard B-Series P-channel. N-channel pair.

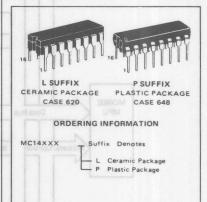
A processor system (such as the MC6800, MC141000 or MC3870) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog to digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

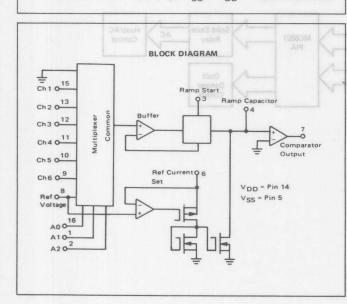
- Quiescent Current 0.8 mA Typical at VDD = 5 V
- Single Supply Operation +4.5 to +18 Volts
- MPU Compatible
- Typical Resolution 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} 2V

CMOS MSI

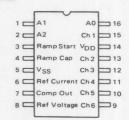
(LOW-POWER COMPLEMENTARY MOS)

MICROPROCESSOR BASED ANALOG TO DIGITAL CONVERTER





PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to VSS)

Rating			Symbol	Value	Unit
DC Supply Voltage	619.0	titian	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	081		V _{in} 0	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	61.	-	1 0	10	mAdd
Operating Temperature Range	250	-	TA	-40 to +85	°C
Storage Temperature Range	380		T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) < V_{DD}.

ELECTRICAL CHARACTERISTICS

			15	VDD	TI	ow		25°C		Thi	gh	
Characte	ristic		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Uni
Output Voltage-Comparato	300	"0" Level	VOL.	5.0	-	0.05	-	0.01	0.05	_	0.05	Vd
Vin @ Pin 4 = 0 V			21	10	_	0.05	-	0.01	0.05	-	0.05	
an 000f			5.0	15	195_	0.05	N	0.01	0.05	-	0.05	
Vin @ Pin 4 = 1.0 V		"1" Level	.VOH	5.0	4.95	-	4.95	4.99	_	4.95	_	Vd
(R ₁ = 10 k, MC14447	only)		- 011	10	9.95	_	9.95	9.99	_	9.95	_	
an 088	450		5.0	15	14.95	-	14.95	14.99	-	14.95	_	
Input Voltage-Address, Ram	p Start	"O Level"	VIL									Vd
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$			81	5.0	-	1.5		2.25	1.5		1.5	
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$			6.0	10	12 _	3.0	_	4.50	3.0	no <u>ir</u> age	3.0	sloith
(VO = 13.5 or 1.5 Vdc)			97	15	-	4.0	-	6.75	4.0	-	4.0	
220		"1" Level	VIH									Vd
$(V_0 = 0.5 \text{ or } 4.5 \text{ Vdc})$			0.8	5.0	3.5	_	3.5	2.75	_	3.5	art Dale	gm
$(V_0 = 1.0 \text{ or } 9.0 \text{ Vdc})$			10	10	7.0	-	7.0	5.50	-	7.0	_	
(V _O = 1.5 or 13.5 Vdc)			15	15	11.0	-	11.0	8.25		11.0	-	
Output Drive Current-Comp	parator	- 1	ІОН		U .					1 3	mit na	mAc
Vin @ Pin 4 = 1.0 V (MC	14447 only)	01			-				76	10001	13
(V _{OH} = 2.5 Vdc)			16	5.0	-2.5	-	-2.1	-4.2	-	-1.7	P = 10	98
(V _{OH} = 4.6 Vdc)			slon delay	5.0	-0.52	delay, ra	-0.44	-0.88	gidlum i	-0.36	mi Lnei	guis
$(V_{OH} = 9.5 \text{ Vdc})$				10	-1.3	-	-1.1	-2.25		-0.9	red-Lings.	deles s
$(V_{OH} = 13.5 \text{ Vdc})$				15	-3.6	-	-3.0	-8.8	-	-2.4	-	
Vin @ Pin 4 = 0 V			IOL									mAd
$(V_{OL} = 0.4 \text{ Vdc})$			MOITA	5.0	0.52	-	0.44	0.88	-	0.36	-	
$(V_{OL} = 0.5 \text{ Vdc})$			615411	10	1.3	-	1.1	2.25	-	0.9	-	
(V _{OL} = 1.5 Vdc)				15	3.6	-	3.0	8.8	-	2.4	-	-
Input Current-Address, Ran	np Start	somos sess	lin	15	21 -7	±0.3	257 11	9. '(7)bet	± 0.3	0010	± 1.0	μАс
Input Current-Analog Input	S		lin	15	- 7	HADRIA I	P-HANDH	±0.1	± 10	10 0 P	1001000	nAc
Input Capacitance-Address,	Ramp Start		Cin	15	-	-	-	5.0	7.5	-	-	pF
Vin = 0 V			the ram	WO S	DESIGN	meR an	When t	(E mi	Stairt	(Ramp)	THAT	BIP E
Quiescent Current	Indui au	nection to I	IDD	5	श्चार्य १	Start	me# !	0.8	V Jann	orla_tus	ini Jar	mAd
				10	-	-	-	1.5	swell o	ms+of	iniged t	otios
				15	-	-	-	1.7	-	-	-	
Crosstalk Between Any Two	Input Chan	nels	VCr	no.Tiein	otion	o ottora	WET (8	0	4.0	OR O	DATA:	mVc
Reference Current Range			1 _R	-		-	10	11100011	50	tor Taxin	is a Torre	μΑσ
Channel Input Voltage Rang	ge		VCM	5	-		0	-	2.5	-	-	Vd
				10	-		0	.22V)	7.0	z Alaw		GAT
				15	is syste	mig_gin	0	155 A3	12	R MENAN	Man.	10 34.53
Buffer Amplifier Output Offs			VBO	5	-	-	-	0.285	-	_	-	Vde
			gso gms	10	serbeib	01_ (8	nt, Pin	0.400	BLTV	BRRUS	BONE	Har
			V-gaV	15 50	DB # M	emuo la	piq+T.	0.420	ont-ylqr	102 -0 Vi7	0 8410S	(tel
Comparator Threshold			VTC	5	-	_	0	0.195	VBO	-	_	Vde
	berlosen a		erly nedw	10 al	uqtuo	zid T (0	0.275	VBO	THO:	RATOR	MPA
				15	-	-	0	0.290	VBO	-	aiu ll oris	h rini
Reference Voltage Range			VR	5	-	-	2.0	-	3.0	-	-	Vde
			anaste.	10	edt a	aidT .	2.0	uno The Y	8.0	0.00	VCE V	BR3:
n is compared.	WOLLSHIP S	and House Of	afigual	15	2111 8	SHEET A	2.0	Voltage	13.0	PART IN	200	2172
Conversion Linearity			Lc	-	-	-	-	0.15	0.5	-	-	% Fu
Vin = VDD - 3 V for C >	100 nF		the state of the	of Distance	beech or	ant (3)	P. P. O.	- PP D	25 am	SLS (P		Scal

POSITIVE POWER SUPPLY (VDD, Pin 14) This pin is the package positive power supply pin.

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

	fields; h	Cha	aracterist	tic		Vide	Sumbol	8.0	V _{DD} Vdc	Min	Тур	Max	Unit
Output	Rise Tin	ne-Comp	parator		(MC144	47 only)	O TELH	01	3.0 5.0 AV	-	120	240	perlo insugni
		n mumi) ance circ					01		10	-	75	150	DC Current
						20			15	-	65	130	aT-mosteranch
Output	Fall Tim	ne-Comp	parator	four be			tTHI	1.00	5.0	-	250	500	ns
						50	1150	-	10	-	350	700	Storage Tem
							UGITE	3 CI	15	-	650	1300	migrage rem
Propaga	ation Del	ay Time-	-Compa	rator	N	AC14443	tPLH		5.0	-	550	1100	LECT RICH
				(RL	= 10 k	to VDD)			10	-	500	1000	ADDA EDBILE
				29°62		WO	T I	ap V	15	-	550	1100	
							tPHL	Vide	5.0	-	350	700	ns
								0.8	10	19v=1 "0"	300	600	Output Volt
							- 1	01	15	-	300	600	vin ⊕ Pic
					- N	AC14447	TPLH	15	5.0	-	600	1200	ns
							80.6	0.8	10	1005J "I"	475	950	V _{in} @ Pin
							20.0	10	15	-	500	1000	(8)
							e tPHL	ar	5.0	-	450	980	ns
									10	"lawed 0"	540	1080	Input Voltar
								0.0	15	_	750	1500	h = oVI
Multiple	exer Pro	pagation	Delay	4.50		3.0	tM	OT	5.0	-	180	360	ns
				6.75				25	10	-	125	250	IVO = 12
									15	Investment to a second	110	220	7 10
Ramp S	start Del	ay Time		2.76	3.5		tTS	0.8	5.0	-	40	80	ns ns
				08.8			7.0	000	10	_	25		1.1 = 0V)
	-	OFF		8.25	11.0		0.11	ar	15	-	20	40	Li s ovi
Acquisi	tion Tim	ne *		1			tA		5.0	_	30		μs μο
	= 1000								10	_	15		Vin @ Pil
RR	EF = 10	00 kΩ					ac-	0.8	15	-	14	28	Comment of the commen

^{*} Acquisition Time includes multiplexer propagation delay, ramp start propagation delay and the time required to charge ramp capacitor to the selected input voltage.

DEVICE OPERATION

ADDRESS INPUTS SELECT (A0, A1, A2, Pins 1, 2, 16) The input voltage source to be presented to the measurement system according to the Truth Table shown in Figure 2.

RAMP START (Ramp Start, Pin 3) When the Ramp Start is low, the ramp capacitor is charged to a voltage associated with the selected input channel. When the Ramp Start is brought high, the connection to the input channel is broken and the capacitor begins to ramp toward VSS.

RAMP CAPACITOR (Ramp Cap, Pin 4) The ramp capacitor is used to generate a time period when discharged from a selected voltage via a precise reference current.

NEGATIVE POWER SUPPLY (VSS, Pin 5) This pin is system ground.

88.0 PR.0

REFERENCE CURRENT (Ref Current, Pin 6) To discharge the ramp capacitor, the reference current is fixed via a resistor (R_{Ref}) to a positive supply from pin 6. Typical current is equal to (V_{DD} - V_{Ref})/R_{Ref}.

COMPARATOR OUTPUT (Comp Out, Pin 7) This output is low when the capacitor has reached the discharged voltage and is high otherwise.

REFERENCE VOLTAGE (Ref Voltage, Pin 8). This is the known voltage to which the unknown is compared.

INPUT CHANNELS (Pins 9, 10, 11, 12, 13, 15) Input channels 1 through,6 are used to monitor up to six separate unknown voltages. Selection is via the address inputs.

POSITIVE POWER SUPPLY (VDD, Pin 14) This pin is the package positive power supply pin.

MC14444

3 Dedicated Digital Inputs





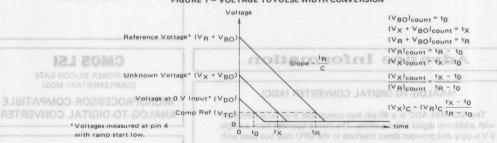
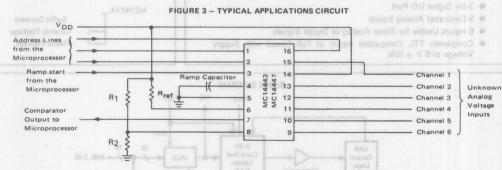


FIGURE 2-TRUTH TABLE: bus nog O'll stiglb tid-E a sed neg out moil

A2	A1	A0	og or aigin	Input Selected	
0	0	0	VSS	Channel 0 (ground)	inputs. All necessary tion, conversion contri-
0	0	1	Ch1	Channel 1	is included.
0	- 1	0	Ch2	Channel 2	Direct Interface to M
0	1	1	Ch3	Channel 3	Dynamic Successive
1	0	0	Ch4	Channel 4	32 as Conversion a
1	0	1	Ch5	Channel 5	Ratiometric Conver
1	1	0	Ch6	Channel 6	
1	1	1	VRef	Channel 7 (External Reference)	 Completely Program
1	1	1	V _{Ref}	Channel 7 (External Reference)	Poiled or Interrupt

FIGURE 3 - TYPICAL APPLICATIONS CIRCUIT



CONVERSION SEQUENCE

Step No.	A2	A1	AO	Ramp Start	Comment					
1.	1	1	1	0	Channel 7 Selected (Reference Voltage)					
2.	1	1	1	1	Record time until Pin 7 goes low					
3.	0	0	0	0	Channel 0 Selected (Ground)					
4.	0	0	0	1	Record time until Pin 7 goes low					
5.	0	0	1	0	Channel 1 Selected					
6.	0	0	1	1 4 eigeR	Record time until Pin 7 goes low					
poul	- prince		Calcula	te tCh7 - tCh0	= t _{Ch7} ' Step 2-Step 4					
161/gi	9		Calcula	te tCh1 - tCh0	= tCh1' Step 6-Step 4					
10/01	0 6		Calcu	late Vunknown	= VCh7 (tCh1'/tCh7')					
7, a0 b	0		Sugar	0	Channel 2 Selected					
8.	0			1	Record time until Pin 7 goes low					
3.5	4			Calculate tCh2	- tCh0 = tCh2'					
			Calcul		= V _{Ch7} (t _{Ch2} '/t _{Ch7} ')					
etc.										

MC14444

Advance Information

FIGURE 1 - VOLTAGE TO PULSE WIDTH CONVERSION

ANALOG-TO-DIGITAL CONVERTER (ADC)

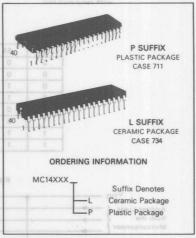
The MC14444 ADC is a 40-pin bus-compatible 8-bit A/D converter with additional digital I/O capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles at 1 MHz and allows for up to 15 analog inputs. In addition, the part has a 3-bit digital I/O port and can accept up to 9 digital inputs. Six of these inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control, bus interface and maskable interrupt capability is included.

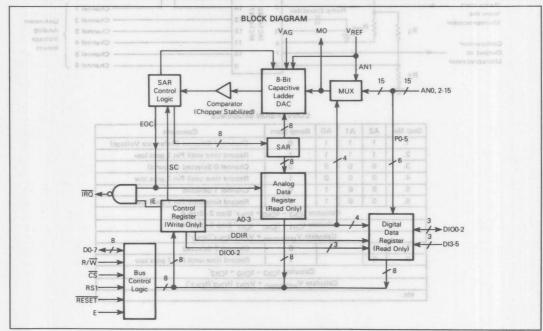
- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at f_E = 1.0 MHz
- Ratiometric Conversion
- Completely Programmable
- Polled or Interrupt Driven Operation
- 3 Dedicated Digital Inputs
- 3-Bit Digital I/O Port
- 9 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- \bullet Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V $\pm\,10\%$

CMOS LSI

(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

MICROPROCESSOR-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER





ADI-878

ABSOLUTE MAXIMUM RATINGS

Max Unit	Rating	Symbol	Value Value	Unit
Supply Voltage		V _{DD}	-0.5 to +6.5 ************************************	Vdc
Input Voltage	- Juojuo rexelo	lum IVin lumi	solens does not word - 0.5 to V _{DD} + 0.5	Vdc
Input Current	new VSS and VDD belonged —			mA
Operating Tempera	ature Range (Ambient)	TA	(DOV≥ 498V≥ V, 0 4-40 to +85. V 0=22V) tenevo	O °CA
Storage Temperati	ure Range	T _{stg}	arts vid bevious and to +65 to +150	°C 8

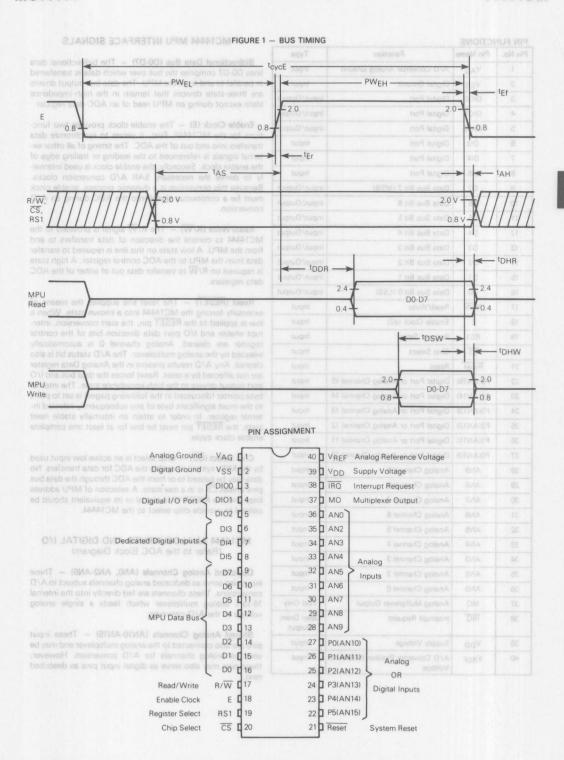
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (VDD=5.0 V ±10%, VSS=0 V, TA=TL to TH unless otherwise noted)

Characte	eristic.	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/W, Enable	, Reset, RS1, CS)	gie analog-t	Lotat hine to perform a sin	30.81	10/218	Conv
Input High Voltage	TOO	VIH	in eldines of payabet awit Bu	2.0	DA_elo	Vdc
Input Low Voltage		VIL		-	0.8	Vdc
Input Leakage Current		lin	V _{in} = 0 to 5.5 Vdc		± 1	μAdo
Interrupt Output (IRQ)			TICS (See Figure 1)	MACTERIS	CHAI	AC
Output Low Voltage lodmy?	Signal	VOL	I _{Load} = 1.6 mAdc	-	0.4	Vdc
Output Leakage Current (Off Sta	te)	ILOH	V _{OH} = V _{DD} = 5.5 Vdc	sk Cycle Ta	10	μAdc
Data Bus (D0-D7)	3		dats High	ck Pulse Wi	el Clo	daria
Input High Voltage	3	VIH	dth, Law	2.0	e Clo	Vdc
Input Low Voltage	3	VIL		TerniT	0.8	Vdc
hree-State (Off State) Input Leakage Current		ITSI	V _{DD} = 5.5 Vdc,	- emil	± 10	μAdo
			V _{SS} ≤V _{in} ≤V _{DD}	and quit	2 000	Acces
Peripheral I/O (DIO0-DIO2, DI3-D	015, P0-P5)			- IOAJID	0.0	ping
Input High Voltage	20-02	VIH		2.0		Vdc
Input Low Voltage	25 Wig ras	VIL		ami I-bio	0.8	Vdc
Input Leakage Current	DI3-DI5, P0-P5	lin	$V_{DD} = 5.5 \text{ Vdc},$ $V_{SS} \leq V_{in} \leq V_{DD}$	Hold Time	± 1.0	μAdc
Output High Voltage	DI00-DI02	Vон	I _{OH} = -0.19 mAdc	V _{DD} -0.4	eQ_fu	Vdc
Output Low Voltage	DI00-DI02	VOL	I _{OL} = 0.975 mAdc	-	0.4	Vdc
Three-State (Off State) Input Leak	sage Current DI00-DI02	ITSI	$V_{DD} = 5.5 \text{ Vdc}$ $V_{SS} \leq V_{Out} \leq V_{DD}$	-	± 10	μAdo
Current Requirements						
Supply Current		IDD	V _{DD} = 5.5 Vdc, f _E = 1 MHz	-	10	mAdo
Converter Input Current		IADC	Analog input current at f _E = 1 MHz with multiplexer inputs between V _{SS} and V _{DD}	-	± 500	nA

finU Characteristic	Value	Description		Min	Max	Unit
Analog Multiplexer	- 01 d 0 -	agV			oltage	Supply Ve
On Resistance	Resistance between each ana	alog input and mu	tiplexer output	-	5 9	ov kΩni
Leakage Current				-	± 400	nAdc
A/D Converter (VSS = 0 V, VA	G=0 V, 4.5, V ≤ VREF ≤ VDD)	AT	e (Ambient)	gnsR erus	Tempera	Operating
Resolution	Number of bits resolved by t	ne A/D		99n87 et	emperatu	Bits
Nonlinearity	Maximum deviation from the characteristic	best straight line	through the A/D transfer	-	± ½	LSB
Zero Error openov vna ro	Difference between the outp input voltage		an actual A/D for zero	ver, it is	± ½	LSB
Full-Scale Error	Difference between the outprinput voltage		an actual A/D for full-scale	oo ed n	± ½,8	LSB
Total Unadjusted Error	Maximum sum of Nonlinearit				± ½	LSB
Quantization Error	Uncertainty due to converter	resolution		-	± ½	LSB
Absolute Accuracy	Difference between the actual equivalent of the binary outp			CHARA	A±1.00	LSB
Conversion Time	Total time to perform a single	e analog-to-digital	conversion	0 0000	32	E cycles
Sample Acquisition Time	Time required to sample the	analog input		-	12	E cycles
bV 8.0 -					v Voltage	vo.J tugnt

AC CHARACTERIS	TICS (See Figure 1)				(0)	Rij tuga				
- 0.4 Vot	Characteristic	YOU		Signal	Symbol	Min	Max	Uni		
Enable Clock Cycle Tir	ne (1/f _E) by è è = ggV = ноV	HOJ		E	tcycE	943	sed to	ns		
Enable Clock Pulse Wi	dth, High			E	PWEH	440	3) au 8	ns		
Enable Clock Pulse Wi	dth, Low	HIV		E	PWEL	410	right	ns		
Clock Rise Time		NE.		E	tEr	abetto,	25	ns		
Clock Fall Time	VDD=5 5 Vdc.	1271		age Cun 3 nt	led Itefil (er	1041 Str	30	ns		
Address Setup Time	GG x ≥ VI x ≤ SS x	1	1	RS1, R/W, CS	tAS	145	-	ns		
Data Delay (READ)		1		D0-D7	tDDR	(DIO)	335	ns		
Data Setup (WRITE)				D0-D7	tDSW	185	uōiH	ns		
Address Hold Time		314		RS1, R/W, CS	tAH	10	WOJ	ns		
Input Data Hold Time	V8525/V90 V8525/V900	181	89-09 3	D0-D7	tDHW	10	Leaks	ns		
Output Data Hold Tim		Уон	5010-00	D0-D7	†DHR	10	Ini R tu	ns		
						Voltage				
bAu Of± -					tel Input Lesk					
					43	nomeniu	ent Req			
						Ing	aly Cum			
	Analog input current at inputs between VSS and VDO				ment	iput Cum		Conv		



PIN FUNCTIONS

PIN PUI	ACTIONS		CONTRACTOR OF THE PARTY OF THE
Pin No.	Pin Name	Function	Type
1	VAG	A/D Converter Analog Ground	Input 30
2	VSS	Digital Ground	Input
3	DI00	Digital Port	Input/Output
4	DIO1	Digital Port	Input/Output
5	DIO2	Digital Port	Input/Output
6	DI3	Digital Port	Input
7	DI4	Digital Port	Input
8HA	D15	Digital Port	Input
9	D7	Data Bus Bit 7 (MSB)	Input/Output
10	D6	Data Bus Bit 6	Input/Output
111	D5	Data Bus Bit 5	Input/Output
12	D4	Data Bus Bit 4	Input/Output
13	D3	Data Bus Bit 3	Input/Output
14	D2	Data Bus Bit 2	Input/Output
15	D1	Data Bus Bit 1	Input/Output
16	D0	Data Bus Bit 0 (LSB)	Input/Output
17	R/W	Read/Write	Input
18	E	Enable Clock (ϕ 2)	Input
19	RS1	Register Select	Input
20	CS	Chip Select	Input
21	Reset	Reset	Input
22	P5(AN15)	Digital Port or Analog Channel 15	Input
23	P4(AN14)	Digital Port or Analog Channel 14	Input
24	P3(AN13)	Digital Port or Analog Channel 13	Input
25	P2(AN12)	Digital Port or Analog Channel 12	Input
26	P1(AN11)	Digital Port or Analog Channel 11	Input
27	P0(AN10)	Digital Port or Analog Channel 10	Input
28	AN9	Analog Channel 9	Input
29	AN8	Analog Channel 8 gumani OAI	Input
30	AN7	Analog Channel 7	Input
31	AN6	Analog Channel 6	Input
32	AN5	Analog Channel 5	Input
33	AN4	Analog Channel 4	Input
34	AN3	Analog Channel 3	Input
35	AN2	Analog Channel 2	Input
36	ANO	Analog Channel 0	Input
37	MO	Analog Multiplexer Output	Test Only
38	ĪRQ	Interrupt Request	Open Drain Output
39	V _{DD}	Supply Voltage	Input
40	VREF	A/D Converter Positive Reference Voltage	alnput

DIMMT 2U8 - 1 32US MC14444 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) — The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) — The enable clock provides two functions for the MC14444. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/ \overline{W}) — The R/ \overline{W} signal is provided to the MC14444 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/ \overline{W} to transfer data out of either of the ADC data registers.

Reset (RESET) — The reset line supplies the means of externally forcing the MC14444 into a known state. When a low is applied to the RESET pin, the start conversion, interrupt enable and I/O port data direction bits of the control register are cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus and I/O port output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the RESET pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{\text{CS}}$) — Chip select is an active low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{\text{CS}}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14444.

MC14444 ANALOG INPUTS AND DIGITAL I/O (Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN9) — These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 16-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN10-AN15) — These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the PO-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

Digital I/O Port (DIO0-DIO2) — These pins serve as a 3-bit digital I/O port. At reset the port is configured as an input and may be read from the ADC digital data register. The port may be programmed as an output by setting the DDIR bit in the control register to a logical 1. See the control register discussion for further details. When configured as an output the DIO port will provide CMOS logic levels for limited dc load currents. (Refer to the Electrical Specifications for the dc drive capability of this port.) New output states are transferred to the external pins on the last falling edge of E during a 16-bit write to the control register. When configured as an input, the port will accept both TTL and CMOS logic

Dedicated Digital Inputs (DI3-DI5) - These three pins are dedicated as digital inputs whose values may be read from the ADC digital data register. They are also TTL and CMOS compatible

MC14444 SUPPLY VOLTAGE PINS AND TEST PIN

Positive Supply Voltage (VDD) - VDD is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14444 were designed with high Vnn supply rejection; however, it is recommended that a filtering capacitance be used externally between Vpp and VSS to filter noise caused by transient current spikes.

Ground Supply Voltage (VSS) - VSS should be tied to system digital ground or the negative terminal of the Vnn power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high VSS rejection.

Positive A/D Reference Voltage (VREF) - This is the voltage used internally to provide references to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{\mbox{REF}} - V_{\mbox{AG}}$ (full scale). Hence $V_{\mbox{REF}}$ should be a very noise-free supply. Ideally VRFF should be singlepoint connected to the voltage supply driving the system's transducers. VREF may be connected to VDD, but degradation of absolute A/D accuracy may result due to switching noise on VDD.

Shared Digital Inputs (P0-P5) - P0-P5 comprise a 6-bit A/D Ground Reference Voltage (VAG) - This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if VAG is wired to VSS at the ADC package unless Vss has been sufficiently filtered to remove switching noise. Ideally VAG should be single-point grounded to the system analog ground supply.

> Multiplexer Output (MO) - The analog multiplexer selects one of 16 analog input channels and connects it to the input of the A/D converter. The multiplexer output is internally connected to the A/D input and requires no external jumpers. Since loading of the MO pin affects the charging time of the DAC, it is recommended that no connection be made to the MO pin.

MC14444 INTERNAL REGISTERS

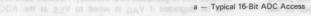
The MC14444 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

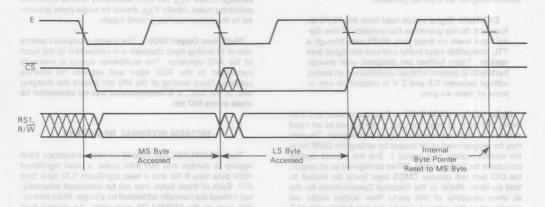
CAUTION: RS1 should not be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

INTERNAL REGISTER ADDRESSING

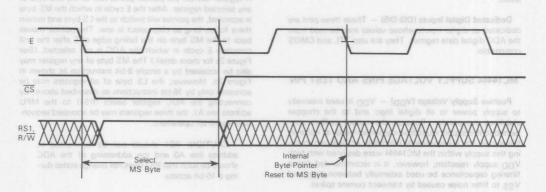
Add	ressing	Signal	s				
RESET	CS	R/W	RS1	ADC Response			
0	X	X	X	Reset			
1	0	0	0	No Response			
1	0	0	1	MPU Write to Control Register			
1	0	1	0	MPU Read from Analog Data Register			
1	0	1	1	MPU Read from Digital Data Register			
1	1	X	X	Chip Deselected (No Response)			







during a 16-bit write to the control register. When reess ADC Access Dispersion of the appropriate register byte during the two E as an input, the port will access both TTL and CMOS logic.

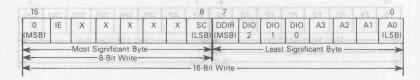


Ground Supply Voltage (VSS) - VSS should be tied to system digital ground or the negative terminal of the Vpp power source, Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high Vost rejection.

		Adds
Reset		

Positive A/D Reterence Voltage (VRgg) — This is the voltage used internally to provide reterences to the analog configurator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be resumeting to VREF — VAG thuis case), thence VREF should be a vary noise free supply. Ideally VREF should be single-point connected to the voltage supply driving the system a transducers. VREF may be connected to VDD, but degradation of absolute A/D accuracy may result due to switching noise on VDD.

MC14444 CONTROL REGISTER (Write Only)



Analog Multiplexer Address (A0-A3) — These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

Hexade	cimal Address (A3 = MSB)	Select
	0	ANO
	1	VRFF
	2-9	AN2-AN9
	A-F	AN10-AN15(P0-P5)

Digital I/O Output (DIO0-DIO2) — When the MPU configures the 3-bit I/O port as an output, these are the bit locations into which the output states are written.

I/O Port Data Direction (DDIR) — This is the data direction bit for the 3-bit I/O port. A logical 1 configures the port as output while a logical 0 configures the port as input.

Start A/D Conversion (SC) — When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel

will begin immediately after the completion of the control register write.

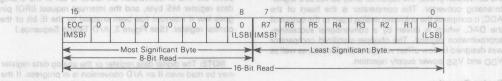
Unused Bits (X) — Bits 9-13 of the ADC Control Register are not used internally.

Interrupt Enable (IE) — The interrupt enable bit, when set to a logical 1, allows the IRO pin to be activated at the completion of the next analog to digital conversion.

Control Register MSB — The MSB of the most significant by the of the ADC control register must be written as a logical MPU con-

NOTE: A 16-bit control register write is required to change the analog multiplexer address or to update the DIO port. However, 8-bit writes to the MC14444 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

MC14444 ANALOG DATA REGISTER (Read Only)



MA/D Result (R0-R7) — The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of \$FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) - The A/D status bit is set whenever a

conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single 8-bit M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14444 DIGITAL DATA REGISTER (Read Only)



Digital I/O Port (DIO0-DIO2) — The states of the three digital I/O pins are read from these bits regardless of whether the port is configured as input or output.

Dedicated Digital Input (DI3-DI5) — The states of the three dedicated digital inputs are read from these bits.

Analog Multiplexer Address (A0-A3) — The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) — The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

MANALOG SUBSYSTEM AND Register MSB - The MSB of the most significant

Isolgol is as neithwied teum relaiger forthoo DUA ent (See Block Diagram)

General Description

The analog subsystem of the MC14444 is composed of a 16-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of sixteen channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as VDD and VSS power supply rejection.

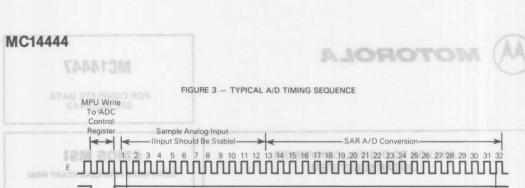
Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14444 allows

2 enable clock cycles for the write into the control register even if only 8 bits are written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 K Ω or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte, and the interrupt request (IRQ) pin goes low if interrupt has been enabled by the IE bit of the control register. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logical 0) if an A/D conversion is in progress.



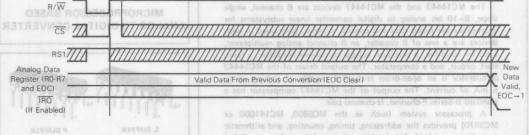
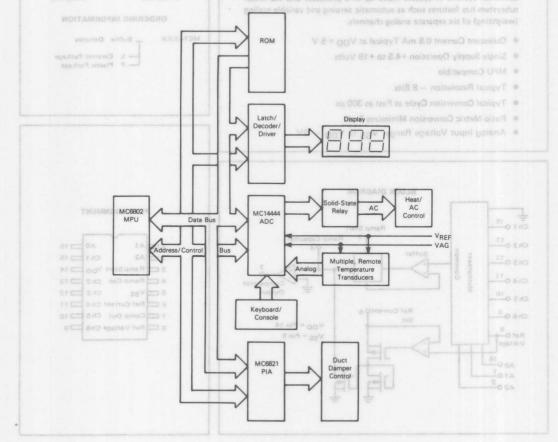


FIGURE 4 - TYPICAL MC14444 APPLICATION IN A CLIMATE CONTROLLER



MC14447

FOR COMPLETE DATA SEE MC14443

ANALOG TO DIGITAL CONVERTER LINEAR SUBSYSTEM

FIGURE 3 - TYPICAL A/D TIMING SEQUENCE

The MC14443 and the MC14447 devices are 6 channel, single slope, 8–10 bit analog to digital converter linear subsystems for microprocessor based data and control, systems. Contained in both devices are a one of 8 decoder, an 8 channel analog multiplexer, a buffer amplifier, a precision voltage to current converter, a ramp start circuit, and a comparator. The output driver of the MC14443 comparator is an open-drain N-channel capable of sinking up to 5 mA of current. The output of the MC14447 comparator has a standard B-Series P-channel, N-channel pair.

A processor system (such as the MC6800, MC141000 or MC3870) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog to digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at VDD = 5 V
- Single Supply Operation +4.5 to +18 Volts
- MPU Compatible
- Typical Resolution 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} 2V

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

MICROPROCESSOR BASED
ANALOG TO DIGITAL CONVERTER

16

L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

MC14XXX Suffix Denotes

L Ceramic Package
P Plastic Package

BLOCK DIAGRAM Ch 1 0 15 Ramp Start 03 Ch 2 0 13 Ramp Capacitor Ch3 0 12 Ch4 0 11 Comparator Ch 5 0 10 Output Ref Current Q 6 Ch6 0 9 Set VDD = Pin 14 Ref O VSS = Pin 5 Voltage 16 A0 0 A10-A2 0

PIN ASSIGNMENT 1 - A1 AOL **1**6 2 A2 **15** Ch 1 Ramp Start VDD □ 14 3 □ 4 Ramp Cap Ch 2 13 5 VSS Ch 3 12 6 Ref Current Ch4 11 7 Comp Out Ch5 10 8 Ref Voltage Ch6 9

2-56



MC14457

SCAAFON FICAASS

MC14457 TRANSMITTER MC14458 RECEIVER

The MC14457 and MC14458 are a transmitter and receiver pair of integrated circuits constructed in CMOS monolithic technology. These units are designed for ultrasonic or infrared remote control of TV receivers, converters, communication receivers, and games. Channel selection up to 16 channels can be done single entry; or, up to 256 channels can be done double entry.

FEATURES:

- Low External Component Count
- High Noise Immunity
- Error Free Operation
- One Analog Output From Receiver
- On-Signal Provision
- Low Power
- Operating Voltage Range
 4.5-10.0 Vdc for MC14457
 4.5-5.5 Vdc for MC14458

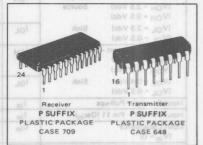
MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating		Symbol	Value	Unit	
DC Supply Voltage	MC14457 MC14458	V _{DD}	-0.5 to +12 -0.5 to +6.0	Vdc	
Input Voltage, All Inputs	-	Vin	-0.5 to V _{DD} + 0.5	Vdc	
DC Current Drain per Pin	veM I	or II as	10	-mAdd	
Operating Temperature Range	20.0	TA	-40 to +85	°C	
Storage Temperature Range		T _{stg}	-65 to +150	°C	

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

TRANSMITTER RECEIVER



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range VSS < (V_{in} or V_{out}) < V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or VDD).

	abV.	4.95		5.0	4.95		4.95	5.0	V.as.	luveJ "!"	
						0101.00	010010050				QQV 10 0 = a(V
						PIN AS	SIGNMEN	115	Jaly	"0" Level	Input Voltage #
				MC144	157	8.1			MC14458		IVO = 4.5 or 0.5 Vdc)
				TRANSM					RECEIVER	"1" Lavel	
1			-	2.75	3.6			6.0			(VQ = 0.5 or 4.5 Vdc)
			1 🗆	R3	VDD	16		1 0	Oscin V	DD 24	Output Drive Current
		8.0-	2	R4	Out 2	15		25.10	Din	Vol 23	(V _{OH} = 2,5 Vde)
			3 🗖	R5 80.0	Out 1	14		100.00		A3 22	(sbV A.0 = JoV)
			4	R2 000	Mod 🗖	13		40	AFT THE	A2 21	
			5	R1 08	Oscout	12		0.0	On mil	A1 5 20	
				C1 0.8	Oscin				JHF/VHF	A0 = 19	
				C2		10			BV	VA 5 18	
			8	VSS	C4 =			1 00		1	
			٠٦	VSS						ady 17	
								1 10.0	M4 ayHV	L8 16	Data Input Hystoresis
							-	1 300 2	VI 2	15 m	
									VI 1	L2 14	
								12 -	/ss	L1 13	(C _{1,1}) of Figure 6 (= 500 kHz



TRANSMITTER MC14457 ELECTRICAL CHARACTERISTICS

MC14457

		VDD	T	ow*		25°C		Thi	gh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level Vin = VDD or 0	V _{OL}	5.0 10	_	0.05 0.05	_	0	0.05 0.05	-	0.05 0.05	Vdc
V _{in} = 0 or V _{DD}	VOH	5.0 10	4.95 9.95		4.95 9.95	5.0 10	C PW	4.95 9.95	_	Vdc
Input Voltage # "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc)	VIL	5.0 10	ieq wvie	1.5	ansenitts	2.25 4.50	1.5	457-and	1.5	Vdc
"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc)	VIH	5.0 10	3.5 7.0	ed remo	3.5 7.0	2.75 5.50	to for surfers, c	3.5 7.0	s stinu s elson V	Vdc
Output Drive Current — Pins 14, 15 (Out 1, 2) (V _{OH} = 2.5 Vdc) Source (V _{OH} = 9.5 ∀dc)	ГОН	5.0 10	-6.0 -3.2	adsins or	-5.0 -2.6	-9.0 -4.5	be done	-3.5 -1.8	256 cha	mAd
(V _{OL} = 2.5 Vdc) Sink (V _{OL} = 0.5 Vdc)	lOL	5.0 10	6.0 3.2	_	5.0 2.6	9.0 4.5	onent	3.5 1.8	ow Exten	mAd
Output Drive Current — Pin 13 (Mod) (V _{OH} = 4.6 Vdc) Source (V _{OH} = 9.5 Vdc)	ІОН	5.0 10	-0.26 -0.6	-	-0.22 -0.55	-0.44 -1.12	n – Nam	-0.18 -0.45	nor Eraer ne Arraig	mAde
(V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc)	lor	5.0	0.26	_	0.22 0.55	0.44 1.12	-	0.18 0.45	n-Signal	mAd
Input Current - Pull-ups	lin	10	-	-	50	500	1000	manifest/		μAdo
Input Current - Pin 11 (Oscin)	lin	10	-	±0.3	-	±0.00001	±0.3		±1.0	μAdd
Input Capacitance (V _{in} = 0)	Cin	-	-	-	-	5.0	7.5	do for M	V 8.6.8.	pF
Quiescent Current - Per Package (Oscin = Low)	IDD	5.0 10	_	50 100	-	0.008 0.016	50 100	-	375 750	μAdo
**Total Supply Current at an External Load Capacitance (C _L) of Figure 4. f = 500 kHz	oi edi:	5.0	_	-	-	5.0	-	-	-	μAdo
(with any Analog command)	160					and the same	manifest to	May 25	MITAGE B	110.613

RECEIVER - MC14458 ELECTRICAL CHARACTERISTICS

or beit od sywys teu stud to at	gri besurU	V _{DD}	Tie	ow*	0-1	25°C		Th	igh "	e loV n
Characteristic	Symb	ol Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0". Vin = VDD or 0	Level VOL	5.0	0.	0.05		0	0.05	agnari	0.05	Vdd
''1" V _{in} = 0 or V _{DD}	Level VOI	5.0	4.95	-	4.95	5.0	-	4.95		Vde
Input Voltage # "0" (V _O = 4.5 or 0.5 Vdc)	Level VIL	5.0	-	1.5	_	2.25	1.5	_	1.5	Vdd
(V _O = 0.5 or 4.5 Vdc)	Level V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdo
Output Drive Current (VOH = 2.5 Vdc) Sour	rce IOH	5.0	-0.5	16 -	-0.5	-1.7	E	-0.4	1	mAd
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.45	- 61	0.4	0.78	35	0.34	-	mAd
Input Current (Oscin, Din)	In	5.0	-	±0.3	Topk	±0.00001	±0.3	_	± 1.0	μAd
Input Current (POR)	e lin	5.0	-	- 21	10	50	400	-	-	μАс
Input Capacitance (V _{in} = 0)	Cin	NAHU DI	-	- 11	5-10	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	r. C volum IDD	5.0	-	5.0	□ <u>70</u>	250	1000	-	-	μAde
Data Input Hysteresis	VHY	s 5.0	-	-	-	0.25	-	-	-	μAd
**Total Supply Current at an External Load Capacitance (CL) of Figure 6 f = 500 kHz	1T	5.0	-	-	-	400	-	-	-	μAd

 $^{\circ}$ Tlow = -40° C $^{\circ}$ Thigh = $+85^{\circ}$ C $^{\circ}$ The formulas given are for the typical characteristics only at 25° C

#Noise immunity specified for worst-case input combination

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc

toposeium topoum

Law Frequency

SWITCHING CHARACTERISTICS (MC14457 - Transmitter VDD = 5 to 15 V, MC14458 - Receiver VDD = 5 V)

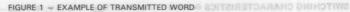
Characteristic	Symbol	Min	Тур	Max	Unit
Output Rise and Fall Time — Receiver CL = 100 pF	tTLH, tTHL	-	0.3	1.0	μs
Oscillator Start-Up Time - Transmitter	ton	-	8.0	_	μs
Clock Pulse Frequency	PRF	11/2	1500	600	kHz

MC14457 - TRANSMITTER

Osc Osc Out 011 0 12 ÷12/÷13 O Output 1 a S/R Start ā Output 2 ÷29 1 0-2 0-Position Counter Inputs 3 0-Modulation Keyboard Decode 40-Control 5 2 Debounce 6 0-ואפעדיסעדפעד פעאכ Column Mux Inputs 9 0-(abo) (abo) (al. 82, 83, 84, 85; 64, 1, 2, 3 be used with nests the black crystal These pins are the row inputs and are applye in the

-ni na to sonazena erti ot sub bebbs ed bluo VDD = Pin 16, 8 Pin 8 SV down device on the oscillator input.

with ceramic transducers or LEDs. In the non-



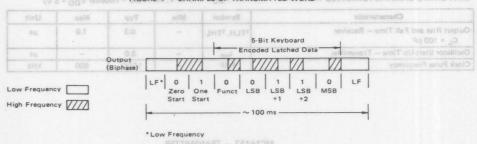
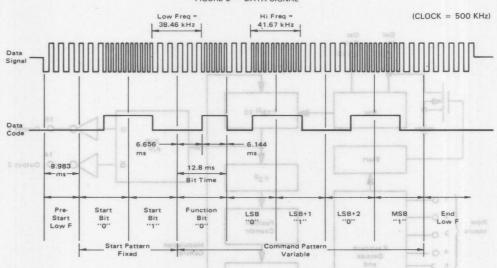


FIGURE 2 - DATA SIGNAL



INPUT/OUTPUT FUNCTIONS — MC14457; TRANSMITTER

ROW INPUTS (R1, R2, R3, R4, R5; Pins 5, 4, 1, 2, 3)

These pins are the row inputs and are active in the low state.

COLUMN INPUTS (C1, C2, C4; Pins 6, 7, 10, 9)

These pins are the column inputs and are active in the low state.

OUTPUT (Out 1, Out 2; Pins 14, 15)

These pins provide push-pull output and can be used with ceramic transducers or LEDs. In the non-operating condition, both outputs are at ground potential.

OSCILLATOR (Oscin; Oscout; Pins 11, 12)

These pins are the input/output terminals of the oscillator. It can be used with ceramic resonator or crystal. The oscillator is automatically turned off after the data is transmitted for low current quiescent operation.

If an external oscillator is used, a current limiting resistor should be added due to the presence of an internal pull-down device on the oscillator input.

MODULATION (Mod; Pin 13)

This pin is a data code output. There is no power-up reset.

TABLE 1 - DATA CODE

Key		Row	Column	Т	ransmitter Dat	ta & Receiver (Output Addr	ess	VA	New
Number	Operation	(Active Low)	(Active Low)	MSB/A3	LSB+2/A2	LSB+1/A1	LSB/A0	Function	Pulse	Notes
1	Digit 0	R1	C1	0	0	0	0	0	-	1
2	Digit 1	R1.	0 C2 0	0 0	0	0	1	0		1
3	Digit 2	R2	C1	0	0	1	0	0	_	1
4	Digit 3	R2	C2	0	40	1	1	0	-	1
5	Digit 4	R3	C1	0	1 4	0 0	T lat Old	0	-	1
6	Digit 5	R3	·C2	0	Parties.	0	TOJ JEST	0	-	1
7	Digit 6	R4	C1	0	1	1 7	0 /	0	-	1
.8	Digit 7	R4	C2	0	1	14	14	0	-	1
9	Digit 8	R5	C1	- 1	0	0	0	0	-	1
10	Digit 9	R5	C2	1	0	0	1	0	-	1
11.3 01	Spare	R1	C3	0	0	0	0	1	1	2
12	Spare de	R1	C4	0	0	0	1	1	1	2
13	Fine Tuning	R2	C3	0	0	1	0-	1	V	3
14	Fine Tuning	R2	C4	0	0	1	1	1	V	3
15	Spare	· R3	СЗ	0	1	0 2750	0	1	V	3
16	Spare	R3	C4	0	1	0/60008	0 1	1	V	3
17	Vol	R4	C3	0	1	1-1-3-	0	1	V	3
18	Vol1	R4	C4	0	1 1	1	1	1	V	3
19	Mute on/off	R5	C3	1	0	0	0	1	V	2
20	Off	R5	C4	1	. 0	0	1.	. 1	V	2
21	Digit 10	R2 + R5	C1	1	0	1	0	0	_	1
22	Digit 11	R2 + R5	C2 060	1	0	1 1	1	0	-	1
23	Digit 12	R3 + R5	C1	1	1	0	0	0	-	1
24	Digit 13	R3 + R5	C2	1	1	0	1	0	_	1
250 🔻	Digit 14	R2+R3+R5	C1	1	1	1	0	0	7-	1
26	Digit 15	R2+R3+R5	C2	1	1	1	1	0 27	-0	JORG1
27	Spare	R2 + R5	C3	1.	0	1	0	1	J_	3
28	Spare	R2 + R5	C4	1	0	1	1	1	-	3
29	Spare	R3 + R5	СЗ	1	1	0	0 112 6	1	-	3
30	Spare	R3 + R5	C4	1	1.	0	1senue	0 1	-	3
31	Spare	R2+R3+R5	C3	1	1	1	0	1	-	3
32	Spare	R2+R3+R5	C4	OUY	1	1	1	1	-O	R03

Notes

- Channel Select Keys (Function Bit = 0). Data is transmitted once each time a key is activated.
- Toggling type On/Off or counter advance type keys.Data is transmitted once each time a key is activated.
- Analog Up/Down or On/Off keys, i.e., one key for Down or Off and another key for Up or On. Data transmission is repeated as long as the key is operated.

In Table 1 all channel select data is noted by the function bit equal to zero. For functions other than channel, the function bit equals one.

The four toggling or counter advance type keys that transmit data once each time a key is activated are Mute, Off, Channel Search Up, and Channel Search Down.

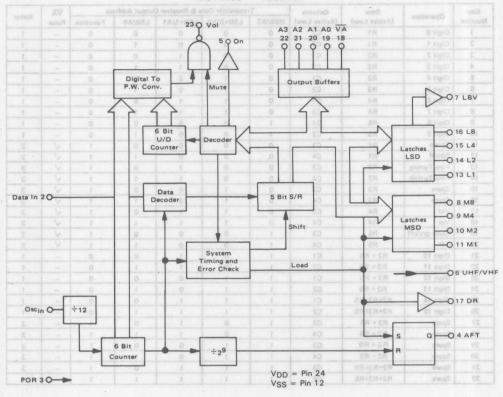
The twelve remaining analog keys (Vol, Tint, Color, etc.) transmit data as long as the key is activated. The keys' functions are arranged to provide the most typical application without grounding of multiple row or columns required.

keyboard position into frequency-modulated biphase

information (continuous transmission of the data word

for duration of key press).





GENERAL DESCRIPTION

This transmitter integrated circuit is used for encoding keyboard position into frequency-modulated biphase data. This integrated circuit can function with a keyboard from 20 to 32 keys and provide either channel select/toggle information (single-word transmission) or analog information (continuous transmission of the data word for duration of key press).

When used in conjunction with the receiver, selection capability is: any single or two-digit channel select up to 256 channels with appropriate keyboard; a maximum of 12 analog control functions; 4 toggle type commands. At an operating voltage of 9.0 volts, the high output drivers provide 4 Vpp into a 1 $k\Omega$ load via an output bridge configuration. The chip features low standby power as all portions are shut off after data transmission, with the counter-chain held in the reset position.

OPERATION

As one example of operation, a free-running ceramic resonator oscillator (at 500 kHz), triggered by the depression of any key, is divided by 12 or 13 to provide frequencies of 41.67 kHz or 38.46 kHz. The transmitted data 'zero' consists of 256 periods of the lower frequency followed by an equal number of the higher frequency. Mark to space ratio is kept at 1:1 in each case. Data 'one' reverses the order of the two frequencies.

Row and column information from the keyboard is encoded into a 5-bit word and loaded onto data latches on the edge of transmit enable. This data, preceded by two bits, 0 and 1, is used in sequence to provide biphase control of the divider and, consequently, the bit pattern transmitted from the unit. Each 7-bit word begins and ends with a low frequency burst. Operation of a channel select key produces an output data stream for a duration of approximately 100 ms.

INPUT/OUTPUT FUNCTIONS - MC14458; RECEIVER

DATA (Din; Pin 2)

The amplified ultrasonic data signal (after amplification and limiting forms a square wave with a peak-to-peak value of V_{DD}) is applied to this input terminal.

OSCILLATOR (Oscin; Pin 1)

The oscillator input pin of the receiver is connected to an oscillator providing, for example, a 500 kHz square-wave signal. A typical oscillator circuit is shown in Figure 5. Accuracy of 1% relative to the oscillator frequency in the transmitter is recommended for satisfactory performance in very high echo-producting environments.

CHANNEL OUTPUTS (L1, 2, 4, 8, M1, 2, 4, 8; Pins 13, 14, 15, 16, 11, 10, 9, 8)

The eight data output pins provide latched data corresponding to the channel selected on the transmitter keyboard. L1 through L8 are the least significant bits; M1 through M8 are the most significant bits. The data on these pins is accompanied by a Data Ready signal.

DATA READY (Pin 17)

A positive pulse with a duration of 768 μ s appears at pin 17 of the transmitter approximately 0.1 second after a complete command is entered on the remote control transmitter keyboard. The negative going edge of this pulse may be used for triggering purposes.

NOTE: A complete command is one digit in the single entry mode or two digits in the double entry mode.

AFT ENABLE (AFT; Pin 4)

The voltage level at this pin is low for a time duration of 0.393 second following a change in selected channel to allow disabling the tuner AFT circuit. Also, miscellaneous commands 0000, 0001, 0010, and 0011 (Channel Search Up/Dòwn, Fine Tuning Up/Down) will cause this disable feature.

POWER-ON RESET (POR; Pin 3)

This pin is low for power-on reset of the analog output to 0 pulse width and off/on output to 0. An internal pull-up device of 10 to 400 μ A will charge an external capacitor. Reset occurs until the input voltage reaches 70% Vpp. All internal registers will also be reset.

ADDRESS (AO, 1, 2, 3; Pins 19, 20, 21, 22)

The Address outputs of the receiver identify selected analog and on/off commands for use in system expansion. The data on these lines is valid when accompanied by a Valid Address pulse.

VALID ADDRESS (VA; Pin 18)

A negative going pulse with a duration of 768 μ s appears at pin 18 approximately 0.1 second after an analog on/off key on the remote control transmitter keyboard is operated. Either edge of this pulse may be used for control of add-on circuits.

MC14457 MC14458

The Valid Address pulse is repeated every 102.4 ms for as long as a key is operated which provides repeated transmission of data when held down.

The Valid Address signal may be used in conjunction with the Address Outputs to drive memories to provide additional control functions such as color, tint, etc.

The Valid Address pulse may be used to provide a stepping clock for up/down counters in a memory. The least significant address line (A0) is used to identify the up or down mode and the remaining address lines (A1, A2, A3) are decoded to enable each individual control circuit.

By adding up/down counters to the Data Outputs, it is possible to use the Valid Address pulse and a decoded address for implementing a channel up/down stepping function from the remote control. Additional On/Off functions may be obtained by using the Valid Address pulse in combination with a decoded address for setting and resetting of latches. The Valid Address signal is disabled in the standby mode (On output at logical 0).

UHF/VHF (Pin 6)

This pin of the receiver provides a low level when the selected channel is a VHF channel (00 to 13, or 84 to 99).

A high level on pin 6 identifies selection of a UHF channel (14 to 83). This signal is provided to permit switching of VHF and UHF tuners.

ON (Pin 5)

This pin of the receiver provides a low level following operation of the Off command (1001) on the remote-control transmitter. The signal on this pin changes to a high level when a channel is selected.

ANALOG OUT (Vol; Pin 23)

An analog voltage in the range between 0 V and V_{DD} is obtained by integrating the signal at the Analog Out pin through a low pass filter. The analog voltage resolution has been chosen to be 64 steps. Its value can be incremented or decremented in steps of one by keys providing commands 0111 and 0110, respectively. (See Table 1.)

The analog voltage can be varied up or down at a speed of approximately 10 steps per second. The D/A conversion is performed with an underflow and an overflow limiting circuit. The Analog Out pin is normally used

A positive

ADDRESS IAO

for the control of volume. The first time power is applied to the remote-control receiver, the volume output is 0 volts.

The Analog Out signal may be increased after a channel has been selected by operating the key providing a command 0111. (Volume Up)

The Analog Out signal may be muted by operating a key on the transmitter providing command 1000. Return to the original output prior to muting may be achieved by operating the mute key a second time or by operating the volume-up key.

In the muted mode the analog level is memorized and cannot be varied by the up/down controls on the transmitter.

least significant address line (A0) is used to identify the up or down mode and the remaining address lines (A1,

LOW BAND (LBV; Pin 7) MONTOMUR TUSTUO TURNI

This pin will go HIGH whenever channels 02, 03, 04, 05, or 06 are selected. The output is LOW for channels 00, 01, and 07 through 99.

SINGLE DIGIT OPERATION TO BE A LOCAL TO BUILDY MEAN

The receiver can be placed in a single-digit mode of operation by connecting the M4 data output (pin 9) to V_{DD} and the UHF output (pin 6) to V_{SS}. In this mode, the L1 through L8 channel outputs will change immediately after the entry of a single digit on the transmitter keys. The M1 through M8 outputs are not used in this mode. (See Figure 6.)

CHANNEL OUTPUTS (L1, 2, 4, 8, M1, 2, 4, 8;

TABLE 2 - COMMAND CODES

Function Bit	MSB	MSB - 1	LSB + 1	LSB	channel selected on the transmon to the transmon to the transmont of the t
0	0	0	0	O areb	Channel Digit 0
bbA ortno		0	0	1	Channel Digit 1
eth 80 an Ac	pauOugo	ad Arou sur	unctil	0	Channel Digit 2
decoco d add	s ritov no	n co O binati	palud .	1	Channel Digit 3
Valid0 Addre	tches The	setting of la	0 0	0	Channel Digit 4
of the tiOutuo	0 0	n the standb	bold	page are far	Channel Digit 5
0	0	1	1	0	Channel Digit 6
0	0	1	1	. 1	Channel Digit 7
0	1	(8 a 0 a M	0	0	Channel Digit 8
0	1	0	0	sids to	Channel Digit 9
wol cosbivo	receiver pr	on of the	1 1	0	Channel Digit 10
or (o) Isnn	a VHF cha	d chaonel is	principal in the state of the s	attais ar	Channel Digit 11
pelos Orifine	bi 8 trig r	o laval rigin	A 0	0.	Channel Digit 12
ivoig 0 tenn	2 airff (8	8 or 141 h	0	1	Channel Digit 13
	The state of the s	RHV ¹ to pri		0	Channel Digit 14
0	1	1	1	1	Channel Digit 15
1	0	0	0	0	Channel Search Down
1	0	0 (8 n	0	1	Channel Search Up
1	0	0	1 .	ofolstrins	Fine Tuning Down
wol syspive	10 190 3381	ent to nice	1	aupansila	Fine Tuning Up
5 (1804) bas	0 370	on of the	0	0	Miscellaneous Command Spare
al on this pir	017	trantmitter	0 11110	s disable	Miscellaneous Command Spare
1betosl	0 0	os natiw jay	al right	0	Volume Down
1	0	1	1	1	Volume Up
1	1	0	0	0	Mute On/Off
1	ol; Pin 23	VI TLO DO	14110	1	Set Off
1	1	. 0	1	11.0 Tuo p	Miscellaneous Command Spare
nga betiveen	1 804 01 6	U		interfiel	Miscellaneous Command Spare
signal at the A	eun Bunea	lesse At pau	0	Is0 istxs	Miscellaneous Command Spare
tiov palans s	illings. Th	asq vupi s n	0.000	and react	Miscellaneous Command Spare
epise Irl value	to be 64 st	en chbeen to	ed call	0	Miscellaneous Command Spare
vet and in an	110000	manual va	1	1	Miscellaneous Command Spare

commands 0111 and 0110, respectively. (See Table 1.)

The analog voltage can be varied up or down at a peed of approximately 10 steps per second. The D/A conversion is performed with an underflow and an over

og V bns V

The Address outputs of the receiver identify selected enelog and on/off commands for use in system expansion. The data on these lines is valid when accompanied by a Valid Address pulse.

2

FIGURE 3 - TYPICAL ULTRASONIC SYSTEM

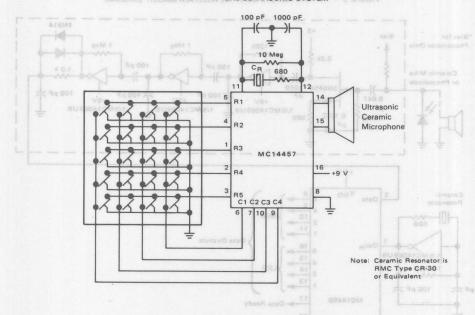


FIGURE 4 - TYPICAL INFRARED SYSTEM

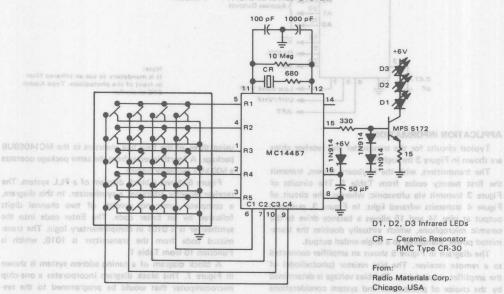
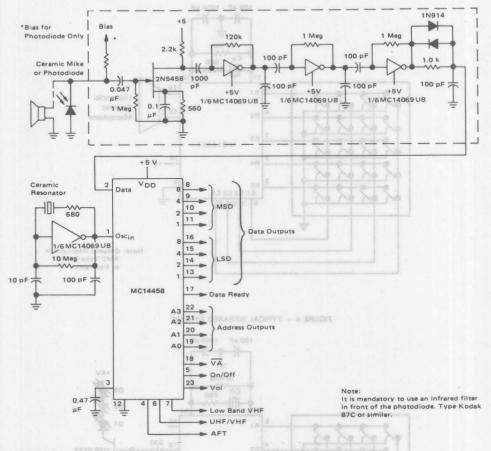


FIGURE 5 - TYPICAL REMOTE CONTROL RECEIVER CIRCUIT DIAGRAM



APPLICATION INFORMATION

Typical circuits for the transmitter and receiver chips are shown in Figure 3 through 8.

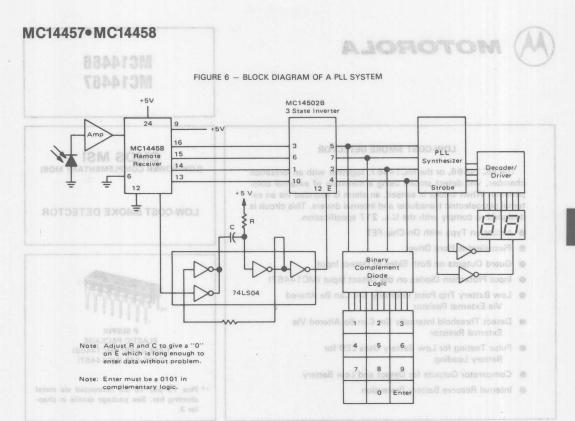
The transmitters, with the keyboard shown, transmit the first twenty codes from Table 1. The circuits of Figure 3 transmit via ultrasonic; whereas, the circuit of Figure 4 transmits infrared light. In Figure 3, push-pull output at pins 14 and 15 allows a balance drive to the ceramic microphone, which virtually doubles the transmitted power, compared to a single-ended output.

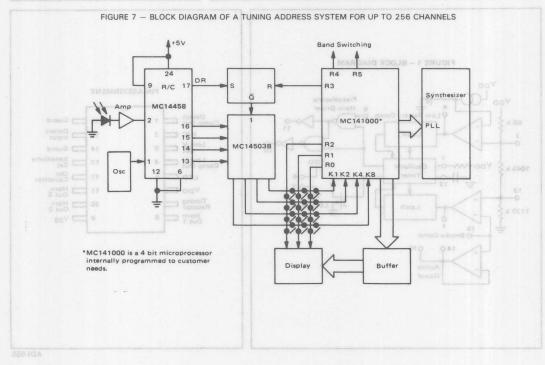
The diagram in Figure 5 shows an amplifier connected to a remote receiver. The bias resistor (photodiode) of the amplifier requires bias. The bias voltage is determined by the choice of photodiode and system considerations such as ambient light. Most of the required gain is realized

using three of the four hex inverters in the MC14069UB package. A fourth inverter from the same package operates a 500 kHz oscillator circuit.

Figure 6 shows a block diagram of a PLL system. The receiver directly addresses a synthesizer. In this diagram, a complete command consists of two channel digits followed by an Enter code. The Enter code into the synthesizer is a 0101 in complementary logic. The transmitted code from the transmitter is 1010, which is Function 10 from Table 1.

A block diagram of a tuning address system is shown in Figure 7. This block diagram incorporates a one-chip microcomputer that would be programmed to the system's needs. The system can be expanded up to 256 channels.





MC14466 MC14467

NUT44579 MIUT4458

LOW-COST SMOKE DETECTOR

The MC14466, or the MC14467, together with an ionization chamber, will detect smoke using a minimum of external components. When smoke is sensed, an alarm is sounded via an external piezoelectric transducer and internal drivers. This circuit is designed to comply with the U.L. 217 specification.

- Ionization Type with On-Chip FET
- Piezoelectric Horn Driver
- Guard Outputs on Both Sides of Detect Input
- Input Protection Diodes on the Detect Input (MC14467)
- Low Battery Trip Point Internally Set Can Be Altered Via External Resistor
- Detect Threshold Internally Set Can Be Altered Via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Outputs for Detect and Low Battery
- Internal Reserve Battery Protection

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

LOW-COST SMOKE DETECTOR



P SUFFIX
PLASTIC PACKAGE
CASE 648B* (MC14466)
CASE 648 (MC14467)

** Pins 15 and 16 are connected via metal shorting bar. See package details in chapter 3.

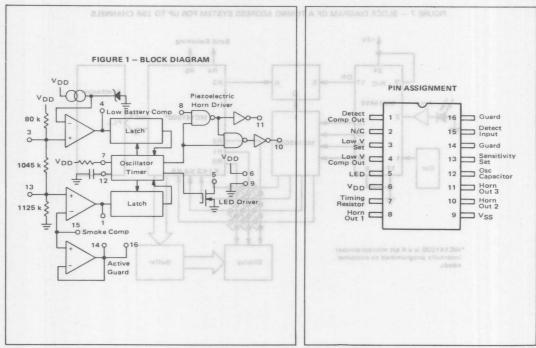


FIGURE 6 - BLOCK DIAGRAM OF A PLL SYSTEM

ADI-555

MAXIMUM RATINGS (Voltages referenced to VSS) 100 80 AT . SEC. AT .

Rating 447	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +15	Vdc	
Input Voltage, All Inputs	Vin	-0.25 to V _{DD} + 0.25	Vdc	
DC Current Drain per Input Pin	- 1	10	mAdd	
DC Current Drain per Output Pin	1	30	mAdd	
Operating Temperature Range	TA	0 to +50	°C	
Storage Temperature Range	T _{stg}	-55 to +125	°C	
Reverse Battery Time	tRB	5.0	S	

RECOMMENDED DC OPERATING CONDITIONS (Voltage referenced to VSS)

Parameter	Symbol	Value of ome	Unit
Supply Voltage	VDD	9.0	Vdc
Timing Capacitor		0.1	μF
Timing Resistor	ANANANA ANANA	8.2	MΩ
Battery Load (Resistor or LED)	_	10	mAdd

ELECTRICAL CHARACTERISTICS (TA = 25°C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Operating Voltage	VDD	D _ D	6.0	-	10 1000	Vdc
Output Voltage				1	- 09	Vdc
Piezoelectric Horn Drivers (IOH = 16 mA)	VOH	7.4	6.5		- webs	
Comparators (IOH = 0.1 mA)		9.0	8.5	8.8	-	
Piezoelectric Horn Drivers (IOL = -16 mA)	VOL	7.4	_	-	0.9	
Comparators (IOL = -0.1 mA)	When going	9.0	t si constatu	0.1	0.5	
Output Current — LED Driver (V _{OL} = 3.0 Vdc)		7.4	10	Comparero	-	mAdc
Operating Current (R _{Bias} = 8.2 M Ω)	IDD	9.0	-	5.0	9.0	μAdc
Input Current - Detect (40% R.H.)	lin	9.0	-	-	± 1.0	pAdc
Internal Set Voltage — Low Battery — Sensitivity	V _{Low} V _{Set}	9.0	7.4 47	- 50	8.0 53	Vdc % VDD
Hysteresis	VHys	9.0	75	100	150	mVdc
Offset Voltage Active Guard Detect Comparator	Vos	9.0	-	=	± 100 ± 50	mVdc

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

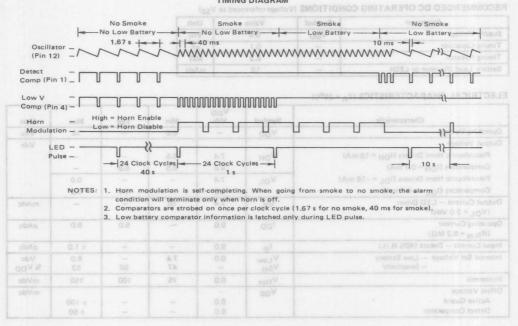
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

TIMING PARAMETERS (C = 0.1 μ F, R_{Rigs} = 8.2 M Ω , V_{DD} = 9.0 Vdc, T Δ = 25°C)

Characteristics		Value	Symbol	Min	Тур	Max	Units
Oscillator Period	Velc	No Smoke Smoke	†CI	1.34	1.67 40	2.0 48	s ms
Oscillator Pulse Width	NAME OF	OF OR	PWCI	8	10	12	ms
Horn Output (During Smoke)	mAdc	On Time Off Time	PW _{on} PW _{off}	1	200 40	Prain pile Duth	ms ms
LED Output	Be	tween Pulses On Time	tLED PWon	32 8	40 10	48 12	s ms
Horn Output (During Low Battery)	Be	On Time	t _{on}	8 32	10 40	12 48	ms s

2

TIMING DIAGRAM



This device contains circuitry to protect the inputs against dumage due to high static voltages or electric fields: however, it is advised that normal preceditions be taken to evoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

DEVICE OPERATION

TIMING

The internal oscillators of the MC14466 and the MC14467 operate with a period of 1.67 seconds during no-smoke conditions. Each 1.67 seconds, internal power is applied to the entire IC and a check is made for smoke. Every 24 clock cycles a check is made for low battery by comparing V_{DD} to an internal zener voltage. Since very small current are used in the oscillator, the oscillator capacitor should be of a low leakage type.

DETECT CIRCUITRY

If smoke is detected, the oscillator period becomes 40 ms and the piezoelectric horn oscillator circuit is enabled. The horn output is modulated 200 ms on, 40 ms off. During the off time, smoke is again checked and will inhibit further horn output if no smoke is sensed. During smoke conditions the low battery detection is inhibited, but the LED pulses at a 1.0 Hz rate.

An active guard is provided on both pins adjacent to the detect input. The voltage at these pins will be within 100 mV of the input signal. This will keep surface leakage currents to a minimum and provide a method of measuring the input voltage without loading the ionization chamber. The active guard op amp is not power strobed and thus gives constant protection from surface leakage currents. Pin 16 of the active guard is connected to pin 15 (the detect input) during shipping to protect pin 15 from static damage.

SENSITIVITY/LOW BATTERY THRESHOLDS

Both the sensitivity threshold and the low battery voltage levels are set internally by a common voltage divider connected between VDD and VSS. These voltages can be altered by external resistors connected from pins 3 or 13 to either VDD or VSS. There will be a slight interaction here due to the common voltage divider network.

TEST MODE

Since the internal op amps and comparators are power strobed, adjustments for sensitivity or low battery level could be difficult and/or time-consuming. By forcing pin 12 to VSS, the power strobing is bypassed and the outputs, pin 1 and 4, constantly show smoke/no smoke and good battery/low battery, respectively. Pin 1 = VDD for smoke and pin 4 = VDD for low battery. In this mode and during the 10 ms power strobe, chip current rises to approximately 50 μ A.

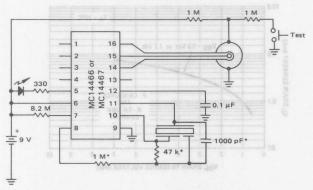
LED PULSE

The 9-volt battery level is checked every 40 seconds during the LED pulse. The battery is loaded via a 10 mA pulse for 10 ms. If the LED is not used, it should be replaced with an equivalent resistor such that the battery loading remains at 10 mA.

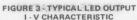
HYSTERESIS

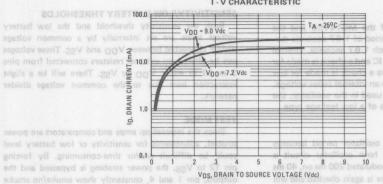
When smoke is detected, the resistor/divider network that sets sensitivity is altered to increase sensitivity. This yields approximately 100 mV of hysteresis and avoids false triggering.

FIGURE 2 - TYPICAL APPLICATION AS IONIZATION SMOKE DETECTOR



*NOTE: Component values may change depending on type of piezoelectric horn used.

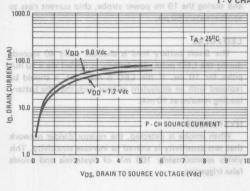




DETECT CIRCUITRY

40 ms and the piezoelectric lenabled. The horn output is mo

shom sirts of vietted wol not ggV = A FIGURE 4 - TYPICAL P HORN DRIVER OUTPUT ish you



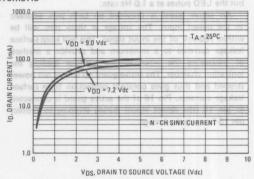
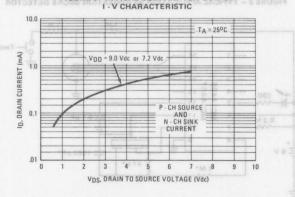


FIGURE 5 - TYPICAL COMPARATOR OUTPUT







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MOTORONA

(LOW-POWER COMPLEMENTARY MOS)

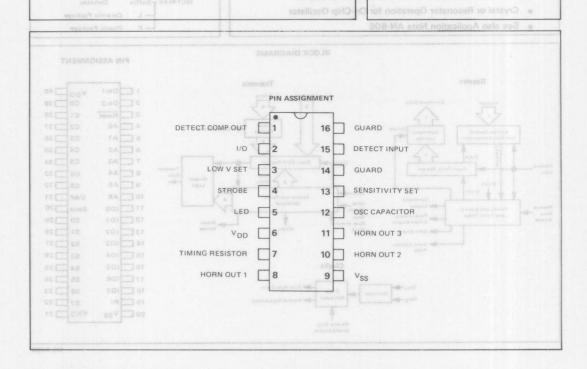
INTERCONNECT
SMOKE DETECTOR

INTERCONNECT SMOKE DETECTOR

- Ionisation Type with On-chip FET
- Piezoelectric Horn Driver On-chip
- Guard Outputs on Both Sides of Detect Input
- Input Protection Diodes on the Detect Input
- Low Battery Threshold, Internally Set, Can Be Altered via External Resistor
- Detect Threshold, Internally Set, Can Be Altered via External Resistor
- Pulse Testing for Low Battery Uses LED for Battery Loading
- Comparator Outputs for Detect
- Internal Reverse Battery Protection
- Strobe Output for External Trim Resistors
- I/O Pin Allows up to 40 Units to be Connected for Common Signalling
- Power-on-reset Prevents False Alarms on Battery Change

16

P SUFFIX
PLASTIC PACKAGE
CASE 648



MC14469

MOTOROL

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER

The MC14469 Addressable Asynchronous Receiver Transmitter is constructed with MOS P-channel and N-channel enhancement devices in a single monolithic structure (CMOS). The MC14469 receives one or two eleven-bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 will then transmit its information in two eleven-bitword data streams. Each of the transmitted words contains eight data bits, even parity bit, start and stop bit.

The received word contains seven address bits and the address of the MC14469 is set on seven pins. Thus 27 or 128 units can be interconnected in simplex or full duplex data transmission. In addition to the address received, seven command bits may be received for data or control use.

The MC14469 finds application in transmitting data from remote A-to-D converters, remote MPUs or remote digital transducers to the master computer or MPU.

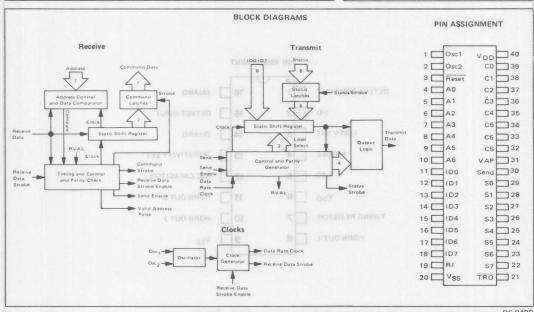
- Supply Voltage Range 4.5 Vdc to 18 Vdc
- Low Quiescent Current − 75 µAdc maximum @ 5 Vdc
- Data Rates to 9600 Baud
- Receive Serial to Parallel Transmit - Parallel to Serial
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator
- See also Application Note AN-806

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER





DS 9490

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 20.

	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +18		
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc	
DC Current Drain per Pin	1	10	mAdo	
Operating Temperature Range	E TA BE	-40 to +85	°C	
Storage Temperature Range	T _{stg}	-65 to +150	°C	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

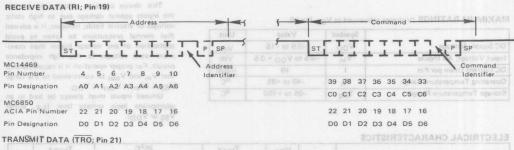
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS

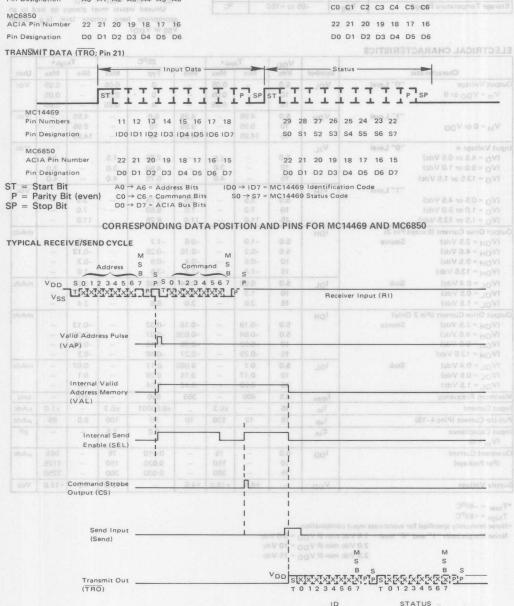
		,	Vpp	V _{DD} T _I			25°C		Thigh*		
Characteristic	Strie	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	J -	0.05	_	0	0.05	-	0.05	Vdc
Vin = VDD or 0		100	10	98-9	0.05	7.7	0	0.05	-	0.05	
	a da da da da d	and the	15	hamb a	0.05	- <u>d</u>	0	0.05		0.05	
V _{in} = 0 or V _{DD}	"1" Level	VOH	5.0	4.95	-	4.95	5.0		4.95	Number	Vdc
	77 07 -7 07	02 12 0	10	9.95	at VI	9.95	10	-	9.95	-	Table .
		ES 23 1	15	14.95	101 901	14.95	601 151 TOL	001_	14.95	Designal	1119
Input Voltage #	"0" Level	VIL								India	Vdc
$(V_0 = 4.5 \text{ or } 0.5 \text{ Vdc})$	16 17 16 16	20 19	5.0	-	a 1.5	18-17	2.25	1.5	interna	1.5	ba
$(V_0 = 9.0 \text{ or } 1.0 \text{ Vdc})$		1 02 03	10	-	3.0	Da Ds	4.50	3.0	- noi	3.0	Pie
(V _O = 13.5 or 1.5 Vdc)		00 50 T	15	-	4.0	00 00	6.75	4.0	-	4.0	
	"1" Level	VIH	MC14468	= 40H +=	IQ1	BITTE BITTE	NBBA = BA =	0.4		He TIST	Vdc
(V _O = 0.5 or 4.5 Vdc)	90	Brattins Co.	5.0	3.5	-	3.5	2.75	00 -	3.5	g Azue	
$(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$. 1911	10	7.0	-	7.0	5.50	00	7.0	tia_gat	8 = 5
(V _O = 1.5 or 13.5 Vdc)		NAME OF THE OWNER, OF THE OWNER,	15	11.0	vana v	11.0	8.25	anon	11.0	-	
Output Drive Current (Excep	ot Pin 2)	ГОН	DAME TO STATE	EN BUSEL	100, 12	THE PERSON NAMED IN	MUNIC 103	minor			mAd
(V _{OH} = 2.5 Vdc)	Source		5.0	-1.0	-	-0.8	-1.7	USTO 0	-0.6 V	BOSE .	PICAL
(V _{OH} = 4.6 Vdc)		No.	5.0	-0.2	NA -	-0.16	-0.35	-	-0.12	-	
(V _{OH} = 9.5 Vdc)			10	-0.5	8 -bon	-0.4	-0.9	see into	-0.3	-	
(V _{OH} = 13.5 Vdc)			15	-1.4	9,500	-1.2	-3.5		-1.0	-	
(V _{OL} = 0.4 Vdc)	Sink	IOL	5.0	0.52	647	0.44	0.88	8-4 B	0.36	oev	mAdo
$(V_{OL} = 0.5 \text{ Vdc})$		Rece	10	1.3		1.1	2.25	bdata	0.9	wo.V	
$(V_{OL} = 1.5 \text{ Vdc})$			15	3.6	-	3.0	8.8	-	2.4	-	
Output Drive Current (Pin 2	Only)	ГОН					1 1				mAde
$(V_{OH} = 2.5 \text{ Vdc})$	Source		5.0	-0.19	-	-0.16	-0.32	-	-0.13	-	
$(V_{OH} = 4.6 \text{ Vdc})$			5.0	-0.04	-	-0.035	-0.07	ight rif gar	-0.03	V -	
(V _{OH} = 9.5 Vdc)			10	-0.09	-	-0.08	-0.16	-	-0.06	(c) -	1 7 7
(V _{OH} = 13.5 Vdc)			15	-0.29	-	-0.27	-0.48	-	-0.2	-	
$(V_{OL} = 0.4 \text{ Vdc})$	Sink	IOL	5.0	0.1	-	0.085	0.17	-	0.07	-	mAd
$(V_{OL} = 0.5 \text{ Vdc})$			10	0.17	-	0.14	0.28	without	0.1	-	
(V _{OL} = 1.5 Vdc)			15	0.50	-	0.42	0.84	ĕ∐eV	0.0	-	
Maximum Frequency		fmax	4.5	400	_	365	550	-	310	-	kHz
Input Current		lin	15	_	±0.3	_	±0.00001	±0.3	-	±1.0	μAdd
Pull-Up Current (Pins 4-18)		lup	15	12	120	10	50	100	8.0	85	μAdd
Input Capacitance		Cin	-		T		5.0	7.5	aroT	-	pF
(V _{in} = 0)				- Lan	are the same of		- Lance	192) el	denil	100	
Quiescent Current	Y THE STREET	IDD	5.0	-	75	-	0.010	75	-	565	μAde
(Per Package)			10	-	150	-	0.020	150	-	1125	
			15		300	-	0.030	300	- 1	2250	
Supply Voltage		VDD	-	+4.5	+18.0	+4.5		+18.0	+4.5	+18.0	Vdc

^{*} T_{low} = -40°C Thigh = +85°C =Noise immunity specified for worst-case input combination. Noise Margin both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc



2



PIGURE 1 - DECILLATOR CIRCUIT | NOITARAGO BOIVAGE 2 - RECTIFIED POWER FROM DATA LINES CIRCUIT

OSCILLATOR (Osc1, Osc2; Pins 1, 2) — These pins are the oscillator input and output. (See Figure 1.)

RESET (Reset; Pin 3) — When this pin is pulled low, the circuit is reset and ready for operation.

ADDRESS (A0-A6; Pin 4, 5, 6, 7, 8, 9, 10) — These are the address setting pins which contain the address match for the received signal.

INPUT DATA (ID0-ID7; Pins 11, 12, 13, 14, 15, 16, 17, 18) — These pins contain the input data for the first eight bits of data to be transmitted.

RECEIVE INPUT (RI; Pin 19) — This is the receive input pin.

NEGATIVE POWER SUPPLY (V_{SS} ; Pin 20) — This pin is the negative power supply connection. Normally this pin is system ground.

TRANSMIT REGISTER OUTPUT SIGNAL (TRO; Pin 21) — This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

SECOND or STATUS INPUT DATA (S0-S7; Pins 22, 23, 24, 25, 26, 27, 28, 29) — These pins contain the input data for the second eight bits of data to be transmitted.

SEND (Send; Pin 30) — This pin accepts the send command after receipt of an address.

VALID ADDRESS PULSE (VAP; Pin 31) — This is the output for the valid address pulse upon receipt of a matched incoming address.

COMMAND STROBE (CS; Pin 32) — This is the output for the command strobe signifying a valid set of command data on pins 33-39.

COMMAND WORD (CO-C6; Pins 33, 34, 35, 36, 37, 38, 39) — These pins are the readout of the command word which is the second word of the received signal.

POSITIVE POWER SUPPLY ($V_{\rm DD}$; Pin 40) — This pin is the package positive power supply pin.

OPERATING CHARACTERISTICS

The receipt of a start bit on the Receive Input (R1) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (AO-A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word "1" or a command word "0". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address compared, a Valid Address Pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit and a stop bit. The eight data bits are composed of a seven-bit command, and a "O" which indicates a command word. At the end of the command word a Command Strobe Pulse (CS) occurs.

A positive transition on the Send input initiates the transmit sequence. Send must occur within 7 bit times of CS. Again the transmitted data is made up of two eleven-bit words, i.e., address and command words. The data portion of the first word is made up from Input Data inputs (IDO-1D7), and the data for the second word from Second Input Data (SO-57) inputs. The data on inputs 1D0-1D7 is latched one clock before the falling edge of the start bit. The data on inputs SO-S7 is latched on the rising edge of the start bit. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines. TRO begins either 1/2 or 11/2 bit times after Send, depending where Send occurs.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. Pin 1 may be driven from an external oscillator. See Figure 1.

FIGURE 1 - OSCILLATOR CIRCUIT MOTA MESSO STIFFIED POWER FROM DATA LINES CIRCUIT

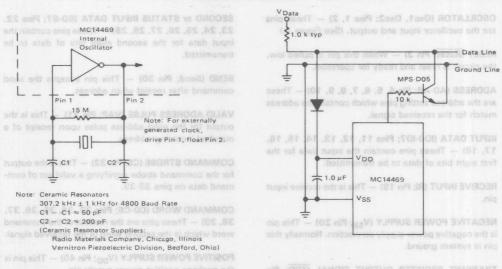
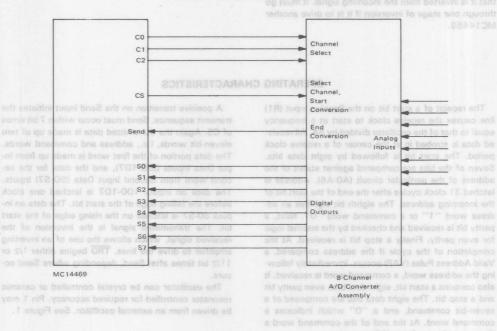
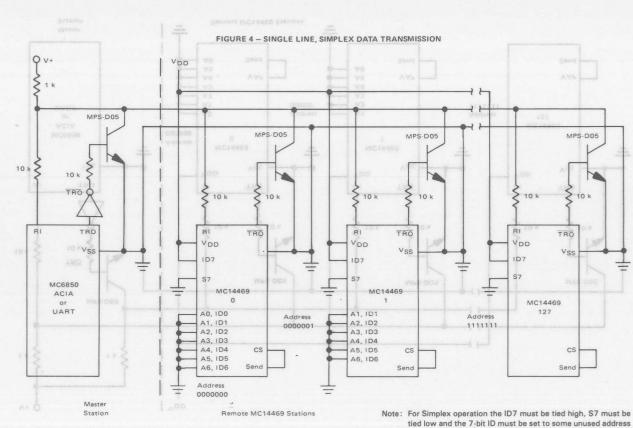
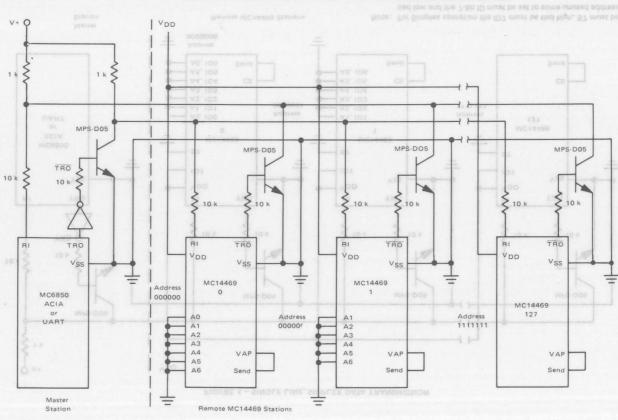


FIGURE 3 - A-D CONVERTER INTERFACE

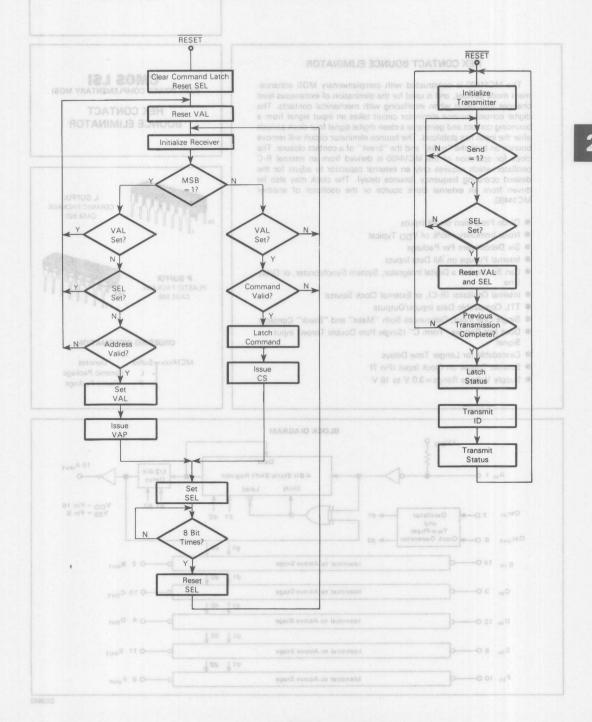






MC14490

FIGURE 6 - FLOW CHART OF MC14469 OPERATION





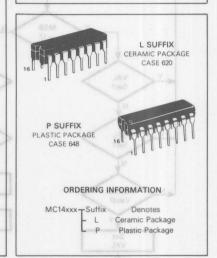
HEX CONTACT BOUNCE ELIMINATOR

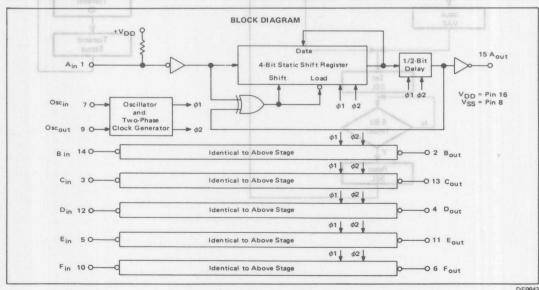
The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V

CMOS LSI (LOW-POWER COMPLEMENTARY MOS)

> **HEX CONTACT BOUNCE ELIMINATOR**





DS9843

MAXIMUM RATINGS (Voltages referenced to VSS, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	morte:	V _{DD}	-0.5 to +18	٧
Input Voltage, All Inputs	ur!	V _{in}	-0.5 to V _{DD} +0.5	٧
DC Current Drain per Input Pin		- 1	10	mA
Operating Temperature Range	MC14490L MC14490P	TA	- 55 to + 125 - 40 to + 85	°C
Storage Temperature Range		T _{stg}	-65 to +150	°C

ERIST	IN ASS	IGNMEN	SWIT
1 🖂	Ain	VDD	— 16
2 🗀	Bout	Aout	15
3 🖂	Cin	Bin	14
4 🖂	Dout	Cout	13
5 🖂	Ein	Din	12
6 🖂	Fout	Eout	-11
7 🖂	Oscin	Fin	10
8 🖂	VSS	Oscout	9

ELECTRICAL CHARACTERISTICS

	Chara	cteristic		Symbol	VDD	Tlo	w*		25°C		Thigh*		
- 95 190 ns	15	Dionotio		O y III DOI	Vdc	Min	Max	Min	Тур	Max	Min	Max	Uni
Output Voltage	6.0	High	"0" Level		5.0	-	0.05	-	0	0.05	-	0.05	
$V_{in} = V_{DD}$ or 0				VOL	10	-	0.05	-	0	0.05	-	0.05	V
- 120 240				0.2	15	-	0.05	-	0	0.05	-	0.05	
			"1" Level	-	5.0	4.95	-	4.95	5.0	G 300	4.95	Freque	Yan Pa
V _{in} = 0 or V _{DD}			1 20101	VOH	10	9.95	_	9.95	10	2 01.00	9.95	Isman	V
- O OI VDD				VOH	15	14.95		14.95	15	_	14.95	10011100	27.
Input Voltage #	1	-	"0" Level			71.00	-	11.00	10				
(V _O = 4.5 or 0.5 V)			O Level		5.0	_	1.5	-	2.25	1.5	(See F	1.5	
$(V_0 = 9.0 \text{ or } 1.0 \text{ V})$				VIL	10		3.0		4.50	3.0		3.0	V
$(V_0 = 13.5 \text{ or } 1.5 \text{ V})$					15		4.0	_	6.75	4.0		4.0	
(V) = 13.5 (1 1.5 V)					15	_	4.0	_	0.75	4.0	SOTETY	4.0	nest.
No Limit ns			"1" Level					7		9/	NT HE	bns s	
$(V_0 = 0.5 \text{ or } 4.5 \text{ V})$				VIH	5.0	3.5	-	3.5	2.75	-	3.5	тотвій	V
$(V_0 = 1.0 \text{ or } 9.0 \text{ V})$				-111	10	7.0	-	7.0	5.50	- V	7.0	7 Total	Bodi
$(V_0 = 1.5 \text{ or } 13.5 \text{ V})$	6.0:	20			15	11.0	-	11.0	8.25	-	11.0	-0	0.5
Output Drive Current									9,	f.0 of	An DOL	= Txa	
Source								0.00				100	
Oscillator Output							1						
$(V_{OH} = 2.5 V)$					5.0	-0.6	-	-0.5	- 1.5	-	-0.4	-	
$(V_{OH} = 4.6 V)$					5.0	-0.12	-	-0.1	-0.3	-	-0.08	-	
$(V_{OH} = 9.5 V)$				la	10	-0.23	-	-0.20	-0.8	-	-0.16	-	m/
$(V_{OH} = 13.5 V)$				ЮН	15	-1.4	-	-1.2	-3.0	-	-1.0	-	mA
Debounce Outputs								-					
$(V_{OH} = 2.5 V)$				no etua	5.0	-0.9	01 01	-0.75	-2.2	0.17500	-0.6	10 Total	
$(V_{OH} = 4.6 \text{ V})$				nanity of	5.0	-0.19		-0.16	-0.46	-	-0.12	T. T.	
$(V_{OH} = 9.5 V)$				Suduni	10	-0.60		-0.50	-1.2	II TIEN	-0.4	CELLISE	
$(V_{OH} = 13.5 \text{ V})$				99060	15	-1.8	m 01	-1.5	-4.5	DBJ THE	-1.2	n <u>n</u> sn	
Sink					SA 6	1773 7 1	F12 (01	Catility	denu	a out	DOAG	THE CIT	
Oscillator Output				stsinger	dde u	s os b	ait so	sysw	46 18	um as	uqni b	อะเกา	3
$(V_{OI} = 0.4 \text{ V})$					5.0	0.36	-	0.30	0.9	-	0.24	-	-
$(V_{OL} = 0.5 \text{ V})$				17.7	10	0.9	-	0.75	2.3	-	0.6	-	
$(V_{OL} = 1.5 \text{ V})$				IOL	15	4.2	-	3.5	10	-	2.8	-	m
Debounce Outputs				0.2	-00.000		A Property	e make		0 100	inches.	1 200	100.10
$(V_{OL} = 0.4 \text{ V})$		A - S BRU			5.0	2.6	W Bitt	2.2	4.0	CAL S	1.8	1.3R	UDI
$(V_{OI} = 0.5 \text{ V})$					10	4.0	_	3.3	9	-	2.7	-	
					15	12	_	10	35	Torna	6.4	-	.0
$(V_{OL} = 1.5 \text{ V})$								1		-	1		-
(V _{OL} = 1.5 V)					1	A Chambre							
Input Current	i = VDD)		Ιн	15	0	2	-	0.2	2	J= 1	11	μA
	-		000 8		15 15	()	and the state of	-	0.2	4 14	J= 14	± 250	
Input Current Debounce Inputs (VI) Input Current Oscillator	- Pin 7		000 B	l _{IH}	15	-	± 620	-	± 255	± 400	-	± 250	
Input Current Debounce Inputs (V _{II}) Input Current Oscillator Pullup Resistor Source (- Pin 7		000 2	l _{in}	15	210	± 620	- 140	± 255	± 400	70	± 250	PμA
Input Current Debounce Inputs (V _{II} - Input Current Oscillator Pullup Resistor Source (Debounce Inputs	- Pin 7		053 760 053 760 050 050 050 050 050 050 050 050 050 0		15 5.0 10	210 415	± 620 375 740	- 140 280	± 255 190 380	± 400 255 500	- 70 145	± 250 130 265	AμA
Input Current Debounce Inputs (V _{II} - Input Current Oscillator Pullup Resistor Source (Debounce Inputs (V _{II} = V _{SS})	- Pin 7 Current		000 2	l _{in}	15	210	± 620	- 140	± 255 190 380 570	± 400 255 500 750	70	± 250	μA
Input Current Debounce Inputs (VI) Input Current Oscillator Pullup Resistor Source (Debounce Inputs (VIL = VSS) Input Capacitance (VIn =	- Pin 7 Current		053 760 053 760 050 050 050 050 050 050 050 050 050 0	l _{in}	15 5.0 10 15	210 415 610	± 620 375 740 1100	- 140 280 415	± 255 190 380 570 5.0	± 400 255 500 750 7.5	70 145 215	± 250 130 265 400	μΑ μΑ pF
Input Current Debounce Inputs (V _{II} - Input Current Oscillator Pullup Resistor Source (Debounce Inputs (V _{II} = V _{SS})	- Pin 7 Current		053 760 053 760 050 050 050 050 050 050 050 050 050 0	l _{in}	15 5.0 10 15	210 415 610	± 620 375 740 1100	- 140 280 415	± 255 190 380 570	± 400 255 500 750	70 145 215	± 250 130 265 400	μA

//Noise immunity specified for worst case combination. Noise margin for both ''1'' and ''0'' level = 1.0 V min @ $V_{DD} = 5.0$ V 2.0 V min @ $V_{DD} = 10$ V 2.5 V min @ $V_{DD} = 15$ V

*T_{low} = -55°C for L Device, -40° C for P Device. Thigh = +125°C for L Device, +85°C for P Device.

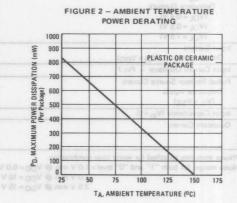
SWITCHING	CHARAC	TERISTICSC	I = 50 pF	$T_A = 25^{\circ}C$

V00		= 1		Chara	acteristi	ic	Value 0.5 to + 18	Symbol – Vap – 1	-	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time	Bout	2 0				V	018.0-				5.0	-	180	360	
All Outputs		bis 8					8.0+00			TLH	10	sındu	90	180	ns
1000	- 0				17	ken.	10				15	orT to	65	130	530
Output Fall Time	- 3									10	apra	Renut	nsane	Tonite	Open
Oscillator Outpu	1									0.	5.0	-	100	200	
		Po						- 01sT		-	10	aff on	50	100	Ston
		PI								THL	15	-	40	80	ns
Debounce Outp	uts	E P									5.0	-	60	120	
											15	=	20	40	
Propagation Delay	Time									tPHL	191831	CRAC	SET 1	VOID.	DBU
Oscillator Input		ounce	Output	S						1100	5.0		285	570	000
										altahota	100	-	120	240	
Win Wax											15	-	95	190	ns
80.0 -										tPLH	5.0	-	370	740	Dutt
A 90:00 -						01					10	-	160	320	V
d0.0 -	80.0	0	_	0.05	1 -	91					15	-	120	240	
Clock Frequency (level "I			5.0	-	2.8	1.4	
(External Clock)			9.95							fcl	10	-	6	3.0	MH
- (8.6)		1	06.40		14,35	16					15	-	9	4.5	
Setup Time (See F	igure							layed 0			5.0	100	50	REPA	ugat
- 15 v		2.25								tsu	10	80	40	B.A.m.C	ns
				0.8		OI.					15	60	30	0.8=0	
Maximum External		Input									5.0	Frank			
Rise and Fall Tir	ne									tr, tf	10		No Lim		ns
Oscillator Input		00.0	0.7		1 0.1	UI	100/				15				100
Oscillator Frequence	СУ									fosc, typ	5.0		1.5		VI.
OSC _{out} C _{ext} = 500 pF	to 0.1											Ce	ext (in)	μF)	btu O
Cext = 300 pr	10 0.1	μι									10	_	4.5	2000	Hz
													ext (in		
- 0.0-											15		6.5		
- 60.0-	-	E.0-			-0.12	5.0						Ce	ext (in)	uF)	
Am - 101.0-	-	8.0-	US. 0 -		EE 0 -	Qf	The state of					(4	d.t =	HOVI	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 - TYPICAL SWITCHING TIME WAVEFORMS VDD Oscin -0 V tPLH-VDD Aout 50% 10% -0 V H TPHL VD Aout 10% -0 V -VDD Oscin 50%

50%



0 V

VDD

-() V

THEORY OF OPERATION - A BRUDIA

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 41/2-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open the shift register is loaded with a 1 (positive logic assumed) on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with 1's and the output is at a 1 or high level.

At clock edge 1 (Figure 3) the input has gone low and a 0 (low level) has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1 the input signal has bounced back to a logic 1. This causes the shift register to be reset to all 1's in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus a logic 0 has been shifted into all four shift register bits and, as shown, the output goes to a 0 during the positive edge of clock pulse 6.

It should be noted that there is a $3\frac{1}{2}$ to $4\frac{1}{2}$ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

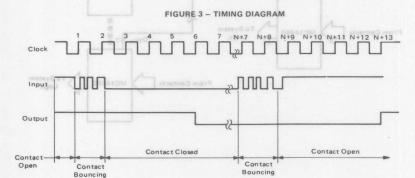
After some time period of N clock periods, the contact is opened and at N+7 a 1 is loaded into the first bit. Just after N+7, when the input bounces low, all bits are reset to 0. At N+8 nothing happens because the input and output are low and all bits of the shift register are 0. At time N+9 and thereafter the input signal is a high (1) clean signal. At N+13 the output goes high (1) as a result of four 1's being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

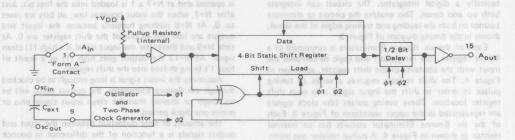
The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if you include the leading edge bounce in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.



2-85



sell on verses a cover support of the bound promote programme of the progr

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between VDD and the input.

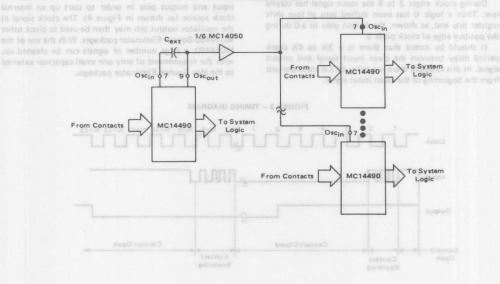
Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when VDD is below 5 V. At this voltage, the input should be driven with

paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When VDD is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

STATE OF STA

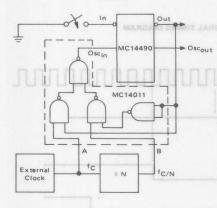


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

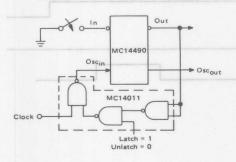
FIGURE 6 – FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 - LATCHED OUTPUT CIRCUIT

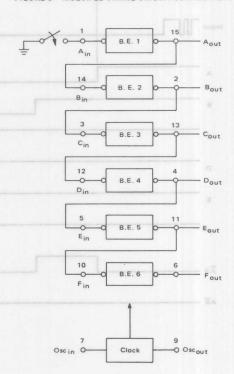


MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

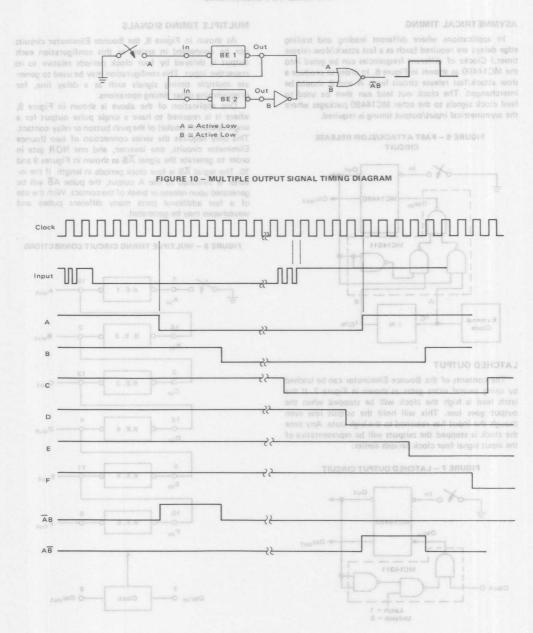
One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $\overline{A}B$ as shown in Figures 9 and 10. The signal $\overline{A}B$ is four clock periods in length. If the inverter is switched to the A output, the pulse $\overline{A}B$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 - MULTIPLE TIMING CIRCUIT CONNECTIONS



2

FIGURE 9 - SINGLE PULSE OUTPUT CIRCUIT



WC144930 MC144940 MC144.95



BINARY-TO-SEVEN SEGMENT LATCH/DECODER/DRIVERS

The MC14493, MC14494 and MC14495 are all constructed with CMOS enhancement mode devices and NPN bipolar output drivers on a single monolithic structure. Internal series resistors of typically 290 ohms allow the parts to interface directly with seven segment common cathode LED displays at 5 volt supply.

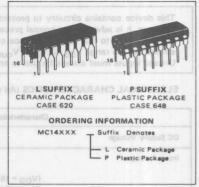
Applications include MPU systems, TV displays and general purpose displays.

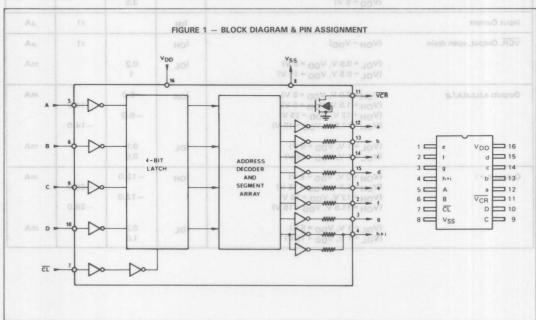
- MC14493 binary plus one decoding for 11/2-digits
- MC14494 binary decoding for 1½-digits
- MC14495 binary to hexadecimal decoding
- · VCR output activated when 16 or F is displayed
- · High-current sourcing outputs with internal limiting resistance
- Internal input level shift
- Supply voltage range 4.5 to 18 Vdc

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY-TO-SEVEN SEGMENT LATCH/DECODER/DRIVERS





Rating		Symbol	Value	Unit
DC Supply Voltage		V _{DD}	-0.5 V to +18	Vdc
Input Voltage, all Inputs		VIN	-0.5 V to V _{DD} + 0.5	Vd _c
DC Current Drain per Input		1	10	mA
Dissipation per Output Driver Pins 1, 2, 3, 12, 13, 14, 15 Pin 4		РОН	50 100	
Operating Temperature Range	rbnw	Do TA ano	Na ana 3840 to +70 na 484413	M . CAAT
Storage Temperature Range	lvers	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (All voltages referenced to V_{SS} = 0, T_A = 25°C)

DERING INFORMATION	Characteristics	Symbol	Min.	Max.	Unit
DC Supply Voltage	MC163	V _{DD}	4.5	agetine yigh	v Sur
Input Voltage		VIL		0.8	V
	(V _{DD} = 15 V) (V _{DD} = 5 V)	VIH	4 3.5		V
Input Current	- BLOCK DIAGRAM & PW ASSIGNMENT	IIN		±1	μΑ
VCR, Output, open drain	(V _{OH} = V _{DD})	ГОН		±1	μΑ
	(V _{OL} = 0.5 V, V _{DD} = 5 V) (V _{OL} = 0.5 V, V _{DD} = 15 V)	IOL	0.2		mA
Outputs a,b,c,d,e,f,g	(V _{OH} = 2.0 V, V _{DD} = 5 V) (V _{OH} = 1.5 V, V _{DD} = 5 V) (V _{OH} = 12 V, V _{DD} = 15 V) (V _{OH} = 11.5 V, V _{DD} = 15 V)	Іон	-6.0 -6.0	-14.0 -14.0	mA
er C o o o o o	(V _{OL} = 1 V, V _{DD} = 5 V) (V _{OL} = 1 V, V _{DD} = 15 V)	IOL	0.1 0.5	<	■ mA
Output h + i	(V _{OH} = 2 V, V _{DD} = 5 V) (V _{OH} = 1.5 V, V _{DD} = 15 V) (V _{OH} = 12 V, V _{DD} = 15 V) (V _{OH} = 11.5 V, V _{DD} = 15 V)	ГОН	-12.0 -12.0	-28.0 -28.0	mA
e = 0	(V _{OL} = 1 V, V _{DD} = 5 V) (V _{OL} = 1 V, V _{DD} = 15 V)	IOL	0.2	<\	mA

MC14493 • MC14494 • MC14495

SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

		V _{DD}	VAJSŽIG	a heil VCH	8 B 2 d 6	A B A
Characteristic	Symbol	Vdc	Min	Тур	Max	Unit
Propagation Delay Times — \$ 3.3847	TPLH	5.0 10 15	2 2 3	1.20 0.45 0.27	2.50 0.90 0.55	μs
MC14495	T _{PHL}	5.0 10 15	÷ ÷ ÷	750 235 135	1500 o r 470 o r 270	μs
Output Rise Time	STILH	5.0 10 15	<u>8</u> <u>8</u>	500 345 250	1000 700 500	ns
Output Fall Time	T _{THL}	5.0 10 15		130 40 27	260 80 55	o o t
Clock Pulse Width	tWH	5.0 10 15	2.4 0.70 0.55	1.2 0.35 0.27		

INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h, i; Pins 1, 2, 3, 4, 12, 13, 14, 15).

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of $V_{DD} = 5.0 \text{ volts}$.

OUTPUT VCR (Pin 11)

This output is activated (goes to low) whenever the address corresponding to program 16 is selected. Otherwise the output is open. See the truth table.

INPUT LATCH (A, B, C, D; Pins 5, 6, 8, 10)

The block diagram is shown on page 1. The inputs A, B, C and D are fed to a 4-bit latch which is controlled by clock (CL). Two modes of operation are available.

CLOCK (CL; Pin 7)

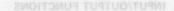
The data on the inputs A, B, C aNd D will pass through the latch and will be displayed immediately when the clock is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when CL = low and will be latched with the rising edge of CL. The data will remain stored as long as CL is high.

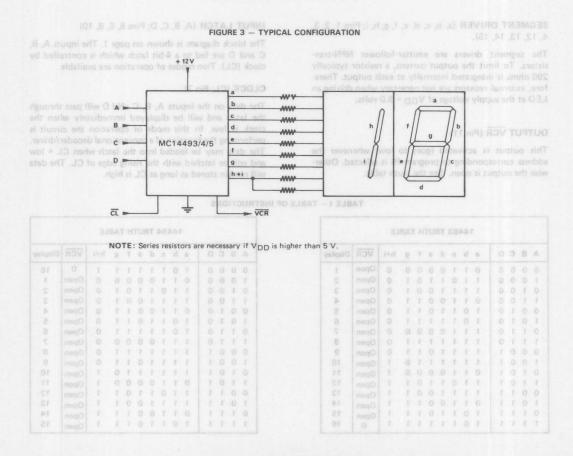
TABLE 1 - TABLE OF INSTRUCTIONS

													.3/ 3
A	В	C	D	a	b	C	d	е	f	g	h+i	VCR	Display
0	0	0	0	0	1	1	0	0	0	0	0	Open	1
1	0	0	0	1	1	0	1	1	0	1	0	Open	2
0	1	0	0	1	1	1	1	0	0	1	0	Open	3
1	1	0	0	0	1	1	0	0	1	1	0	Open	4
0	0	1	0	1	0	1	1	0	1	1	0	Open	5
1	0	1	0	1	0	1	1	1	1	1	0	Open	6
0	1	1	0	1	1	1	0	0	0	0	0	Open	7
1	1	1	0	1	1	1	1	1	1	1	0	Open	8
0	0	0	1	1	1	1	1	0	1	1	0	Open	9
1	0	0	1	1	1	1	1	1	1	0	1	Open	10
0	1	0	1	0	1	1	0	0	0	0	1	Open	11
1	1	0	1	1	1	0	1	1	0	1	1	Open	12
0	0	1	1	1	1	1	1	0	0	1	1	Open	13
1	0	1	1	0	1	1	0	0	1	1	1	Open	14
0	1	1	1	1	0	1	1	0	1	1	1	Open	15
1	1	1	1	1	0	1	1	1	1	1	1	0	16

A	В	C	D	а	b	c	d	0	f	g	h+i	VCR	Display
0	0	0	0	1	0	1	1	1	1	1	1	0	16
1	0	0	0	0	1	1	0	0	0	0	0	Open	-1
0	1	0	0	1	1	0	1	1	0	1	0	Open	2
1	1	0	0	1	1	1	1	0	0	1	0	Open	3
0	0	1	0	0	1	1	0	0	1	1	0	Open	4
1	0	1	0	1	0	1	1	0	1	1	0	Open	5
0	1	1	0	1	0	1	1	1	1	1	0	Open	6
1	1	1	0	1	1	1	0	0	0	0	0	Open	7
0	0	0	1	1	1	1	1	1	1	1	0	Open	8
1	0	0	1	1	1	1	1	0	1	1	0	Open	9
0	1	0	1	1	1	1	1	1	1	0	1	Open	10
1	1	0	1	0	1	1	0	0	0	0	1	Open	11
0	0	1	1	1	1	0	1	1	0	1	1	Open	12
1	0	1	1	1	1	1	1	0	0	1	1	Open	13
0	1	1	1	0	1	1	0	0	1	1	1	Open	14
1	1	1	1	1	0	1	1	0	1	1	1	Open	15

				PUTS	TUC	(3	UTS	INF	
		DISPLAY	VCR	h+i	g	f	е	d	С	b	а	A	В	С	D
		0	Open	0	0	1	1	1	1	1	1	0	0	0	0
		1	Open	0	0	0	0	0	1	1	0	1	0	0	0
		2	Open	0	1	0	1	1	0	1	1	0	.1	0	0
TABLE 2 -		3	Open	0	1	0	0	1	1	1	1	1	1	0	0
		4	Open	0	1	-1	0	0	1	1	0	0	0	-1	0
MC14495		5	Open	0	1	1	0	1	108	0	1	1	0	1	0
		6	Open	0	1	1	1	1	1	0	1	0	1	1	0
LPHANUMERIC DISPLAY	AL	7	Open	0	0	0	0	0	1	1	1	1	1	1	0
Lucial platatological plata		8	Open	0	1	1	1	1	1	1	1	0	0	0	1
1456789866888	8 183	8 9 A	Open	0	1	1	0	1	1	1	1	1	0	0	1
4 5 6 7 8 9 10 11 12 13 14 15	0 1 2 3	A	Open	1	1	1	1	0	1	1	1	0	1	0	1
		b	Open	1	1	1	1	1	1	0	0	1	1	0	1
Nitput Fali Time		С	Open	161	0	1	1	1	0	0	1	0	0	1	1
		d	Open	1	1	0	1	1	108	1	0	1	0	1	1
		E	Open	100	1	1	1	1	0	0	1	0	1	1	1
		F	0	1	1	1	1	0	0	0	1	1	1	1	1
			2.4 1.2 -												







MC14495-1

Advance Information

HEXADECIMAL-TO-SEVEN SEGMENT LATCH/ DECODER/DRIVER

The MC14495-1 hexadecimal-to-seven segment latch/decoder/driver is constructed with CMOS enhancement-mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch. With a 5-volt power supply, it can be used without resistor interface to drive seven segment LED displays. The series output resistors of, typically, 290 ohms are internal to the device.

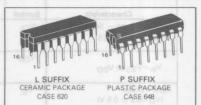
Applications include MPU systems display driver, instrument display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic-Circuit Power Dissipation
- High Current-Sourcing Outputs With Internal Limiting Resistors
- Latch Storage of Code
- Supply Voltage Range = 4.5 V to 18 V
- CMOS Input Switching Levels

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

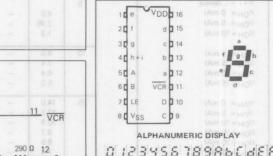
HEXADECIMAL-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



ORDERING INFORMATION

MC14XXX Suffix Denotes

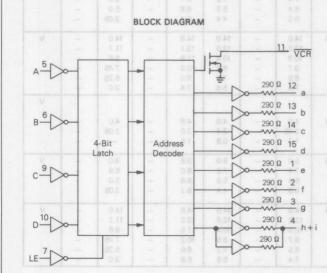
L1 Ceramic Package
P1 Plastic Package



0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

1	NP	UT	S		OUTPUTS - HOL										
D	С	В	A	a	b	c	d	e	f	g	h+i	VCR	DISPLAY		
0	0	0	0	1	1	1	1	1	1	0	0	Open	0		
0	0	0	1	0	1	1	0	0	0	0	0	Open	1		
0	0	1	0	1	1	0	1	1	0	1	0	Open	2		
0	0	1	1	1	1	1	1	0	0	1	0	Open	3		
0	1	0	0	0	1	1	0	0	1	1	0	Open	4		
0	1	0	1	1	0	1	1	0	1	1	0	Open	5		
0	1	1	0	1	0	1	1	1	1	1	0	Open	6		
0	1	1	1	1	1	1	0	0	0	0	0	Open	7		
1	0	0	0	1	1	1	1	1	1	1	0	Open	8		
1	0	0	1	1	1	1	1	0	1	1	0	Open	9		
1	0	1	0	1	1	1	0	1	1	1	in a	Open	A		
1	0	1	1	0	0	1	1	1	1	1	1	Open	ь		
1	1	0	0	1	0	0	1	1	1	0	Alm a	Open	C		
1	1	0	1	0	1	1	1	1	0	1	1	Open	d		
1	1	1	0	1	0	0	1	1	1	1	1	Open	E		
1	1	1	1	1	0	0	0	1	1	1	1	0	F		

ADI-484R1



Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to + 18	V
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	V
DC Current Drain per Input Pin	E	10	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to + 150	°C
Maximum Continuous Output Power (Source) per Output @ 25°C Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	POHmax [‡]	50 HOTA	Wm SMENT L

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high inpedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out})$ HEXADECIMAL DOV SEN SE

		VDD	Man Tie	ow*	b abom-	25°C	erina 20	This	gh [*]	s cons
Characteristic	Symbol	V	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage - Segments	VOL	5	supply,	0.1	v-d Entily	0 8 9	0.05	A B To an	0.05	VIS
Vin = VDD or VSS	·OL	10	GEL TO	0.1	drive sev	0	0.05	er tworth	0.05	d nap I
-111 -00 5. 133		15	lanasini	0.1	085_ylls	0	0.05	ugtuo se	0.05	sysiqait
2 1 1 1 2 2 2 2 1 1 1 1 1	Vон	5	4.1	_	4.1	4.65		4.1	. <u>9</u> :0 y s	V
Vin=VSS or VDD	·UH	10	9.1	mercunta	9.1	9.6	etsys U	9.1	ni engire	Apple
XIGHTS 4 XIGHT		15	14.1	Hib walge	14.1	14.5	leigeb re	14.1	etuarro:	neviti
Input Voltage	VIL					.86	Su 19mil U	ans ,don	clock, w	V
(V _O = 3.8 or 0.5 V)	NO VIL	5	102	1.5		2.25	1.5	reult Pov	1.5	wo.J 6
(Vo=88 or 10 V)		10	41012	3.0	mi.) lema	4.50	3.0	Sourcine		tgiH 8
$(V_0 = 13.8 \text{ or } 1.5 \text{ V})$		15	_	4.0	_	6.00	4.0	baOHa a	4.0	nsl e
	11	-	3.5		3.5	2.75	V & X =	3.5	stlo¥ vla	100000000000000000000000000000000000000
$(V_0 = 0.5 \text{ or } 3.8V)$	VIH	5	7.0		7.0	1-000				
(V _O = 1.0 or 8.8 V)		10	11.0		11.0	5.50 8.25	distred g	7.0	DS Imput	MD 4
$(V_0 = 1.5 \text{ or } 13.8 \text{ V})$		15	11.0	-	11.0	8.25		11.0		
Output Drive Voltage - Segments,	VOH									V
h+i - L device		5								
(I _{OH} = 0 mA)			4.0	-	4.0	4.8	-	4.0	-	
(I _{OH} = 5 mA)			2.45	-	2.4	3.0	· -	2.05	-	
(I _{OH} = 10 mA)			1.3		0.8	1.8	-	-	-	
(I _{OH} = 0 mA)		10	9.0		9.0	9.8	_	9.0		V
(IOH = 5 mA)		10	7.4		7.2	8.1		6.9		
(I _{OH} = 10 mA)			6.4		5.8	6.8		5.0		
15 45			5.3		4.4	5.4		3.05		
(IOH = 15 mA)			0.0		7.4	MAY TAIL	BLOCK	3.00		
(IOH = 0 mA) or do		15	14.0	-	14.0	14.8	-	14.0	_	V
(I _{OH} = 5 mA)			12.2		12.0	13.1	-	11.7	_	
(I _{OH} = 10 mA)		T.	10.9	-	10.4	11.8	-	9.6		-
(I _{OH} = 15 mA)			9.7	_	8.8	10.5	-	7.45	4	12,
(I _{OH} = 20 mA)			8.5	-	7.2	9.0	- 1	5.25	10	N.
(I _{OH} = 25 mA)			7.4	062	5.6	7.4	-	3.0	-	
Output Drive Voltage - Segments,	VOH			con	V					V
h+i - P device	OIT		2 13 b	AAA	1		1			
(I _{OH} = 0 mA)		5	4.0	000-	4.0	4.8	- 100	4.0		5
(I _{OH} = 5 mA)			2.45	///OC	2.4	3.0	-	2.05	+	W
(I _{OH} = 10 mA)		1-1-1	1.3	092-	0.8	1.6	BA-	-184	-	
1 1 1 1 1 0 0 Open			b	W-00		- tebe	100 P	riote		
$(I_{OH} = 0 \text{ mA})$		10	9.0	- 290	9.0	9.8	-	9.0	10	V
$(I_{OH} = 5 \text{ mA})$			7.4	nov00	7.2	8.0	- 14	6.9	1-0	(1
(I _{OH} = 10 mA)			6.4	299	5.8	6.6	-	5.0		1
(I _{OH} = 15 mA)		I LAN	5.3	non	4.4	5.2		3.05	+	
(I _{OH} = 0 mA)		15	14.0	WW-00	14.0	14.8		14.0		V
(I _{OH} = 5 mA)			12.2	280	12.0	13.0		11.7	1	101
(I _{OH} = 10 mA)		1	10.9	///OX	10.4	11.6		9.6	1-0	5-0
(I _{OH} = 15 mA)			9.7	290	8.8	10.2		7.45		
(I _{OH} = 20 mA)			8.5	W00	7.2	8.6		5.25		
			7.4		1.00	6.8		3.0		

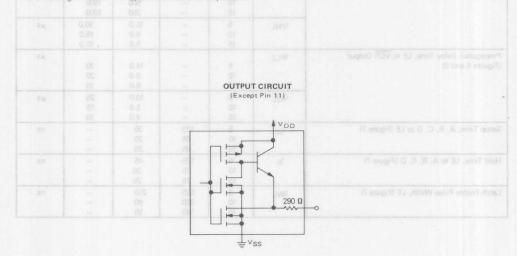
⁺ POHmax = IOH (VDD-VOH)

FI	FCTRICAL	CHARACTERISTICS	(Continued)

			VDD	-4	0°C		25°C		85	°C	
Characteristic	Typ	Symbol	V	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Sink Current-VCR outp	ut-	IOL			HJT		(f -stup)	hi studini	Legment 4	iso Time,	mA
L device	210										
$(V_{OL} = 0.4 \ V)$	2014		5		-	0.3	1.00	-		-	
$(V_{OL} = 0.5 V)$	-06		10		-			-		-	
$(V_{OL} = 1.5 V)$			15		THOS	0.5	1.25	atputs (6)	O Insmos	8 Jentin Re	
Output Sink Current-VCR outp	ut-	IOL		E 01							mA
(V _{OL} = 0.4 V)			5	15	_	0.3	1.00	_			
(V _{OL} = 0.5 V)			10		THE			-	ogrue RO	V per I lis	
(V _{OL} = 1.5 V)	901		15	8	-	0.5	1.25	-		(a b = a & d	
Input Current (L Device)	UP	lin	15	01_	±0.1	-	± 0.00001	± 0.1	-	± 1.0	μΑ
Input Current (P Device)	000	lin	15	- 91	±0.3	-	± 0.00001	±0.3	-	± 1.0	μΑ
Input Capacitance (Vin = 0)	CINC	Cin	-	ō.	HUM	-	5.0	7.5	3/4_38/10	s (Figure 2	pF
Quiescent Current (L Device)	088	IDD	5	24	0.3	+	0.08	0.25	-	0.2	mA
(Per Package)	7.1		10	2-	1.5	+	0.40	1.25	-	1.0	
0.8			15	GT	3.0	+	0.85	2.50	-	2.0	
Quiescent Current (P Device)	23	ממו	5	45	0.3	-	0.08	0.25	-	0.2	mA
(Per Package)			10	-	1.5	+	0.40	1.25	B ATems	1.0	15.0800
0.00	nes.		15	-	3.0	+	0.85	2.50	-	2.0	
Total Supply Current**†	0.8	IT	5	Of	1 115	1 _T = (1	1.9 µA/kHz)f	+IDD			μА
	4:0		10	-81		$I_{T} = (3$	3.8 µA/kHz)f	+IDD			
Per Package) (C _L = 50 pF on all outputs, all buffers switching)	800		15	8		1 _T = (5	5.7 μA/kHz)f	+ IDD			

tTo calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) \text{ V}_{DD} f$ where: I_T is in μ A (per package), C_L in pF, VDD in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.



SWITCHING CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

Int X5W Characteris	stic M gyT n	Symbol	VDD	V Min odn	Тур	Max	Unit
Output Rise Time, Segment Ou	itputs (Figure 1)	tTLH		30		ADV-menub	ns ns
			5	-	210	450	
		0 -	10	9 -	145	300	
			15	01 -	90	200	0= JOV
Output Fall Time, Segment Ou	tputs (Figure 1)	tTHL		61		(V	
			5	- 10	1.5	3.5	μS
			10	-	1.3	2.75	
	3 1.00 -	D	15	8 -	1.1	2.25	(Var = 0.4
Output Fall Time, VCR Output		tTHL	1	10		IV	ns
(Figures 3 and 4)		0 -	5	- 15	105	250	
		1.0+	10	ar t al	40	100	
			15	1 10	30	75	
Propagation Delay Time, A, B,	C, D to Segment	tPLH		01		1001920 11	ns
Outputs (Figure 2)	0.1 UC		5	1 00	935	2400	TOUR Lapac
			10	-	340	900	
		+ 8.0	15	8 + 00	230	500	ulascent C
		tPHL	5	01 1	7.0	18.0	μS
		1,08	10	1-81 1	3.5	9.0	
		8:0	15	8 + 00	2.0	5.0	
Propagation Delay Time, A, B,	C. D to VCR	tPLZ		61		190	μS
Output (Figures 3 and 4)	0.85 2.50	17.6	5	15	11.0	25.0	μ5
Output (rigules 5 and 4)			10	18 1	8.0	20.0	
			15	0 L	4.0	10.0	
			5	8			9319 59
		tPZL			800	1500	ns
			10 15		400	1000 500	
	20 V 100 - 1010 - 01 K 8	A CHIEF DOCUME	15	C martin lection	200	500	ministration to
Propagation Delay Time, LE to	Segment	tPLH	5	of opv. He m	O Japayosa	is in a cliner	ns
Outputs (Figure 5)				eracteristics co	1300	3000	
			10		500	1500	
			15	-	350	1000	
		tPHL	5	-	16.0	30.0	μS
			10	-	6.0	15.0	
			15	-	5.0	10.0	
Propagation Delay Time, LE to	VCR Output	tPLZ					μS
(Figures 4 and 6)			5	-	14.0	30	
			10	-	8.0	20	
		CIRCUIT	1091150	-	6.0	15	
		tPZL	5	-	10.0	25	μS
			10	-	5.0	15	
			15	-	4.0	10	
Setup Time, A, B, C, D to LE	Figure 7)	t _{su}	5	100	35	-	ns
		-	10	65	25	-	
			15	65	25	_	
Hold Time, LE to A, B, C, D (F	igure 7)	th	5	125	45	_	ns
			10	75	30		12 FI 118
			15	75	25	_	
Latch Enable Pulse Width, LE (Figure 7)	twL	5	525	210		ns
LOTO, Eliable i dise viidtii, EE (riguio //	12 00S	10	200	80		115
		1111	15	140	55		
			1 0 10	140	00		

2

INPUT/OUTPUT FUNCTIONS

SEGMENT DRIVER (a, b, c, d, e, f, g, h + i; PINS 12, 13, 14, 15, 1, 2, 3, 4)

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of $V_{\rm DD}=5.0$ volts.

OUTPUT (VCR; PIN 11)

This output is activated (goes low) whenever inputs A, B, C, and D are all set to a logic one. Otherwise the output is open. See the truth table.

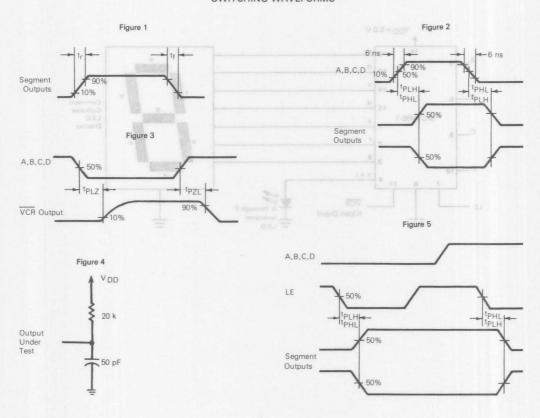
INPUT DATA (A, B, C, D; PINS 5, 6, 9, 10)

The block diagram is shown on page 1. The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by the Latch Enable input.

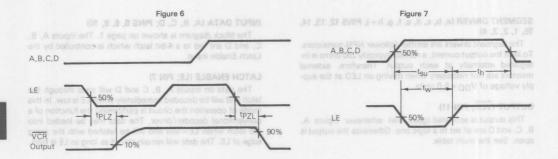
LATCH ENABLE (LE; PIN 7)

The data on inputs A, B, C and D will pass through the latch and will be decoded immediately when LE is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when LE=low and will be latched with the rising edge of LE. The data will remain stored as long as LE is high.

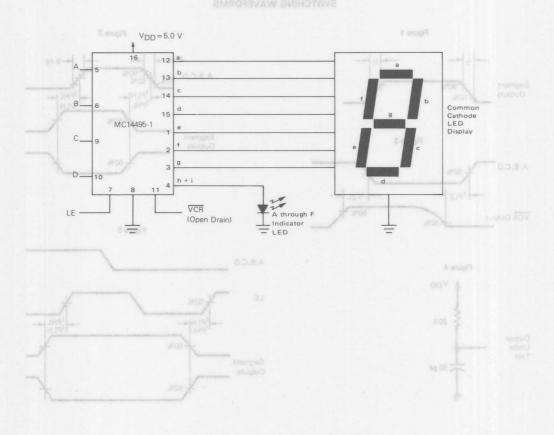
SWITCHING WAVEFORMS







TYPICAL CIRCUIT @ VDD = 5.0 V





PCM REMOTE CONTROL TRANSMITTER

The MC 14497 is a PCM remote control transmitter realised in CMOS technology. Using a dual-single (AM/FSK) frequency biphase modulation the transmitter is designed to work with various receivers.

- Both AM/FSK modulation selectable
- mure 62 channels up to 62 keys a to not assigned blove of made and and
 - 500kHz reference oscillator controlled by inexpensive ceramic resonator
 - Very low duty cycle
 - · Very low standby current
 - Infrared transmission
 - Selectable Start-Bit polarity (AM only)
 - Shifted key mode available

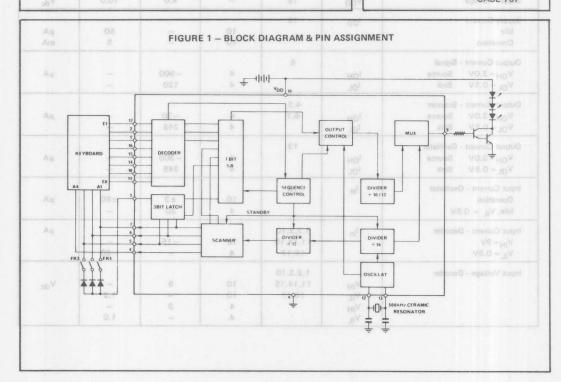
CMOS

PCM REMOTE CONTROL
TRANSMITTER



This device contains circuitry to pro

P SUFFIX
PLASTIC PACKAGE
CASE 707



MC14497



· Very low standby current

MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit	1 E3 V _{DD} 18 2 E2 E1 17
OC Supply Voltage	V _{DD}	-0.5 to +15	Vdc	3 = E9 E4 = 16
nput Voltage, All Inputs	V _{in}	-0.5 to V _{DD} +0.5	Vdc	4 A4 E5 15 5 A3 E6 14
OC Current Drain per Pin	1	10	mA	6 A2 Osc 13
Operating Temperature Range	TA	0 to +70	°C	7 A1 100 Osc 12 A MOS
torage Temperature Range	T _{stg}	- 65 to + 150	°C	8 V1 E8 11 9 V _{SS} E7 10 VAA OM SE

PIN	ASSIG	NME	ENT
1 =	E3	VDD	18
2 =	E2	E1	17
3 🗀	E9	E4	16
4	A4	E5	15
5 🗀	A3	E6	14
6 =	A2	Osc	13
7	A1 / 0	Osc	12 A MO9
8 =	V1	E8	— 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°)

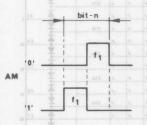
Characteristics	Symbol	Pin	V _{DD} V _{dc}	Min sidsli	evs si Max ysx t	of in Units
Supply Voltage	V _{DD}	18	-	4.0	10.0	V _{dc}
Supply Current Idle Operation	DD ^I	18 9 8 Mardau	10 01 0 T	≣RUĐI <u>3</u>	50 5	μA mA
Output Current - Signal VOH = 3.0V Source VOL = 0.5V Sink	I _{OH}	8	4 4	-900 120	_	μА
Output Current - Scanner VOH = 3.0V Source VOL = 0.5V Sink	I _{OH}	4,5, 6,7	4 4	-30 245	(i) (ii)	μА
Output Current - Oscillator VOH = 3.0V Source VOL = 0.5V Sink	I _{OH}	13	4 4	-300 245	Se GRAGEY	μА
Input Current - Oscillator Operation Idle, V _{IL} = 0.5V	over lin	13x12 kg	10	±2 30	±80 -	μА
Input Current - Decoder V _{IH} = 9V V _{IL} = 0.5V	s cond lin	1,2,3,10 11,14,15 16,17	10	-15 -	- -60	μА
Input Voltage - Decoder		1,2,3,10 11,14,15 16,17	10 10 4	9 - 3	1.2	V _{dc}

CIRCUIT OPERATION

The transmitter emits a 6-bit, labelled A(LSB) to F(MSB), binary code giving a total of 64 possible combinations or code words. All of these are user selectable, except the last two- where channel 63 is not sent while channel 62 is automatically sent by the transmitter at the end of each transmissions as an "End of Transmission" code.

In either mode, AM or FSK, the transmitted signal is in the form of a biphase pulse code modulation (PCM) signal. The AM coding is shown in figure 1.

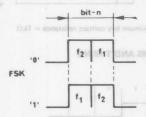
FIGURE 2 - AM CODING



Where f₁ is a train of pulses at the modulating frequency of 31.25 kHz for a reference frequency of 500 kHz.

In the FSK mode two modulating frequencies are used as shown in figure 3,

FIGURE 3 - FSK CODING



Where f_1 is 50 kHz and f_2 is 41.66 kHz for a reference frequency of 500 kHz.

The keyboard can be a simple switch matric using no external diodes, connected between the four scanner outputs, A1 to A4, and the eight row inputs, E1 to E8. Under these conditions only the first 32 code words are available, bit-F is always at logical "O". However, a simple two-pole, changeover switch, in the manner of a typewriter "shift" key (switch FK3 in figure 1) can be used to change the polarity of bit-F to give access to the next full set of 32 instructions.

An alternative method of accessing more than 32 instructions is by the use of external diodes between the address inputs, see figure 4. These have the effect of producing "phantom" address inputs by pulling two inputs low at

the same time, which causes bit-F to go high, that is to logical "I". By interconnecting only certain address inputs it is possible to make an intermediate keyboard with between 32 and 64 keys.

The other two switches in figure 1, FK1 and FK2, change the modulation mode, a closure changes the modulation from FSK to AM, and the start-bit polarity, a closure changes the start-bit to a logical "O", respectively:

The full range of options available is illustrated in the table below:

	Start-bit	Modulation	bit-F	Channels
E9 - open	o.H1sh	FSK	0	0 - 31
E9 - A1 (FK1)	151 celles	AM	0	0 - 31
E9 - A2 (FK2)	0	FSK	0	0 - 31*
E9 - A3 (FK3)	1	FSK	1	32 - 61
E9 - A1 + A2	0	AM	0	0 - 31
E9 - A1 + A3	Simila Bein	AM	1 2	32 - 61
E9 - A2 + A3	0	FSK	./II	32 - 61*
E9 - A1 + A2 + A3	0	AM	1	32 - 61

- Not allowed.

One of the transmitter's major features is its low power consumption – in the order of $10\mu A$ in the idle state. For this reason the battery is perpetually in circuit. It has in fact been found that a light discharge current is beneficial to battery life.

In its active state the transmitter efficiency is increased by the use of a low duty cycle, less than 2.5% for the modulating pulse trains.

While no key is pressed the circuit is in its idle state, the reference oscillator is stopped and the eight address input lines are held high through internal pull-up resistors.

As soon as a key is pressed this takes the appropriate address line low, signalling to the circuit that a key has been selected. The oscillator is now enabled. If the key is released before the code word has been sent the circuit returns to its idle state. To account for accidental activation of the transmitter the circuit has a built-in reaction time of some 20ms, which also overcomes contact bounce. After this delay the code word will be sent and repeated at 90ms intervals for as long as the key is pressed. As soon as the key is released the circuit automatically sends channel 62, the "End of Transmission" (EOT) code. The transmitter then returns to its idle state.

The differences between the two modulation modes are illustrated in figure 5. However it should be noted that:

In the AM mode each transmitted word is preceded by a burst of pulses lasting $5\,1\,2\,\mu s$. This is used to set up the AGC loop in the receiver's preamp. In the FSK mode the first frequency of the first bit is extended by 1.5ms and the AGC burst is suppressed. In either mode it is assumed that the normal start-bit is present.

2

Row Inputs E1 to E8 (Pins 1, 2, 10, 11, 14, 16 & 17). Under idle conditions these inputs are held high, by internal pull-up resistors. As soon as a key is pressed a logical "O" on that particular line signals to the circuit that a key has been selected. After a delay of 20ms the internal register is loaded with the code word for the key selected.

Row Input E9 (Pin 3). This is a special programming input and when connected to the appropriate scanner output, via a diode, it will modify the transmitted output according to the table in the previous section.

In that table the figures in brackets, FK1 etc. refer to the switches shown in figures 1 and 4. If only one option is required the diode may be omitted. The connections shown in the table may be made in any combination.

Although E9 is a row input forcing this line low will not activate the circuit.

Scanner Outputs A1 to A4 (Pins 4, 5, 6 & 7). Under idle condition these outputs are held low, logical "O". When the circuit is activated, by a key being pressed, the oscillator will start and release the outputs.

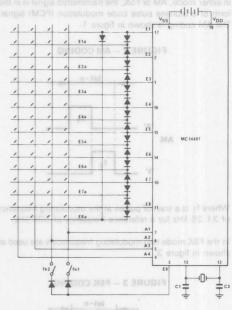
Oscillator (Pins 12 & 13). This is designed to operate with a 500kHz ceramic resonator or a tuned LC circuit.

It is important that a ceramic resonator and *not* a filter is used here as the oscillator frequency can not be guaranteed if a ceramic filter is used.

Signal Out (Pin 8). This output provides the modulating signal ready to drive the modulation amplifier.

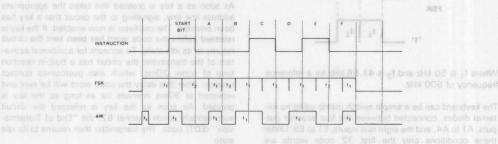
If required the transmitter can be used as a keyboard encoder for direct use with a receiver. In this case the AM option is selected, the output inverted and fed directly to the receiver's signal input pin.

FIGURE 4 - 64-KEY KEYBOARD



Note : Maximum key contact resistance = $1k\Omega$

FIGURE 5 - TRANSMITTED WAVEFORMS AND TIMING





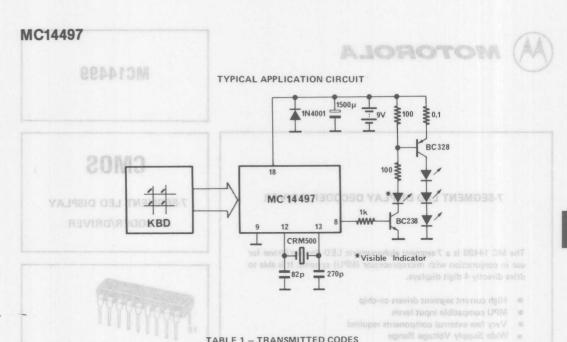


TABLE 1 - TRANSMITTED CODES

Channel		C	ode	wo	rd		Key	yboard	Channel			C	ode	wo	rd		Keybo	ard
	F	E	D	C	В	A	-In-	Out			F	E	D	C	В	Α	In	Ou
0	0	0	0	0	0	0	E8	A4	32		1	0	0	0	0	0	E8a	A
1				0	0	11:000	E1.	A4	33					0	0	1	E1a	A
2				0	1	0	E2	A4	34					0	1	0	E2a	A
3				0	1	1	E3	A4	35					0	1	1	E3a	A
4				1	0	0	E4	A4	36					1	0	0	E4a	A
5				1	0	1	E5	A4	37					1	0	1	E5a	A
6				1	1	0	E6	A4	38					1	1	0	E6a	A
7				1	1	1	E7	A4	39					1	1	1	E7a	A
8	0	0	1	0	0	0	E8	A1	40		1	0	1	0	0	0	E8a	A
9				0	0	1	E1	A1	41					0	0	1	E1a	A
10				0	1	0	E2	A1	42					0	. 1	0	E2a	A
11				0	1	1	E3	A1	43					0	-1	1	E3a	A
12				1	0	0	E4	A1	44					1	0	0	E4a	A
13				1	0	1	E5	A1	45					1	0	1	E5a	A
14				1	1	0	E6	A1	46					1	1	0	E6a	A
15				1	1	1	E7	A1	47					1	1	1	E7a	A
16	0	1	0	0	0	0	E8	A3	48		1	1	0	0	0	0	E8a	A
17				0	0	1 /	E1	A3	49					0	0	1	E1a	A
18				0	1	0	E2	A3	50					0	1	0	E2a	A
19				0	1	1	E3	A3	51					0	1	1	E3a	A
20				1	0	0	E4	A3	52					1	0	0	E4a	A
21				1	0	1	E5	A3	53					1	0	1	E5a	A
22				1	1	0	E6	A3	54					1	1	0	E6a	A
23				1	1	1	E7	A3	55					1	1	1	E7a	A
24	0	1	1	0	0	0	E8	A2	56		1	1	1	0	0	0	E8a	A
25				0	0	1	E1	A2	57					0	0	1	E1a	A
26				0	1	0	E2	A2	58					0	1	0	E2a	A
27				0	1	1	E3	A2	59					0	1	1	E3a	A
28				1	0	0	E4	A2	60					1	0	0	E4a	A
29				1	0	1	E5	A2	61					1:	0	1	E5a	A
30				1	1	0	E6	A2	62 (EC	(TC		-		1	1	0	E6a	A
31	0	1	1	1	1	1	E7	A2	Not transmit	ted	1	1	1	1	1	1	E7a	A
									NOTE: Althousing a keybo	ough the	a 'a' :	uff	ix a	ppli	es	to a 'pl	nantom' inpu	it w

MC14499

ACTAVS!

2

7-SEGMENT LED DISPLAY DECODER/DRIVER

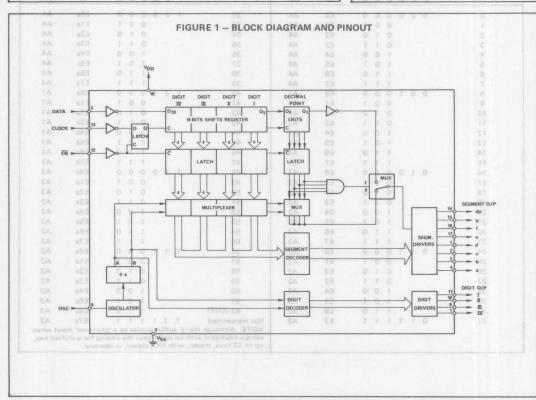
The MC 14499 is a 7-segment alphanumeric LED decoder/driver for use in conjunction with microprocessor (MPU) systems. It is able to drive directly 4 digit displays.

- High current segment drivers on-chip
- MPU compatible input levels
- Very few external components required
- Wide Supply Voltage Range

CMOS

7-SEGMENT LED DISPLAY
DECODER/DRIVER





MAXIMUM RATINGS (Voltages referenced to VSS) TARBED THORIO

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to+7.0	Vdc
Input Voltage, all Inputs	VIN	-0.5 to V _{DD} + 0.5	Vdc
Operating Temperature Range	TA	0 to + 70	°C
Storage Temperature Range	TSTG	-65 to+150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid an application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

In order to enter data the enable input, EN, m

PIN ASSIGNMENT

17

16

15

13

口 12

11

10

register to the latches when EN goes high, = 1. While the

An external oscillator signal can be used, within the ELECTRICAL CHARACTERISTICS (VDD = 4.5 to 6.5 V)

Characteristic	Pin	Symb.	ednessek er	90		250		70	ne latch of	Uni
provides four non-over lapping aponding to the four digits		four c	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	11
Input Voltage '0' level '1' level Input Current $(V_{IN} = 0 \text{ to } V_{DD})$	5,12, 13	VIL VIH IIN	0.7xV _{DD}	0.3xV _{DD}	0.7xV _{DD}	0.45xV _{DD} 0.55xV _{DD} ±0.001	0.3xV _{DD} - ±0.1	0.7xV _{DD}	0.3xV _{DD} ±1.0	Vdc Vdc μA
Oscillator Input Voltage '0' level '1' level Oscillator Input Current V _{OSC} =0' V _{OSC} =V _{DD}	6 eidt n	VILO VIHO IOL IOH	0.75xV _{DD}	0.25xV _{DD} 100 -100	0.75xV _{DD} 30 -30	0.3×V _{DD} 0.7×V _{DD} 50 -50	0.25×V _{DD} - 80 -80	0.8xV _{DD} 10 -10	1111 w	Vdc Vdc μA μA
Segment Driver Voltage below V _{DD} I _{OUT} =50mA I _{OUT} =10mA Segment Driver OFF Leakage V _{OUT} =0	14,15, 16,17	V _{DD} - -VsOH	WT 916 9101	1.1	firstly los - - g 1, with 3	0.9 0.7	0.75	ers a set-b cading wor displayers 20-bits, th	1.1	Vdc Vdc
Digit Drivers	10,11	Грон	6 -0.2		5.5 -0.2	8 -2 891	he latch 3 (n-f) tin	baol of .	checky 3 EN = 1 4 Repeat	mA mA
Quiescent Current V _{IN} = 0, I _{OUT} = 0, C _{OSC} = 15 nF	18	olicatio	protected typical ap		ts, with 111 ascad <u>i</u> ng.	to a circui				mA
Maximum Power Dissipation				500	_	_	500		500	mW

SWITCHING CHARACTERISTICS (VDD = 5V ± 10 %, TA = 0 to 70 %)

Characteristic Fig. Symbol Min. Max. Unit Clock High time 1 _ d VDD 18 3 2 tCH μs Clock Low time 3 tCL 02 μs 2 = C old site Clock Rise time 3 2 tCR μs 3 □ b Clock Fall time 3 2 tCF μs 4 [а Enable Lead time 3 †Elead 200 ns 5 🗆 Enable Lag time Data DP 3 200 tElag ns Data Set-up time 3 tDSup 200 6 == Osc CL ns Data Hold time 3 tDHold 1 шs IV EN 7 Scanner Frequency* 5 1/tScan 50 300 Hz 111 1 8 [Osc/Digit Lead time 5 top 10 ШS 11 Osc/Segment Lead time 9 VSS 5 tos 10 μs Digit Overlap 5 tov 5 μs

^{*} Scanner Capacitance = 22nF.

The circuit accepts a 20-bit input, 16-bits for the four digit display plus 4-bits for the decimal point — these latter four-bits are optional.

The input sequence is the decimal point code followed by the four digits, as shown in figure 2.

In order to enter data the enable input, $\overline{\text{EN}}$, must be low, = 0. The sample and shift are accomplished on the falling clock edge, see figure 3. Data are loaded from the shift register to the latches when $\overline{\text{EN}}$ goes high, = 1. While the shift register is being loaded the previous data are stored in the latches.

If the decimal point is used the system requires 20 clock pulses to load data, otherwise only 16 are required.

CASCADING

The circuit may be cascaded in the following manner.

If a 1111 word is loaded into the decimal point latch, the output of the shift register is switched to the decimal point driver, see figure 4. Therefore, to cascade n four digit display drivers a set-up is used which will firstly load the 1111 cascading word:

- $1 \overline{EN} = 0$
 - 2 Load 20-bits, the first four bits being 1, with 20 clock pulses.
 - $3 \overline{EN} = 1$, to load the latch
 - 4 Repeat steps 1 to 3 (n-1) times
 - 5 (nX20)-bits can be loaded into n circuits, with 1111 as decimal point word to continue the cascading.

SCANNER

The scanner frequency is determined by an on-chip oscillator, which requires an external frequency determining capacitor. The capacitor voltage varies between two trigger levels at the oscillator frequency.

An external oscillator signal can be used, within the recommended operating range of 200 to 800Hz — to avoid flicker and digit overlap. For test purposes this frequency can be increased up to 10kHz.

A divide by four counter provides four non-over lapping scanner waveforms corresponding to the four digits — see figure 5.

SEGMENT DECODER

The code used in this matrix decoders is shown in figure 6.

OUTPUT DRIVERS

There are two different drivers : " = 100 V

The segment and decimal point drivers; these are NPN emitter followers with no current limiting devices.

The digit output buffers; These are short circuit protected CMOS devices.

A typical application circuit is shown in figure 7.

SWITCHING CHARACTERISTICS (VDD = FIGURE 2 - INPUT SEQUENCE ← time Bit No. 18 16 15 13 11 10 8 5 shift → Ξ Digit Digit LSB Digit IV Digit III Digit II **Decimal Point** Digit I

FIGURE 3a - SERIAL INPUT, POSITIVE CLOCK

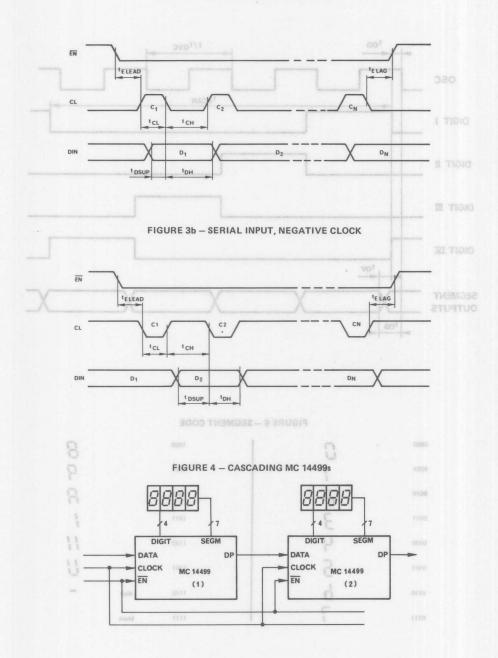


FIGURE 5 - SCANNER WAVEFORMS

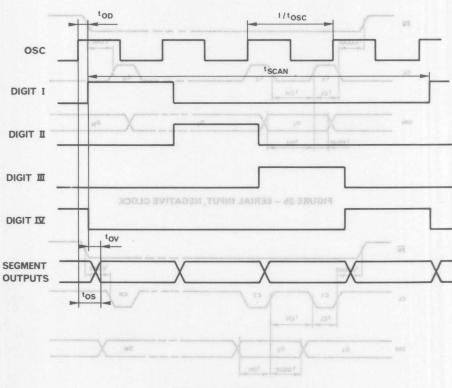
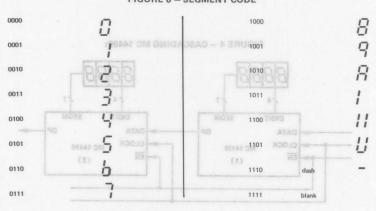
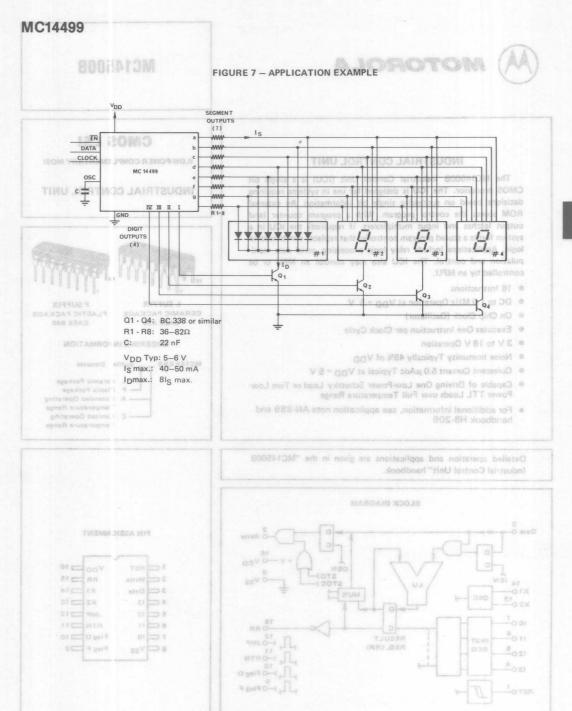


FIGURE 6 - SEGMENT CODE







MC14500B

INDUSTRIAL CONTROL UNIT

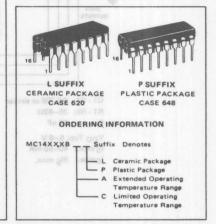
The MC14500B Industrial Control Unit (ICU) is a single bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

- 16 Instructions
- DC to 1.0 MHz Operation at VDD = 5 V
- On Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 V to 18 V Operation
- Noise Immunity Typically 45% of VDD
- Quiescent Current 5.0 μAdc Typical at VDD = 5 V
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range
- For additional information, see application note AN-889 and handbook HB-209

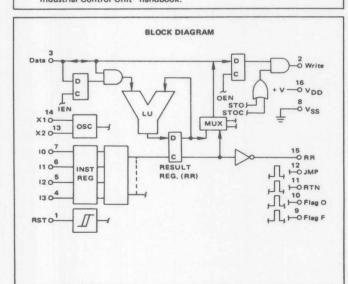
CMOS LSI

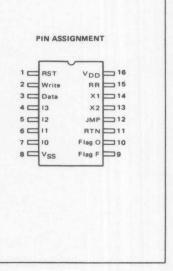
(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL CONTROL UNIT



Detailed operation and applications are given in the "MC14500B Industrial Control Unit" handbook.





MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10 - 10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	оС
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out}) < V_{DD}.

ELECTRICAL CHARACTERISTICS

			318.0		0.0	VDD	Tio	w*		25°C		Th	igh "	
Characterist	ic as				Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	. 08		"0" Leve	el	VOL	5.0		0.05	-	0	0.05	-	0.05	Vdc
Vin = VDD or 0				-	oi	10	-	0.05	-	0	0.05	-	0.05	
орАн			(sA/kHz)		100	15	-	0.05	-	0	0.05	Xne Tru C	0.05	Sugar .
			"1" Leve		VOH	5.0	4.95	-	4.95	5.0	eo (4.95	Capacia	Vdc
Vin = 0 or VDD			(sH#\Au		.01	10	9.95	_	9.95	10	-	9.95	street@(HA
VIII VOLVOO					-	15	14.95	_	14.95	15	-	14.95	_	-
Input Voltage #			"O Level	"	VIL			2011/10/05	TOTAL III		2014219	200	1	Vdc
RST, D. X2			0 2010		115		000	niveO 90	ter CLA	0°88+ 4		A not De		dist ¹
(Vo = 4.5 or 0.5 Vdc)						5.0	A 97 38 of	1.5	19708190	2.25	1.5	loeds yr	1.5	Noil s
(Vo = 9.0 or 1.0 Vdc)						10	-110	3.0	2 Judin s	4.50	3.0	enante XII	3.0	1000
(Vo = 13.5 or 1.5 Vde		OL Y			bond 1 best	15	00-0	4.0	de i-a-t	6.75	4.0	REARING	4.0	Trave
			"1" Leve		VIH				(.81)	ey bote a	a for Da	101 177	+ 90 00	Vdc
(Vo = 0.5 or 4.5 Vdc)					1111	5.0	3.5		3.5	2.75	_	3.5	-	1
(Vo = 1.0 or 9.0 Vdc)	and a				- 4	10	7.0		7.0	5.50	_	7.0	_	
(VO = 1.5 or 13.5 Vde		TY				15	11.0	11.65	11.0	8.25	Shall and	11.0		-
Input Voltage #		2015	"0" Leve	al	VIL	0.8	1910	-			HOLLX	Detti I Va	BLLADIS	Vdc
10, 11, 12, 13			O LEVE		1 TIL	ar .	_JF	d)						1
(V _O = 4.5 or 0.5 Vdc)						5.0		0.8	_	1.1	0.8	O-10013	0.8	1X
(V _O = 9.0 or 1.0 Vdc)						10	_	1.6	_	2.2	1.6	C Bally	1.6	100
(VO = 13.5 or 1.5 Vdc						15		2.4		3.4	2.4	_	2.4	
100 1000 110 40			"1" Leve	-1	V	18	-	2.7	-	0.4	6.17		articley as	Vdc
(Vo = 0.5 or 4.5 Vdc)			1 Leve	ei	VIH	5.0	2.0	_	2.0	1.9	_	2.0		Vac
(V _O = 1.0 or 9.0 Vdc)						10	6.0	_	6.0	3.1	_	6.0	_	
(V _O = 1.5 or 13.5 Vdc)		250				15	10	_	10	4.3	_	10	staG o	IX.
	1	307			-	15	10		10	4.3		10		
Output Drive Current	0		Source		ІОН	15								mAdo
Data, Write (AL/CL/CP D	1 0					1.8	1.0					0.7		RBR
(V _{OH} = 4.6 Vdc)						5.0	1.2	-	-1.0 -3.0	-2.0	-	-0.7	-	1
(VOH = 9.5 Vdc)						10	7.2	-		-6.0	-	-2.1	_	
(V _{OH} = 13.5 Vdc)						15	-		-6.0	-12		-4.2	135-01	189
(VOL = 0.4 Vdc)			Sink		IOL	5.0	1.9	-	1.6	3.2	-	1.1	-	mAdo
(VOL = 0.5 Vdc)					-	10	3.6	-	3.0	6.0	, KITCH .	2.1	to Flag	128
(VOL = 1.5 Vdc)	- 0	XIP.		77		15	7.2	-	6.0	12	ALC: N	4.2	Bei.7 en	
Output Drive Current			Source		ІОН	3.5								mAdd
Other Outputs (AL Devic	9)					58			1			aruG I		28
(VOH = 2.5 Vdc)		229				5.0	-3.0	-	-2.4	-4.2	_	-1.7		
(VOH = 4.6 Vdc)		178				5.0	-0.64	-	-0.51	-0.88	_	-0.36	_	
(VOH = 9.5 Vdc)						10	-1.6	NO -	-1.3	-2.25	-	-0.9	b Weelu	Clock
(VOH = 13.5 Vdc)						0115	-4.2	-	-3.4	8.8	-	-2.4	-	
(VOI = 0.4 Vdc)			Sink		IOL	5.0	0.64	_	0.51	0.88	_	0.36	_	mAdo
(VOL = 0.5 Vdc)					1	10	1.6	147	1.3	2.25	_	0.9	billy_getu	2000 Fl
(VOL = 1.5 Vdc)	1 5					15	4.2	-	3.4	8.8	-	2.4	_	
Output Drive Current		-	Source	100	ТОН	-								mAdo
Other Outputs (CL/CP De		200		008	.01	0.8	(1)	ps.				joiyau un		I III
(VOH = 2.5 Vdc)		126				5.0	-2.5		-2.1	-4.2	-	-1.7	-	
(VOH = 4.6 Vdc)		100			-	5.0	-0.52	-	-0.44	-0.88	_	-0.36	_	te G
(VOH = 9.5 Vdc)		50			189	10	-1.3	107	-1.1	-2.25	_	-0.9	_	100
(VOH = 13.5 Vdc)		40				15	-3.6	_	-3.0	-8.8	_	-2.4	_	1
(VOL = 0.4 Vdc)			Sink		IOL	5.0	0.52		0.44	0.88	_	0.36	miem	mAdo
(VOL = 0.5 Vdc)		0	JIIIK		OL	10	1.3	217 -	1.1	2.25	_	0.36		made
(VOL = 1.5 Vdc) 4						15	3.6		3.0	8.8		2.4	_	
OFo 400/ 4		OCH				.0	0.0		3.0	0.0	_	4.9		1

ELECTRICAL CHARACTERISTICS (continued)

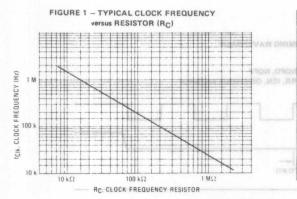
Characteristic Symbol Vdc Min	Max ± 0.1 ± 0.3 - 5.0 10 20 20	Min	Typ 150 ±0,00001 ±0,00001 15 5.0 0.005 0.010 0.015	Max - ±0.1 ±0.3 - 7.5 5.0 10	Min surgn sir Sun surgna surgna surgna surgna surgna surgna surgna surgna surgna surgna surgna	Max 250 ±1.0 ±1.0 - 150 300	Unit μAdc μAdc μAdc pF pF μAdc
Input Current (AL Device)	±0.1 ±0.3 - - 5.0 10 20	A7-	±0.00001 ±0.00001 15 5.0 0.005 0.010	±0.1 ±0.3 - 7.5 5.0	ngs 16 lure_Hang	±1.0 ±1.0 - - 150	μAdc μAdc pF pF
Input Current (CL/CP Device)	±0.3 - 5.0 10 20	A7=	±0.00001 15 5.0 0.005 0.010	± 0.3 - 7.5 5.0 10	naP_stu	±1.0	μAdc pF pF
Input Capacitance (Data)	5.0 10 20	-	15 5.0 0.005 0.010	7.5 5.0 10	-	150	pF pF
Input Capacitance (All Other Inputs)	5.0 10 20	912 -	5.0 0.005 0.010	7.5 5.0 10	o range ARACT	150	pF
(V in = 0) Quiescent Current (AL Device) (Per Package) Quiescent Current (CL/CP Device) Quiescent Current (CL/CP Device) IDD 5.0 Quiescent Current (CL/CP Device) IDD 5.0 —	5.0 10 20	912 _	0.005 0.010	5.0	ARACT	150	
(Per Package) 10 - 15 - 15 - 10 - 15 - 10 - 15 - 10 - 15 - 10 - 10	10 20	1-	0.010	10	ARACT	META STANDAR	μAdc
15 -	20	TE	1		Unite	300	1110000
Quiescent Current (CL/CP Device) IDD 5.0 -		-	0.015				
DD -	20		0.015	20	-	600	
(Per Package) - 80.0 0 - 10	20	m/2 _	0.005	20	D <u>11</u> 3110	150	μAdo
	40) -	0.010	40	-	300	aV rugsi
80.0 - 80.0 0 - 8015	80	-	0.015	80	-	0 600	I = miV
**Total Supply Current at an External IT -		1 _T = (1.5 μA/kHz)	f + IDD			μAdc
Load Capacitance (CL) on 0.8 39.8 - 0.8	LB HI	VIT = (3.0 MA/kHz)	f + IDD			100
All Outputs 38.8 - 01 38.8 - 8.8 9		IT = ((4.5 µA/kHz) f + IDD			agV 103	Vin = p
* T _{IOW} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.	11	V	"leveul 0"			0.000	sioV suc

(VQ = 4.5 or 0.5 Vdc) (VQ = 8.0 or 1.0 Vdc) SWITCHING CHARACTERISTICS ($T_A = 25^{\circ}C$; $t_r = t_f = 20$ ns for X and I inputs; $C_L = 50$ pF for JMP, X1, RR, Flag O; Flag F; $C_L = 130$ pF + ITTL load for Data and Write.)

C _L = 130 pF + ITTL load for Data and Write.)						Visit L			All Types (abV 8.4 to 1.0 = 0V)					
2.75 - 3.5 -		3.5	3.5		VDD			All Types	ro = 0A)					
	Chara	acteristic	5.50	7,0	Sy	mbol	Vdc		Min	Тур	Max	Unit		
Propagation De	lay Time	X1 to F	RR	Mr. V. V	tp	PLH,	5.0		_	250	500	ns		
						PHL	10	11	_ lava_i	125	250	gasloV sur		
							15		_	100	200	11, 12, 13		
X1 to Flag F	, Flag O	RTN, J	IMP .		8.0		5.0		-	200		ns		
		8.7		-	8.1		0110		-	100	200 0.1 10 1	(VO = 9.4		
2.4		2.4		-	2.4		8115		-	85	(5)170 .7 10 8.	Cr = aV1		
X1 to Write							5.0	11/2	- leve_l	225	450	ns		
			0.7	2.0	-		10		-	125	250 A 10	$(V_{O} = 0.1)$		
				0.8			15		-	100	200	Model		
X1 to Data				01			5.0		-	250	500	ns		
		-			-	-	10	-	-	120	240			
ob Am							15	101	901	100	200	tout Drive		
RST to RR							5.0		-	250	500	ns		
					-	1.2	10		-	125		= HOA		
				0,8-	-	3.6	15		-	100	200 SbV 8.			
RST to X1				0.8-			5.0		-	450	Note 1			
					-		0.810	101	- 0	200	(sigV A.	EVOL " C		
					-		15		-	150		Da inVi-		
RST to Flag	F, Flag	O, RTN	, JMP		1		5.0		-	400	800 (abV 8.	= nsV)		
sbAm I			-		-	-	10	TX	901	200	400	tout Drive		
207-1111							15	10"	_ 1001	150	300	constant and		
RST to Write	e, Data						5.0		-	450	900	ns		
			-4.2		1 17		0.010		-	225	450 96 V 8			
100	-0.36	-	88.0-	-0.61	-	08.0-	0.615		-	175	350	(AOM = N		
Clock Pulse Wid	ith, X1	-	-2,28	-13	- t)	N(cl)	5.0		400	200	_ (strV c.	ns		
				A.S.	-		ar 10		200	100	3.5 Vde)_	= HOV		
Sh.Am	0.00		00.0	120		100.0	15		180	90	- Labor N	Diament Contract of the Contra		
Reset Pulse Wid	th, RST			1.3	t	W(R)	5.0		500	250	- (sty 8)	ns vi		
	2.4		8.8	3.6		0.8	10		250	125	S Vdc)			
	1		0,0		1	31.5	15		200	100		aro		
Setup Time - I	nstructio	n			t,	su(1).	5.0	1000	400	200	s (Ct_/CP Davice)	ns		
							10		250	125				
	-1.7		-4.2		-	-2.8	15		180	90	_ lobV 8.	(AOM = 3		
Data	-0.38				te	u(D)	5.0		200	100	- 130 A. O.	ns		
		1 -	-2.25		- 1		10		100	50		B = MOA)		
-	14.5-		8.8-	-3.0	1000	3.6	8115		80	40	3.5 Vdo)_	(= NOA)		
Hold Time - In	struction	n -	68.0	0.46	_ tı	h(I) 8.0	5.0	100	100	0	- (ab V de)	ns		
	0.0			1.1	-	1.8	10		50	0	- (abV 8	(VOL = 0		
			8.8		1	3.8	15		50	0	5 Vde)			
Data					. t	h(D)	5.0	T	200	100	_	ns		
							10	-	100	50	_			
							15		100	50	-			

NOTE 1, Maximum Reset Delay may extend to one-half clock period.

[#] Noise immunity specified for worst-case input combination.

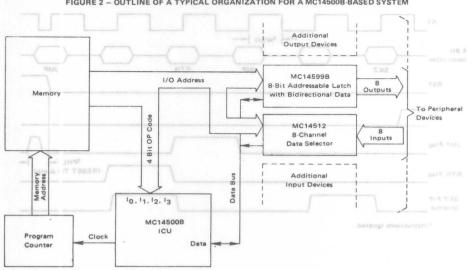


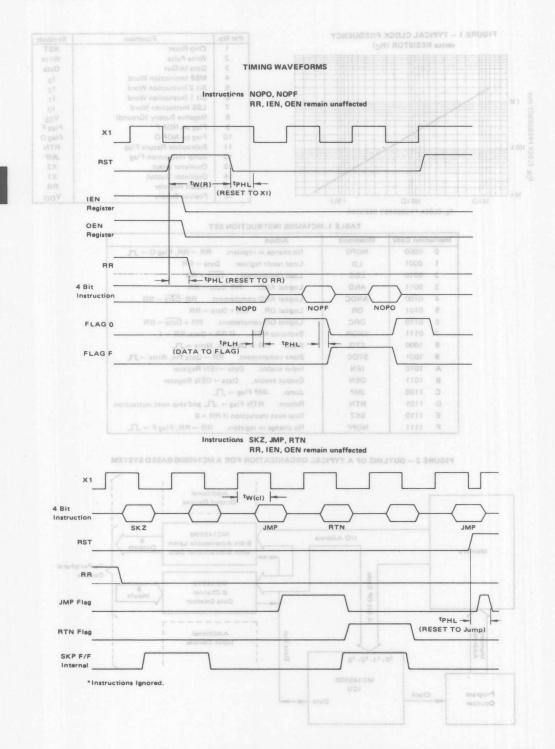
Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	13
5	Bit 2 Instruction Word	12
6	Bit 1 Instruction Word	11
7	LSB Instruction Word	10
8	Negative Supply (Ground)	Vss
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V _{DD}

TARLE 1 MC14500B INSTRUCTION SET

Instruc	tion Code	Mnemonic	Action
0	0000	NOPO	No change in registers. RR → RR, Flag O →
1	0001	LD	Load result register. Data → RR
2	0010	LDC	Load complement. Data → RR
3	0011	AND	Logical AND. RR Data -+ RR
4	0100	ANDC	Logical AND complement. RR · Data → RR
5	0101	OR	Logical OR. RR + Data → RR
6	0110	ORC	Logical OR complement. RR + Data → RR
7	0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8	1000	STO	Store. RR → Data Pin, Write → JL
9	1001	STOC	Store complement. RR → Data Pin, Write → JL
Α	1010	IEN	Input enable, Data → IEN Register
В	1011	OEN	Output enable. Data → OEN Register
C	1100	JMP	Jump. JMP Flag → JL
D	1101	RTN	Return. RTN Flag → JTL and skip next instruction
E	1110	SKZ	Skip next instruction if RR = 0
F	1111	NOPF	No change in registers. RR → RR, Flag F → \$\infty\$

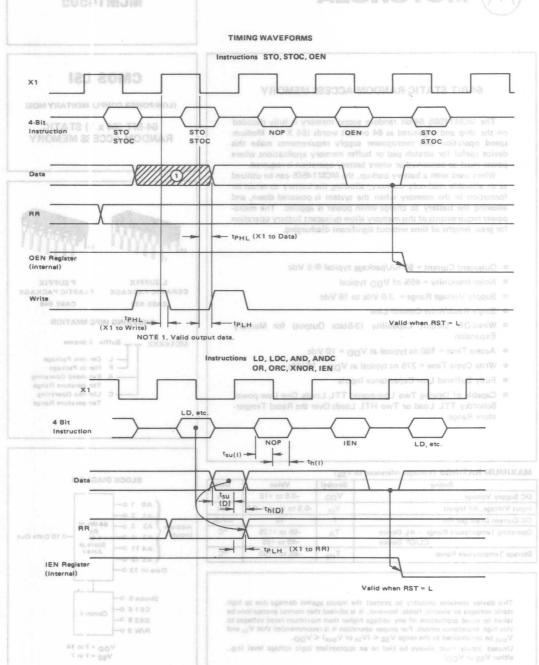
FIGURE 2 - OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM







MC14500B 202arm3M



MCM14505

NC14500B

THANKS WAVESCAME

64-BIT STATIC RANDOM ACCESS MEMORY

The MCM14505 64-bit random access memory is fully decoded on the chip and organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

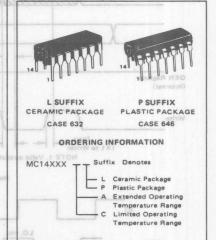
When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Current = 50 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at VDD = 10 Vdc
- Write Cycle Time = 275 ns typical at VDD = 10 Vdc and according to the control of the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 10 Vdc and according to the cycle Time = 275 ns typical at VDD = 275 ns typical at V
- Fully Buffered Low Capacitance Inputs
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

64-BIT (64 x 1) STATIC RANDOM ACCESS MEMORY



MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	оС

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM A0 1 0 A1 2 0-64-Word Address A2 3 0-By 1 Bit A3 4 0--0 10 Data Out Storage A4 11 0-A5 12 0-Data in 13 0-Strobe 5 0-CE16 0-Control CE28 0-R/W 9 0-VDD = Pin 14 VSS = Pin 7

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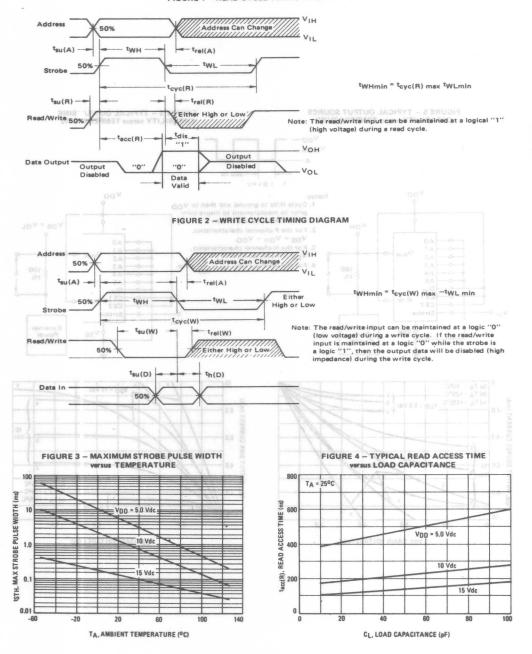
ELECTRICAL CHARA	CTERISTI	CS MINI	- ×		Symbol						
881	180		VDD	T	ow*		25°C	un 2.02	Th	igh*	1 1955
Characteristi		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05	-	0	0.05	PP-LCL I	0.05	Vdc
Vin VDD or 0		-	10	-	0.05	-	0	0.05	-	0.05	nogru
3.20	087	-	15	8 -	0.05	-	0	0.05	OFFICE -	0.05	DETT
1:50	"1" Level	VOH	5.0	4.95	-	4.95	5.0	32 mt	4.95	in 89.0) ~	Vdc
Vin O or VDD	65	-	10	9.95	-	9.95	10	33 Hs	9.95	en (1849) =	BHTI
981			15	14.95	(83) 55g/	14.95	15	-	14.95	yaleti no	reendo
Noise Immunity #		VNL			1				51	Access Tin	Vdd
(· V _{out} ≤ 0.8 Vdc)	465	-	5.0	1.0	-	1.5	2.25	1,14386	1.4	1) = +Rlas	12
(∴V _{out} ≤ 1.0 Vdc)	210		10	3.0	-	3.0	4.50	CL + 128	2.9	(1) = +Rlos	57
(∧V _{out} ≤ 1.5 Vdc)	130	-	15	4.5	-	4.5	6.75	30 L+ 10	4.4	07 7 +312	107
(\(V_{out} \) < 0.8 Vdc)		VNH	5.0	1.4	71/1/62	1.5	2.25	-	1.5	emiT-nwc	Vdd
(V _{out} ≤ 1.0 Vdc)	100	800	10	2.9	-	3.0	4.50		3.0	-	
(△V _{out} ≤ 1.5 Vdc)	50	125	15	4.4		4.5	6.75	_	4.5	_	
Output Drive Current (AL		10Н				-					mAd
$(V_{OH} = 2.5 \text{ Vdc})$	Source		5.0	-1.2	-02	-1.0	-1.7	- ,,	-0.7	emi i zgursi	1007500
(V _{OH} = 4.6 Vdc)		300	5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	
(V _{OH} = 9.5 Vdc)		120	10	-0.62	-	-0.5	-0.9	-	-0.35	-	
(V _{OH} = 13.5 Vdc)		-	15	-1.8	-	-1.5	-3.5		-1.1		-
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.3	(Q)m2	0.25	0.35	-	0.18	omit o	mAd
$(V_{OL} = 0.5 \text{ Vdc})$	70	200	10	0.9	-	0.75	1.2	-	0.50	-	
(V _{OL} = 1.5 Vdc)	25	75	15	2.2	-	1.7	4.5	1	1.2	-	
Output Drive Current (CL/		ІОН			-						mAd
$(V_{OH} = 2.5 \text{ Vdc})$	Source		5.0	-1.0	(FI) us?	-0.8	-1.7	-	-0.6	Brist III	as he
(V _{OH} = 4.6 Vdc)		270	5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
(V _{OH} = 9.5 Vdc)	20	60	10	-0.5	-	-0.4	-0.9	-	-0.3	-	
(V _{OH} = 13.5 Vdc)		-	15	-1.4	-	-1.2	3.5		-1.0	-	-
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.2	(W) thi	0.15	0.35	-	0.1	5/1#1 QU	mAd
(V _{OL} = 0.5 Vdc)		400	10	0.6	_	0.5	1.2	_	0.4	_	
(V _{OL} = 1.5 Vdc)						0.75	4.5 ±0.00001		0.6		
Input Current (AL Device)		lin	15	-	± 0.1	-		± 0.1	-	± 1.0	μAde
Input Current (CL/CP Dev	ice)	lin	15		± 1.0	-	±0.00001	±1.0		± 14	μAde
Input Capacitance (V _{in} = 0)	10	Cin	-		-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Dev	vice)	IDD	5.0		5.0	-	0.050	5.0	-	150	μAdo
(Per Package)		08	10	-	10	-	0.100	10	-	300	ON STE
	10	90	15	-	20	-	0.150	20	-	600	
Quiescent Current (CL/CP	Device)	IDD	5.0	-	50	-	0.050	50	-	375	μAd
(Per Package)		-	10	-	100		0.100	100	_	750	of but
011	- 00		15	-	200		0.150	200		1500	100
Total Supply Current**†		IT ₀	5.0			IT = (1	.28 μA/kHz	f + IDD			μAd
(Dynamic plus Quiescei	nt, ot-	0	. 10	3			.56 μA/kHz				
Per Package)			15	-	(W)ties?	1T = (3	.85 μA/kHz) f + 1DD			AR eri
(CL = 50 pF on all outp	outs, all	0		de i							
buffers switching)	- 01	. 0	1.5			-	T		_		-
Three-State Leakage Curre	30	ITLO	15		± 0.1	-	+0.00001	± 0.1	-	±3.0	μAd
(AL Device)					The same of						-
Three-State Leakage Curre (CL/CP Device)	008	ITL.	15	10 -	±1.0	-	+0.00001	± 1.0	-	± 7.5	μAd
0.6	150	-		ar I	-						
- 80 - 0	-	-		-					PIN AS	SIGNME	NT
*T _{low} = -55°C for AL D				un I							
Thigh = +125°C for AL #Noise immunity specifie				10				1 🗆	= A0	VD	
†To calculate total supply	current at le	oads other th	an 50 nF					2 □	A1	D	
IT(CL) = IT(50 pF)	+ 1 x 10-3	CL -50) VD	Df	-		1		3 🗆	A2 U	Assis Dela	
where: IT is in #A (per	package), Ci	in pF. Von	in Vdc.	and f in kl	Hz is input	frequenc	y. (bas	4 0		Author Car	100
**The formulas given are f	or the typica	l characterist	ics only a	at 25°C.			5.000				
001				88 1				5 □	ST	Dou	ut 🗀
								6 -			N

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

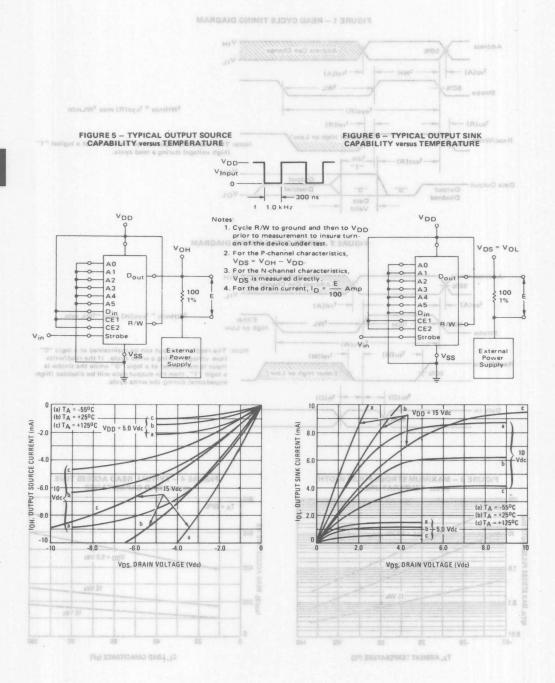
	Charac	cteristic			Symbol	VDD		Min	Тур	Max	Unit
Output Rise Time	7	1	28°C		tTLH .		J	1			ns
tTLH = (2.43 ns				-	wo!	0.0	OV	2000000	180	360	
tTLH = (1.08 ns				mild	NEW 1	10	SOV	Symbol	90	180	
tTLH = (0.72 ns	/pF) CL	+ 39 ns			80.0	15	9.0	- 20V	75	150	HIOV TURTU
Output Fall Time		80.0	0		tTHL		01			0.10.0	ns
tTHL = (2.16 ns	/pF) CL	+ 52 ns		-	80.0	5.0	15	_	160	320	
tTHL = (0.96 ns				4.85	- 8	10	5.0	HOY	80	160	
tTHL = (0.69 ns				88.8		15	10	-	65	130	Vin 0 of
Propagation Delay 1			25	14.93	tacc(R)	19.8	GI.	1			ns
Read Access Tim					-acc(n)			VNL			nomm) szio
tacc(R) = (1.		Cı + 385	ns acc	ar		5.0	5.0	-	455	750	P (UoV)
tacc(R) = (10).7 ns/pF) Ci + 175	5 ns	3.0	- 1	10	10	-	210	400	100 V 1
tacc(R) = (0.	5 ns/pF)	CI + 105	ns aca	4.5		15	15	-	130	300	P JugVA
Strobe Down Time	1.5	-	2.28	1.5	tWL	111	6.0	Venu		(abV 8.0	ns
				3.0	-44.	5.0	07	500	100	(±V0.1	= JugV-J
				4.5		10	91	125	50	1 b V de 1	3100 V-1
						15		95	75		7300
Address Setup Time		-		0.1		10	0.0	1 100	CHOICE	JAI menu.	ns
nuuress setup i ime					t _{su}	5.0	5.0	300	-100	- Caby S	1.16
						10	0.6	120	-40	HobV d	1
						15	115	90	-25		1
		1	-3.5	8.1-		10	-	90	-25	B V de	
Data Setup Time	81.0				t _{su(D)}	5.0	0.0	JO	Sink	(obV)	
						5.0	07	200	70	-tobV i	
				1.7		10	91	75	25	- ValeV	100
sbAm						15		55	20	Junean (CL)	tiput Drivid
Read Setup Time			-1.7		t _{su(R)}	2.7-	0.8		Saurce		ns V
					- 1	0-5.0	0.8	270	90	HobV 6	
					- 1	10	01	60	20		16 = HOAL
	0.1-	-	-2.5	5.7-	- 1 3	15	81	45	15	₩bV 8.	NOV!
Write Setup Time	1.0	1	0.35	0.16	t _{su} (W)	0.2	0.8	JOL	Sink	(Vdc)	0 = ns VI
					-	5.0	10	400	80	-(abV)	
			4.5		- 1	10	15	100	25	-€obV i	IVOL = 1
					7.0.±	15	15	75	11	(AL Device)	nonu Curren
Address Release Tin	ne	0.1±	1000000		trel(R)		81	1 7	lad	(C) (CP Dev	ns ns
	-				101(11)	5.0	-	75	15	530	dur Cagagia
						10		25	10	- 5.500	(0 = mV)
						15	-	20	5.0	_	10 - W -1
Data Hold Time		0.0	230.0		\$1.701		0.0	90	100	40 101 ton	ns.
					th(D)	5.0	10	50	0	(8)	(Pg an pack)
					20	10	15	15	0		
					68	15	5.0	10	0 =51490	rent (CL/CP	nescent Cur
Read Release Time	-	607	0.100		2-1/21		-01				ns
ייים וייים מפסים וייוופ					trel(R)	5.0	15	0	-90		118
phylic		cool + 1				10	5.0	0	-25	T** Inemu	ital Supply
		001+1				15	10	0	-10	slus Quiesces	(Dynamid)
Write Release Time		autor	Ismateria de	101-13	9 4000		-01			101	
Attite Lielegze i IW6					² rel(W)	5.0		0	5.0	F on all ourg	08 NS
						10		0	10	(tehing)	Sulfars se
					1.01	15	215	0	30	chage Curre	ree-State L
						15	-	-	30	1	Sept 101
Read Cycle Time					tcyc(R)		15		F00	STORAGE SE	UISIC DON
						5.0		-	500	750	ICL/CP D
						10			200	400	
SICHMENT	SV MIZ					15			150	300	
Write Cycle Time					tcyc(W)		.60		10°00 - 10°0	C YOU ALL D	ns ns
or CE ggV						5.0	evic	for GERGP	440	700	Thigh = +12
						10	rania	moo Tuoni e	275	560	Noise immu
or EE ma	TA	- X				15	50	orly redition that	200	10.415	To colculate
Output Diseble Dele	BY SAF	3 122			^t dis			00 V 108-	3) 4-01 × 1+	HI 00171 =	ns
(10% Output Ch	ange inte	0 1.0 kΩ L	.oad)	yoneupes?	RHE IS INPUL	0.0	bV s	igf, Vogi	200	600	where: I'm
		-				10	ino.	haractaristic	80	200	The formula
						15			60	150	1

^{*} The formulae given are for the typical characteristics only.

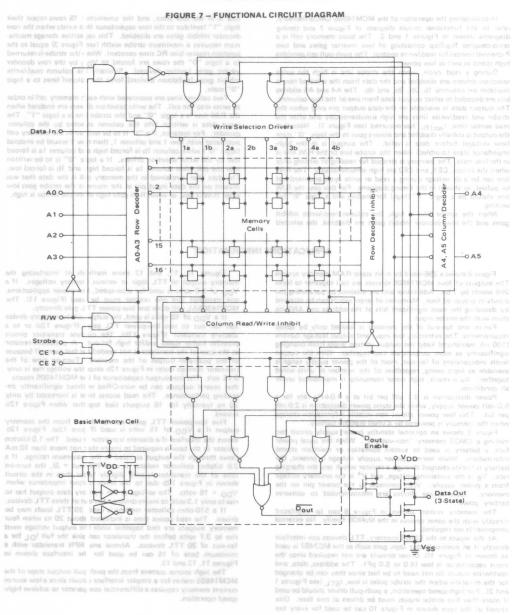
FIGURE 1 - READ CYCLE TIMING DIAGRAM







DPERATING CHARACTERISTICS



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 7 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The Ad and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{\rm acc}(R)$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the RM line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The RM line is no be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the RM line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected

row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to VpD by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 8 shows a 256-word by n-bit static RAM memory system The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μ W per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 9 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. Vg is the sustaining voltage, and V* is the ordinary voltage from a power supply. VDD connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 8 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 10. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, tSTL (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 10 can be used for every ten strobe inputs.

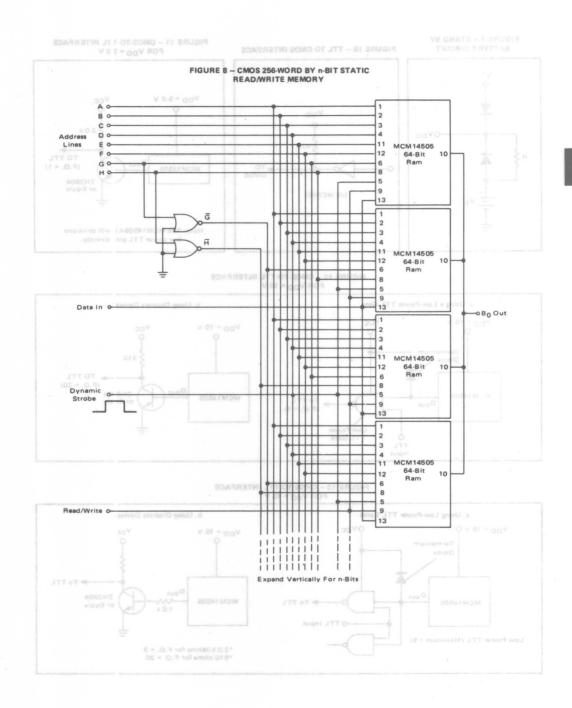
Figures 11, 12, and 13 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 11). The MCM14505AL will drive one low-power TTL gate directly.

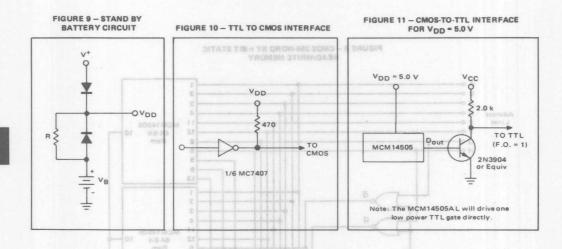
If a VDD of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 12a) or to a discrete transistor (Figure 12b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 12b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 12b

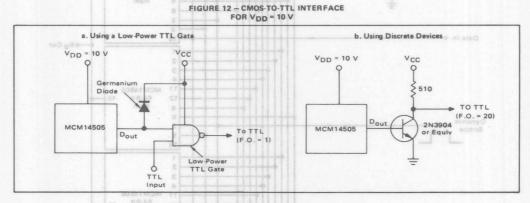
Five low-power TTL gates can be driven from the memory DDD of 15 volts is used (Figure 13a). Figure 13b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 12b due to the lower output impedance when $V_{\mbox{\scriptsize DD}}=15$ volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

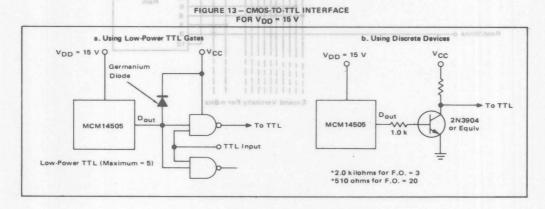
If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 11, 12 and 13.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.











MC14511B

BITCHTO

							80	ELECTRICAL CHARTACHERIST
	"via			25°C				
ziniJ	NeN	nifit	Max	qyT			Symbol	Churacteristic
Vdc	0.05			0			JoV	Serie L''D'' egasieV-tueruD'

3.40

08.8

0.87

2,80

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

9.04

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS).

Vdc	Rating	88	Symbol	Value 01.8	Unit
DC Supply Volt	age	.26	VDD	-0.5 to +18	Vdc
Input Voltage, A	All Inputs	111	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Dra	n per Input Pin	00	Inc. o	10	mAdc
Operating Temp	erature Range — AL Dev CL/CP Dev	-0.7	TA	-55 to +125 -40 to +85	°C
Storage Tempera	ature Range	1.27	T _{stg}	-65 to +150	
Maximum Outp (Source) per	ut Drive Current Output	1.18	OHmax	_25 ac.ar	mA
Maximum Conti (Source) per	nuous Output Power Output ‡	88,1 08.1	POHmax	-50 [.8]	mW

POHmax = IOH (VDD -VOH)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

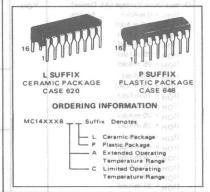
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratinos).

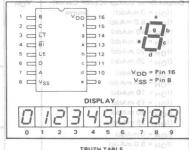
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT





		NPUT	S		_	_	_		uhy	λæ	OU	TP	UTS	6.11
LE	BI	LT	D	С	В	Α	а	b	C	d	0	f.	9	DISPLAY
X	X	0	×	×	×	×	1	1.	ot.	1	.1:	1.	1	8
X	.0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1 1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	11	0	0	0	1	0	1	1.	0	0	0	0	Stri 1
0	1	1	0	0	90	0	1	1.	0	1	1	0	41	2
0	1	1	0	0	1	1	1	1	10	\1	0	0	1	W 3
0	1	1	0	1	0	0	0	1	1	.0	0	1.	1	(V) 4
0	1	- 1	0	1	0	1	1	0	1	1	0	1	-19	5
0	-1	1	0	1.	1	0	0	0	1	1	.1	1	-1	6
0	1	1111	0	1	1	10	1	1	1	0	0	0	0	ucur 7
0	1	1.	1	0	0	0	1	1	1	1	1	1	ri	8
0	1	1	1	0	0	1	1	1	1	0	0	01	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	-1	-1	-1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	٥	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	×	×	X			_				_	

- X = Don't Care
- *Depends upon the BCD code previously applied when LE = 0





FL FCT	TRICAL	CHARAC	CTERISTICS

		V _{DD}	Tlov			25°C	I 88	Thi	gh Max	Unit
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	0.05	Vdc
utput Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	_	0.05	Vuc
V _{in} = V _{DD} or 0		15	038101	0.05	1000-01 to	0	0.05	39-831	0.05	
"1" Level	VOH	5.0	4.1	-	4.1	4.57	-	4.1	-	Vdc
Vin = 0 or VDD	TOH	10	9.1	oder <u>/</u> dris	9.1	9.58	100-52/01	9.1	8 MC145	
TIN SS. SDD		15	14.1	109 <u>0</u> 01000	14.1	14.59	M youthe	14.1	ritius bs	struc
put Voltage# "0" Level	VIL		SUMPLIE	SHUILDE	audia tud	R UI SJAN	um sindi n	o ligoriar o	ALAN OUR	Vdc
(V _O = 3.8 or 0.5 Vdc)	"	5.0	an <u>B</u> 42	1.5	note_tide	2.25	1.5	u sapive	1.5	ine
(VO = 8.8 or 1.0 Vdc)	1	10	ty. Lamp	3.0	ivi ituq	4.50	3.0	egment o	3.0	
(V _O = 13.8 or 1.5 Vdc)	8	15	1201 AT, ba	4.0	qni (d.d.)	6.75	4.0	(18)+pnu	4.0	1891
(V _O = 0.5 or 3.8 Vdc) "1" Level	VIH	5.0	3.5	brigatine	3.5	2.75	Md 30 4	3.5	is walds	Vdc
(V _O = 1.0 or 8.8 Vdc)		10	7.0	90 FB2 1	7.0	,5.50	0024308	7.0	97 DAG 39	displa
(V _O = 1.5 or 13.8 Vdc)		15	11.0	scen4, flu	11.0	8.25	PORE-BUILD	11.0	205miges	riavas
Output Drive Voltage (AL Device)	VOH		Vilasnos		THE TOTAL	esdoors !	etskio	biupil 10		Vdc
(IOH = 0 mAdc) Source:		5.0	4.10	MYO.	4.10	4.57	nurteni.	4.1	noneand	DAY.
(I _{OH} = 5.0 mAdc)	100		ay deixelf.	cpit d isp	3.90	4.24	notalinal	3.5	TOD TOVIT	plays
(I _{OH} = 10 mAdc)	158		3.90		3.90	3.94	n, and tin	OK, Wate	DID STIGITS	v bris
(I _{OH} = 15 mAdc)	V lot		3.40		3.40	3.75	10-03	3.0	A	0 0
(I _{OH} = 20 mAdc) (I _{OH} = 25 mAdc)	1		3.40	5bV)	3.40	3.54	0.0 nA/s	7 70091310	O JUROISH	
	1 3	10	9.10	_	9.10	9.58	-	9.1	-	Vdc
(I _{OH} = 0 mAdc) (I _{OH} = 5.0 mAdc)	CERAL	10	3.10	_	25 mA)	9.26	egto0 gr	t Source	gh-Curren	H 6
(IOH = 10 mAdc)	p : 1		9.00	_	9.00	9.17	- 5	8.6	tch Stora	6. La
(IOH = 15 mAdc)		3	-	-	-	9.04	-		ed official	10 0
(I _{OH} = 20 mAdc)			8.60	-	8.60	8.90	-	8.2	ara Galesia	10
(IOH = 25 mAdc)	KENDA		-	_	-	8.75	-	udisīno.	150 T du	0 1
(IOH = 0 mAdc)		15	14.1	-300	14.1	14.59	all Lites	14.1	adout Bh	Vdc
(I _{OH} = 5.0 mAdc)			-	-	-	14.27) notice	boM vrid	mp Inten	3.0
(IOH = 10 mAdc)	1.		14.0	-	14.0	14.18	-	13.6	-	T e
(I _{OH} = 15 mAdc)			-	-	-	14.07	xing), Fa	editinisti	ne Share	
(IOH = 20 mAdc)		13	13.6		13.6	13.95	0.5 = 0	13.2	IloV Vigg	15 0
(IOH = 25 mAdc)			THE PROPERTY OF	I and	iso I II	13.80	in Law	nn Wa G	30 slden	0.0
Output Drive Voltage (CL/CP Device)	VOH		be		pads Ove	J JTH O	T 10 ba	4.1		Vdc
(IOH = 0 mAdc) Source	1	5.0	4.10	-	4.10	4.57	.00	raff snut	Tempera	T LK
(IOH = 5.0 mAdc)	1 200	1	3.60	-	3.60	4.24	- /	3.3		
(IOH = 10 mAdc)	m: 3	1	3.00		3.00	3.94		-		-
(I _{OH} = 15 mAdc) (I _{OH} = 20 mAdc)	P		2.80	_	2.80	3.75	-	2.5	= 2	l della
(I _{OH} = 25 mAdc)		Tares de Line	-	-	(2	3.54	grater tag	ata¥1 88	BATTIN	MUBBIN
(IOH = 0 mAdc)	5	10	9.10	Notes V	9.10	9.58	-	9.1	-	Vdc
(I _{OH} = 5.0 mAdc)	de la	obv	- 50	es ≥0-	7105	9.26	-	-	secrio	/ ylanui
(I _{OH} = 10 mAdc)		by	8.75	av to al	8.75	9.17	-	8.45	BOST TA A	satto V z
(IOH = 15 mAdc)		obAn	-	A.F	-	9.04	-	nist more	d read of the	TORUM.
(I _{OH} = 20 mAdc)	101	20	8.10		8.10	8.90	- Tuesday	7.8	000000000000000000000000000000000000000	T onlin
(I _{OH} = 25 mAdc)	[3.3]	1 0	- 00	- 01 00-	-A1	8.75	1000	-		ar Same
(IOH = 0 mAdc)	0	15	14.1		14.1	14.59	-	14.1	P and to you	Vdc
(IOH = 5.0 mAdc)		-	-00	* 00 00-	7015	14.27	-	August 1	and the same	O muse
(IOH = 10 mAdc)	-	Am	13.75	95-	13.75	14.18	-	13.45	turned se	Tambos
(IOH = 15 mAdc)	B 127	-			-	14.07	-		The second second	
(I _{OH} = 20 mAdc)	1 2	Ville	13.1	00-	13.1	13.95 13.80	- 769	12.8	THE CARTON	increased
(I _{OH} = 25 mAdc)	1		-			13.00	-	- 1	100	mAc
Output Drive Current (AL Device)	IOL	5.0	0.64		0.51	0.88	_	0.36	BOAL HOL	mAc
(V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc)	1 0	10	1.6		1.3	2.25	_	0.9		
(VOL = 1.5 Vdc)	1 8	15	4.2	uds -	3.4	8.8	1000	2.4	n animum	and a second
Output Drive Current (CL/CP Device)	le:	011	207 00 21	girustness:	Isavion 1	of bearing	87 71 380	evior an	HT ordoule	mAc
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	t ampation	0.44	0.88	higher to	0.36		bildes p
(VOL = 0.5 Vdc)	1 2	10	1.3	TE NEW Y	1.1	2.25	igh_cum	0.9	do A_diu	nio eani
(VOL = 1.5 Vdc)	7 8	15	3.6	-	3.0	8.8	Vin or M	2.4	nan aftr of	beniani
	1 1 5 1	1 80	Ox mades	u gift ur s	GOOD TIED S	germen pri	ONE CHO	o Assistand	ea Bujainh	9717 02
HIS 0 0 0 0 0 0 0 0 1 1 1 1 1 1 4 10 0 0 0					01 8 10 000	pue SSA	os botro		dino aut	
A10 0 0 0 0 0 0 0 1 1 1 1 1										
						endordes	ns of her	ed skew		

ELECTRICAL CHARACTERISTICS (Continued) (Co

		VDD	Tic	w*		25°C		Th	igh "	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Input Current (AL Device)	l _{in}	15	IN ARATA	± 0.1	ot Be suc	±0.00001	±0.1	_	± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	Signal of	± 0.3	79102717	±0.00001	±0.3	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)	Cin		-	-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device) (Per Package)	I _{DD} -	5.0 10 15	1000	5.0 10 20	9 pn	0.005 0.010 0.015	5.0 10 20	-	150 300 600	μAdc
Quiescent Current (CL/CP Device) (Per Package)	IDD HOV-	5.0 10	0 1400 I	20 40 80	- - -	0.005 0.010 0.015	20 40 80	_ _ _	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	10 A -	5.0 10 15	J 1000	1	IT = (1.9 μΑ/kHz 3.8 μΑ/kHz 5.7 μΑ/kHz) f + IDD			μAdc

^{*}Tlow = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

SWITCHING CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

Cheracteristic	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Output Rise Time tTLH = (1.5 ns/pF) C _L + 50 ns tTLH = (0.75 ns/pF) C _L + 37.5 ns tTLH = (0.55 ns/pF) C _L + 37.5 ns	tTLH	5.0 10 15	-	40 30 25	80 60 50	ns
Output Fall Time	TTHL	5.0 10 15	=	125 75 65	250 150 130	ns
Data Propagation Delay Time tp_H = (0.40 ns/pF) C _L + 620 ns tp_H = (0.25 ns/pF) C _L + 237.5 ns tp_H = (0.20 ns/pF) C _L + 165 ns	tpLH	5.0 10 15	=	640 250 175	1280 500 350	ns
tpHL = (1.3 ns/pF) CL +655 ns tpHL = (0.60 ns/pF) CL + 260 ns tpHL = (0.35 ns/pF) CL + 182.5 ns	PHL	5.0 10 15		720 290 200	1440 580 400	ns
Blank Propagation Delay Time tp_H = (0.30 ns/pF) C_L + 305 ns tp_H = (0.25 ns/pF) C_L + 117.5 ns tp_H = (0.15 ns/pF) C_L + 92.5 ns	ФЦН	5.0 10 15	D rugil	600 200 150	750 300 220	ns
tpHL = (0.85 ns/pF) C _L + 442.5 ns tpHL = (0.45 ns/pF) C _L + 177.5 ns tpHL = (0.35 ns/pF) C _L + 142.5 ns	ФНГ	5,0 10 15	Ουτρυτ	485 200 160	970 400 320	ns
Lemp Test Propagation Delay Time tp_H = (0.45 ns/pF) C _L + 290.5 ns tp_H = (0.25 ns/pF) C _L + 112.5 ns tp_H = (0.20 ns/pF) C _L + 80 ns	tPLH .	5.0 10 15	-	313 125 90	625 250 180	ns
tpHL = (1.3 ns/pF) CL + 248 ns tpHL = (0.45 ns/pF) CL + 102.5 ns tpHL = (0.35 ns/pF) CL + 72.5 ns	PHL	5.0 10 15	- -	313 125 90	625 250 180	ns
Setup Time	t _{su}	5.0 10 15	180 76 40	90 38 20	-	ns
Hold Time	th	5.0 10 15	0	-90 -38 -20	- - -	ns
Latch Enable Pulse Width	\$WL	5.0 10 15	520 220 130	260 110 65	=	ns

^{*} The formulae given are for the typical characteristics only.

Noise Margin for both "1" and "0" level =

^{1.0} Vdc min @ V_{DD} = 5.0 Vdc

^{2.0} Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

[†]To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} \text{ (C}_L -50) \text{ V}_{DD}f$ where: IT is in µA (per package), CL in pF, VDD in Vdc,

and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 - DYNAMIC POWER DISSIPATION 20172193TOARAMO JACISTOSIJS

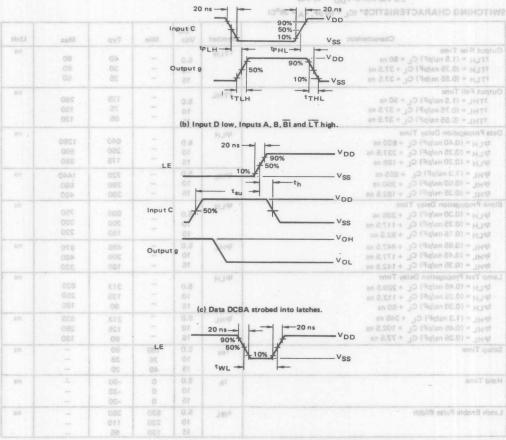
	"ris				SIGNAL WAVEF	ORMS		
	nabl			Min Typ		Vdc	Symbol	Characteristic
				10000 Olnput LE	low, and Inputs D, B	and LT	nigh.	input Current (AL Device)
obAu	0.11				et to a system clock.	l ar	ni ¹	
			7.6	0.8	uts connected to respe	-	oads.	Input Capaditance IV _{in} = 0)
abAu.				- 0.005	0.0	20 ns	VDD	
				A, B, and C	90%	01/	00	(Per Package)
				9100 -		10%	V _{SS}	
		-			05 - 1/f -	5,0	00	Quiescent Current (CL/CP Device)
	300		- 04		50% Duty 0	ycle Of		(Per Packaga)
				9100 -	OB/T	ar/	VOН	
			001+1	Any Output		er er	VOL	Total Supply Current**1 (Dynamic plus Quinscent, Per Package) (Cr. 2 SQ oF on all outputs, all buffers switching)

*Trow = -55°C for AL Device, -40°C for CL/CP Device. † To calculate total supply current at leads other than 50 pF.

Thigh: * 125°C for AL Device, *85°C for CL/CP Device. † Trick properties at 10°3 (CL -50) Vppf.

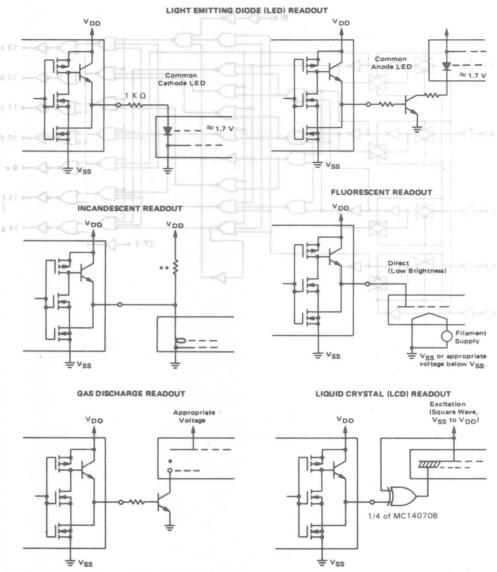
#160180 Instrumently specified for worst case in Comparable Margin Figure 2 — Dynamic Signal Waveform Dynamic Volta in the section of the Margin for both """ and "0" level "" and "0" level """ and "0" level "" and "0" lev

(a) Inputs D and LE low, and Inputs A, B, BI and LT high.



The formulae given are for the typical characteristics only.

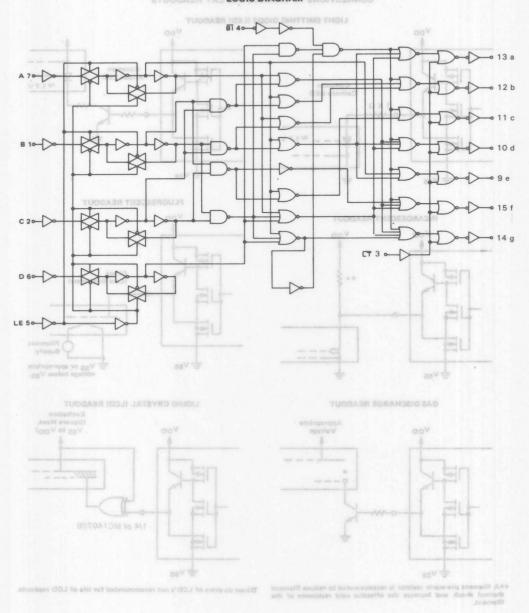
CONNECTIONS TO VARIOUS DISPLAY READOUTS



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

STUDGA 3 N VA LOGIC DIAGRAM SHOTTO SHIP





MC14513B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- · Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Input Pin	11 000	10	mAdd
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	
Maximum Continuous Output Drive Current (Source) per Output	IOHmax	- 25	mA 01
Maximum Continuous Output Power (Source) per Output ‡	POHmax	- 50 - - 8.78	mW

POHmax = IOH (VDD - VOH)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

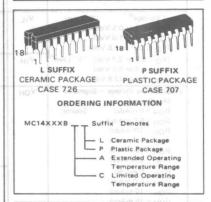
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (see Maximum Ratings).

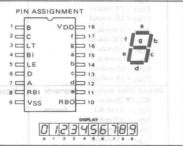
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING





						T	RUT	TH TAB	E.							
		11	NPUTS					OUTPUTS								
RBI	LE	BI	LT	D	C	В	A	RBO	0	b	c	d		1	9	DISPLAY
X	X	X	0	X	X	X	X	- 5	1	1	1	1	1	1	1	. 8
×	×	0	1	×	X	×	Х	-	C	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	. 1.	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
×	0	1	1	0	0	1	0	0	-1	1	0	1	1.	0	3	2
×	0	1	1	0	0	1	1	0	. 1	1	1	1	0	0	. 1	3
×	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
×	0	1	1	0	1	0	1	0	1	0	1	1	0	-1	. 1	5
×	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
×	0	1	1	0	1	1	1	0	12	1	1	0	0	0	0	7
×	0	1	1	1	0	0	0	0	1	1	1	1	1	Ŷ	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	(1)	13	9
×	0	1	1	- 1	0	1	0	0	0	0	0	0	0	0	.0	Blank
×	0	1	1,	1	0	1	1	0	0	0	0	0	0	0	0	Blank
×	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
×	0	1	1	1	1	0	1	.0	0	0	0	0	0	0	0	Blank
×	0	1	1.	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	. 1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
×	1	1	1	×	×	×	×									

- X Don't Care
- = RBO RBI (□€€4) indicated by other rows of table.

MC14513B



ELECTRICAL CHARACTERISTICS

		VDD	Tio			25°C			igh*	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage - Segment Outputs	VOL									Vdc
"0" Level	-	5.0	BRIVER	0.05	MADEC!	0	0.05	VEN SE	0.05	GOS
V _{in} = V _{DD} or 0		10 15		0.05	-	0	0.05		0.05	-
1281 2080			- mint	- House by	olai Inc		0.05	e ocia	1010 0	(T.
Level -	VOH	5.0	4.1	nhancer	4.1 9.1	5.0	demiintar	4.1 9.1	v betou	Vdc
Vin = 0 or VDD	000	10 15	9.1	ionom s	14.1	15	eqtuo is	14.1	4 bas a	devic
Output Voltage - RBO Output	1/	10	a done	geroje j	J-9 8 10	mortonia	वार्धि कार्य	PORCE PRO	nio self	Vdc
"0" Level	VOL	5.0	diffidaces	0.05	atuo ne l	0	0.05	pez nevez	0.05	Vac
V _{in} = V _{DD} or 0	0	10	BEU STE E	0.05) eldene	0	0.05	pinsid (0.05	Lame
THE RESTRICTION OF THE PARTY OF	NJ	15	to assertific	0.05	Induboro	0 0	0.05	splay, te	0.05	10 18
TI Level	VOH	5.0	4.95	I Vela	4.95	5.0	E_8101	4.95	,velqu	Vdc
V _{in} = 0 or V _{DD}	*OH	10	9.95	BRI TUO	9.95	10	diff_bns	9.95	gnL pni	Inel8
VIII O OL V DD		15	14.95	od (460.1)	14.95	15	lead-ing	14.95	ICCHE IO	bezu
nput Voltage# "0" Level	VIL	,	t. fluore	nodescen	pm (C)	J) anboi	politic	s tripil	mampee	Vdc
(VO = 3.8 or 0.5 Vdc)	VIL	5.0	o vizoeti	1.5	enuébse	2.25	1.5	. seasont	1.5	Joso
(V _O = 8.8 or 1.0 Vdc)	1889	10	-	3.0	_	4.50	3.0	-	3.0	indice
(V _O = 13.8 or 1.5 Vdc)	T PRET	15	illa frata	4.0	atru-en	6.75	4.0	holoed a	4.0	Δ
(V _O = 0.5 or 3.8 Vdc) "1" Level	VIH	5.0	3.5	pxipep .	3.5	2.75	teliminal	3.5	194110	Vdc
(V _O = 1.0 or 8.8 Vdc)	HI	10	7.0	-	7.0	5.50	Hotest 4	7.0	sv bas	swinb
(V _O = 1.5 or 13.8 Vdc)	CERAIN	15	11.0		11.0	8.25	1100000,00	11.0	av one ,	26110
Output Drive Voltage - Segments	VOH	1.0	1	- Shirt a	ED TROUB	10000000	50000	E the nic	theres	Vdc
(AL Device)	HOV		1	-		noissgia	ower Die	Circuit F	w Logic	DJ Vac
(IOH = 0 mAdc) Source:		5.0	4.10	-	4.10	4.57	otuO si	4.1	011142-rh	H o
(I _{OH} = 5.0 mAdc)	MCM	0.0	-	-	-	4.24	ant via	10 L	and done	1.0
(I _{OH} = 10 mAdc)	DI DW		3.90	-	3.90	4.12	office A see	3.5		
(I _{OH} = 15 mAdc)			-	-	-	3.94	-	3/1/0	in length	is e
(IOH = 20 mAdc)			3.40	-	3.40	3.75		3.0	tre L qu	6.1.0
(IOH = 25 mAdc)			-	7000	isal d mo(3.54	all+lla-r	o amistra	a reobs	P Re
(IOH = 0 mAdc)		10	9.10	-	9.10	9.58	nottalu	9.1	sated ore	Vdc
(IOH = 5.0 mAdc)			-	-	-	9.26	A MANAGEMENT		-	T 8
(IOH = 10 mAdc)		1	9.00	-	9.00	9.17	sO (griixs	8.6	preug eu	
(I _{OH} = 15 mAdc)			2118	PFOM of	tuQ_gnii	9.04	dill til b	e Blankin	ds Bipp	DA P
(IOH = 20 mAdc)	1819		8.60	-	8.60	8.90	0.8- 00	8.2	oV ylee	0 Su
(IOH = 25 mAdc)			Anno Trans	1.000 3	to I II	8.75	As Court	nation.	to alden	0.0
(IOH = 0 mAdc)	E.	15	14.1	rsyO s	14.1	14.59	or bso.	14.1	Sohottle	Vdc
(I _{OH} = 5.0 mAdc)	The last		dans aur	1000	D807 7	14.27		77.11		
(IOH = 10 mAdc)	B. 1		14.0	-	14.0	14.18	00	13.6	Tampen	
(OH = 15 mAdc)	500		-	-	-	14.07	-		HATIN	WILINI)
(IOH = 20 mAdc)	Eno .	-	13.6		13.6	13.95	ges raters	13.2	nt (24n	atratait >
(I _{OH} = 25 mAdc)	123	tinit	-	uls¥	Hode	13.80	-	philo	-	
Output Drive Voltage - Segments	VOH	Vdc	81-	-0.5 to	00				oltage	Vdc
(CL/CP Device) as cooper	De	obV	8.0 + 0	0.6 to Vg	- 440	457		221	gn1 lt/k g	geHaV I
(IOH = 0 mAdc) Source:		5.0	4.10	01	4.10	4.57		4.1	rain par	Jagyan
(I _{OH} = 5.0 mAdc)		30	3.60	01 38-	3.60	4.24	AL Device	3.3	nuteroge	eting Te
(I _{OH} = 10 mAdc) (I _{OH} = 15 mAdc)			3.00	or GA-	3.00	3.94	CP Device	10 3.3		
(I _{OH} = 20 mAdc)			2.80	os_20-	2.80	3.75	1 _	2.5	enuinte.	meT se
(I _{OH} = 25 mAdc)		Am	-	ac	2.00	3.54	ive Gerne	0.1-000	ano-nito	O mum
(I _{OH} = 0 mAdc)		10	9.10	-	9.10	9.58	-	9.1	antico sar	Vdc
(I _{OH} = 5.0 mAdc)	X X	Wen	9.10	na -	9.10	9.36	- 1000	9.1	n extending	vuc
(IOH = 10 mAdc)	IX X	T TOOL	8.75		8.75	9.17	- 1011	8.45	notieD and	(acress)
(IOH = 15 mAdc)	10.0	-	-	_	0.70	9.04	-	0.40	-	1000
(I _{OH} = 20 mAdc)	0 2	1 -1 - 5	8.10	-	8.10	8.90	_	7.8	DV) HOT	" xamil-
(I _{OH} = 25 mAdc)	0 X	-	-	-	-	8.75	-	-	_	-
(IOH = 0 mAdc)	0 4	15	14.1	- reprincia	14.1	14.59	parond of	14.1	emissinos	Vdc
(IOH = 5.0 mAdc)	P X	to me	167 50 mo	preceus	sorton 190	14.59	11 ,18V0	ved table	olafosla	Vuc
(I _{OH} = 10 mAdc)	0 2	-baqn	13.75	oltages to	13.75	14.27	on might s	13.45	70 Horis	iriqqa bi
(IOH = 15 mAdc)	12 2 1		10.70	V _{in} and	10.75	14.10	VI m	13.45	smarr of a	bt beni
(IOH = 20 mAdc)	0 2		13.1	- No 1	13.1	13.95		12.8	_	
(IOH = 25 mAdc)	0 8		reld-need	Jactical	10 700	13.80	bueno de	.2.0	un atri	on ball
- Off		1000	PEIN SEE	1001901	10 316 0	1.0.00	MAX SOLD	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	and sold to	10 (1194)

2

ELECTRICAL CHARACTERISTICS (Continued)

			VDD	Tlo	w*		25°C		Thi	gh °	
		Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Drive Current - RE	30 Output	ТОН	abV]	Symbol			28	rii tutore	(C)		mAdo
(AL Device)		011		HAT?				gtunteO		300 30	THEFT
(VOH = 2.5 Vdc)	Source	- 1	5.0	-0.40	-	-0.32	-0.64	-	-0.22	-	
(VOH = 9.5 Vdc)		- 1	0/10	-0.21	-	-0.17	-0.34	_	-0.12	_	
(V _{OH} = 13.5 Vdc)			8115	-0.81	-	-0.66	-1.3	-	-0.46	-	
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.18	-	0.15	0.29	- 100	0.10	- 9m=1 5s	mAde
(VOL = 0.5 Vdc)			10	0.47	-	0.38	0.75	_	0.26	1-	
(VOL = 1.5 Vdc)		- 1	0115	1.8	-	1.5	2.9	-	1.0	-	
Output Drive Current - RE	30 Output	ГОН	61								mAdd
(CL/CP Device)				11477				at not no	Segment	- BIT 11 II	1 mg
(VOH = 2.5 Vdc)	Source	-	5.0	-0.25	-	-0.21	-0.64	_an 0	-0.17	an iLi	CHTH
(VOH = 9.5 Vdc)		- 1	10	-0.13		-0.11	-0.34	37.5.76	-0.092	in 81_0	THE
(V _{OH} = 13.5 Vdc)		-	3115	-0.52	-	-0.44	-1.3	37 5205	-0.36	in 64_0	JHTI
(V _{OL} = 0.4 Vdc)	Sink	loL	5.0	0.12	-	0.098	0.29	-8500	0.080	in Lane	mAd
$(V_{OL} = 0.5 \text{ Vdc})$		- 1	10	0.30	-	0.25	0.75	_an 0i	0.21	en dut	THAT
(VOL = 1.5 Vdc)		- 1	0115	1.2	-	0.98	2.9	37.5-01	0.80	n 25_1	THIT
Output Drive Current - Se	gments	IOL	(6)					en e. v.	TOLLOR	an ee or	mAdo
(AL Device)				HTA			83.1/Q7	1.0.5.8	.A - 91111	Veta Char	1995-00
	Sink		5.0	0.64	-	0.51	0.88	sm 028	0.36	In 02 0	H1di
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.6	-	1.3	2.25	237 <u>5</u> ns	0.9	en (22.0)	11/1/91
(V _{OL} = 1.5 Vdc)		-	15	4.2		3.4	8.8	8 <u>44</u> 084	2.4	m (=,0)	H1197
Output Drive Current - Se	gments	loL	D.C	THds				8N 66	8 + 73 (±	Perts S. C.	mAdd
(CL/CP Device)			-07					an 0.85		1000	744
	Sink		5.0	0.52	-	0.44	0.88	182. <u>8</u> ns	0.36	-	11145
$(V_{OL} = 0.5 \text{ Vdc})$			10	1.3	-	1.1	2.25	haqn Li	0.9	yzimi m	HERMAN
(V _{OL} = 1.5 Vdc)	800	_	15	3.6	-	3.0	8.8	308 #4	2.4	in 0±01.	H.197
Input Current (AL Device)	000	lin	15	-	±0.1	_	±0.00001	±0.1	4 77 Lad	±1.0	μAdd
Input Current (CL/CP Devi	ice)	lin	15	_	±0.3	-	±0.00001	±0.3	130130	±1.0	μAdd
Input Capacitance (V _{in} = 0)		Cin	01	THAN	-	-	5.0	7.5	+ 12 (34	en dado	pF
Quiescent Current (AL Dev	rice)	IDD	5.0	T hert	5.0	-	0.005	5.0	10 -	150	μAdo
(Pet Package)			10	FDM	10	-	0.010	10	- Th (3)	300	- undergo
300	200		15	-	20	-	0.015	20	7.30	600	190.97
Quiescent Current (CL/CP	Device)	IDD	5.0	-	20		0.005	20	4 (318)	150	μAde
(Pet Package)			10	THIS	40	-	0.010	40	1 .5 (36)	300	1000
000	200		15	7111.	80	_	0.015	80	T.9.	600	11111
Total Supply Current**†		_IT	5.0				.9 μA/kHz)			ien हेर हो।	μAdd
(Dynamic plus Quiescer	nt,		10	HJR			.8 μA/kHz)				I ROSCO:
Per Package)		- 1	15	7442		$I_{T} = (5$.7 μA/kHz)	+ IDD			Legal
(CL = 50 pF on all outp	outs, all		01								404)
buffers switching)		- 1	15	-							112

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +25°C for CL/CP Device.

Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} \text{ (C}_L - 50) \text{ V}_{DD}f$ where: IT is in μA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

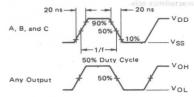
** The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 - DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

Input LE and RBI low, and Inputs D, BI and LT high.

f in respect to a system clock.

All outputs connected to respective CL loads.



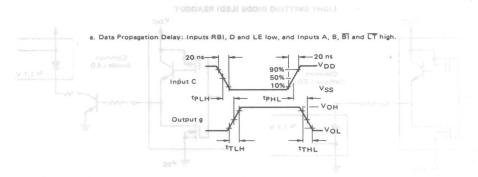
SWITCHING	CHARACTERISTICS*	* (C ₁ = 50 pF, T _A = 25°C)	

					COV		All Types		
Max Min Max Unit			no.	Niki	VDD	Symbol			
Characteristic	:			Symbol	Vdc	Min	Тур	Max	Unit
Output Rise Time - Segment Outputs				tTLH				100	ns
					0.5.0	-	40	80	- HOA
					0110	-	30	60	HOV
- 80:0	6,1-	88.0-		18.0-	al 15	-	25	50	C HOV)
Output Rise Time - RBO Output			-	TTLH	0.3	101	Sink	[shV-Ad]	ns
			-		5.0	7"	480	960	= 10 A)
			-	8.1	10	-	240	480	" JOY)
StaAm					15	Juni T	190	380	dr.C. sport
Output Fall Time - Segment Outputs				tTHL				(spired	ag ns
tTHL = (1.5 ns/pF) CL + 50 ns			-	-0.25	5.0	-	125	250	- HOY
t _{THL} = (0.75 ns/pF) C _L + 37.5 ns			-		10	-	75	150	HOV
tTHL = (0.55 ns/pF) CL + 37.5 ns					15	-	65	130	FHAVI
Output Fall Time - RBO Outputs	0.29	880.0		TTHE	6.0	101	Sink	laby at	ns
tTHL = (1.5 ns/pF) CL + 50 ns			-	0.30	5.0	20.	270	540	
tTHL = (0.75 ns/pF) C1 + 37.5 ns					10	-	135	270	= 10VI
tTHL = (0.55 ns/pF) CL + 37.5 ns			-		15	-	110	220	5041
Propagation Delay Time - A, B, C, D In	puts			tPLH		100	21.0/5/(00)		ns
tpLH = (0.40 ns/pF) CL + 620 ns	88.0			NB.O	5.0	-	640	1280	
tp_H = (0.25 ns/pF) C _L + 237.5 ns					10	_	250	500	- TOA
tpLH = (0.20 ns/pF) CL + 165 ns					15	-	175	350	* TO/A)
tpHL = (1.3 ns/pF) CL + 655 ns		10.00	-		5.0		720	1440	- 10 41
tpHL = (0.60 ns/pF) CL + 260 ns				tPHL	10	TOL	290	580	ns ns
tpHL = (0.35 ns/pF) CL + 182.5 ns					15		200	400	(CL/CP
	86.0	0.44		0.62	U.C.	-	200	400	No.
Propagation Delay Time - RBI Input				tPLH .	10		000	(obV 8.0	ns
tpLH = (0.30 ns/pF) CL + 305 ns					5.0	-	600	750	- TOAL
tPLH = (0.25 ns/pF) CL + 117.5 ns			1.0		10	ni T	200	300	moDifug
tPLH = (0.15 ns/pF) CL + 92.5 ns			8.8		15	T	150	220	Jan. 3 Aug.
tpHL = (0.85 ns/pF) CL + 442.5 ns				tPHL	5.0	1 5	485	970	ns
tpHL = (0.45 ns/pF) CL + 177.5 ns					10	ats_	200	400	0 = 159
tpHL = (0.35 ns/pF) CL + 142.5 ns	200.0				15	-	160	320	S. St.
Propagation Delay Time - BI Input			-01	tPLH	0.0	GG.	1000	2 200 2007	ns
tpLH = (0.3 ns/pF) CL + 305 ns			00		5.0	-	600	750	1881 Fee
tpLH = (0.25 ns/pF) CL + 117.5 ns					10	-	200	300	
tpLH = (0.15 ns/pF) CL + 92.5 ns			00		15	00L	150	220	Dinequely
$tpHI = (0.85 \text{ ns/pF}) C_1 + 442.5 \text{ ns}$			03	^t PHL	5.0	-	485	970	ns
tpHL = (0.45 ns/pF) CL + 177.5 ns			68		10	- 1	200	400	
tpHL = (0.35 ns/pF) CL + 142.5 ns	SpA/kHz				15	TI-	160	320	oqu8 lets
Propagation Delay Time - LT Input	ZHATAN B	17 1 13		tPLH	107		(20)	e pros Usanto	ns
tpLH = (0.45 ns/pF) CL + 290.5 ns	7 pA/kida			11	5.0	-	313	625	Per Peo
tpLH = (0.25 ns/pF) CL + 11,2.5 ns					10	-	125	250	101 - 101
tpLH = (0.20 ns/pF) CL + 80 ns					15	- 1	90	180	pullers
tpHL = (1.3 ns/pF) CL + 248 ns				tPHL	5.0	1_/3=in? 3	313	625	ns
tpHL = (0.45 ns/pF) CL + 102.5 ns				THE	10		125	250	4950
tpHL = (0.35 ns/pF) CL + 72.5 ns					15	19 TOT 09	90	180	Tright T
Minimum Setup Time				nol	5.0	Comi sero	90	180	000
				tsu	10	= level	38	76	ns
are for the typical characteristics					15		20	40	V 0.1
Minimum Hold Time	(3)**(is to vino	-		-	1	- CO Y CO	Total Committee	400
Minimum Hold Time				th	5.0	-	-90	ov on ma	ns
	NO			O VINAME PO	10	-	-38	0	
			MROT	SYAW JANDIS	15	-	-20	0	
Minimum Latch Enable Pulse Width			50	tWL(LE)	5.0	-	260	520	ns
	inged T		, LI 87118		10	egni_	110	220	10074
				a system ciock.	15	TOTAL TOTAL	65	130	

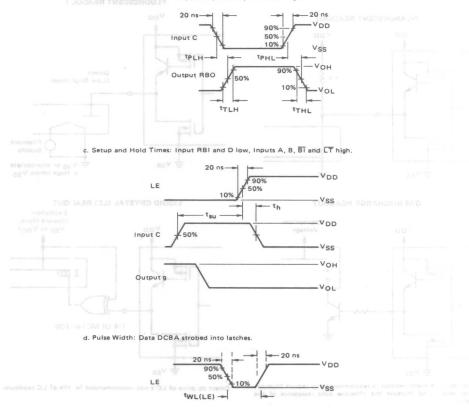
^{*} The formulae given are for the typical characteristics only.



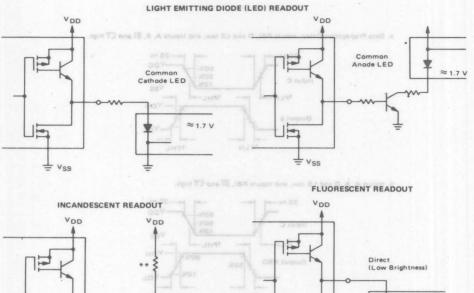
FIGURE 2 - DYNAMIC SIGNAL WAVEFORMS

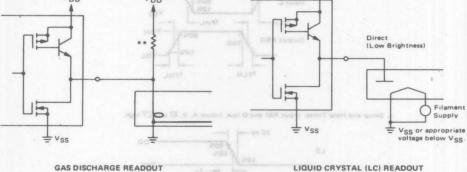


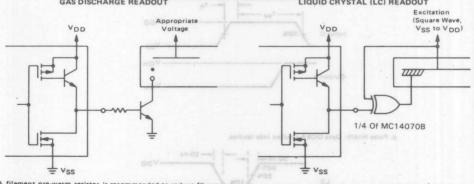
b. Inputs A, B, D and LE low, and Inputs RBI, $\overline{\text{BI}}$ and $\overleftarrow{\text{LT}}$ high.



CONNECTIONS TO VARIOUS DISPLAY READOUTS

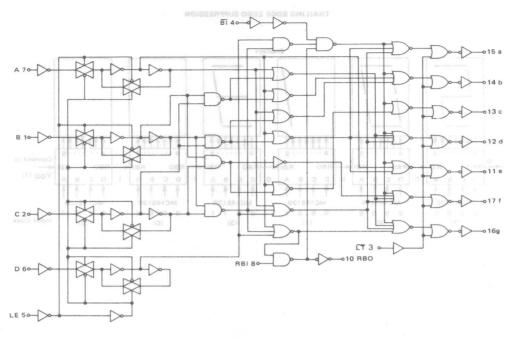






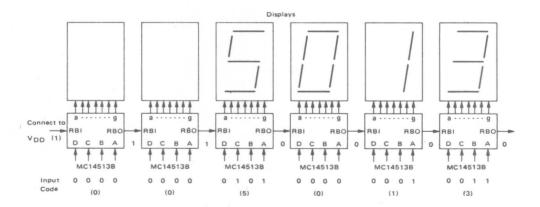
**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LC's not recommended for life of LC readouts.



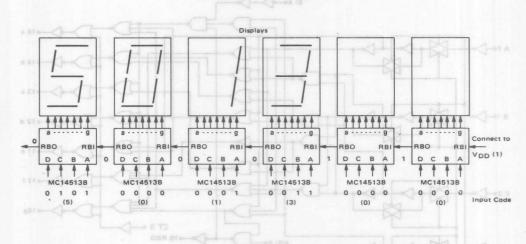
TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION

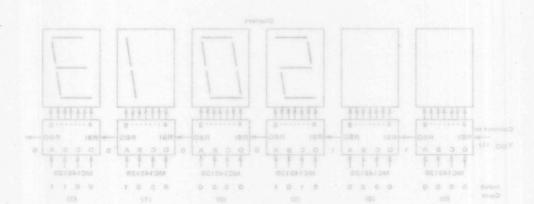


TYPICAL APPLICATIONS FOR RIPPLE BLANKING (Cont),

TRAILING EDGE ZERO SUPPRESSION



TYPICAL APPLICATIONS FOR RIPPLE BLANKING





1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

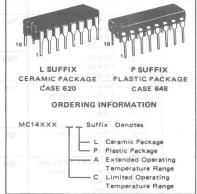
This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the output will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

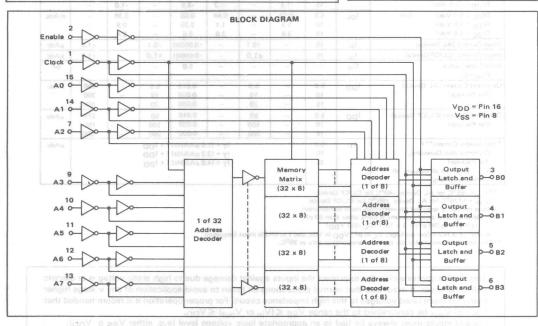
- Diode Protection on All Inputs
- Noise Immunity = 45% of Vpp typical
- Quiescent Current 10 nA/package typical @ 5 Vdc
- Single Supply Operation Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT (256 x 4) READ ONLY MEMORY





MAXIMUM RATINGS (Voltages referenced to Voc.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range · AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	оС

PIN ASSIGNMENT V_{DD} 16 A0 15 2 - En 3 - BO A1 14 4 C B1 A7 13 5 □ 82 6 □ 63 7 □ A2 A6 12 A5 11 A4 10 A3 9

717 1075		VDD	Tic	w °		25°C	lipsos d	notzac ^T h	igh *	rizive
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "O" Level	VOL	5.0	W 150 C	0.01	AC AS	PAOCA	0.01	A 54 ss	0.05	Vde
READ ONLY MEMORY	0	10	100	0.01		0	0.01	etal5 au	0.05	
		15	M. Bushe	0.01	1, 92, 1	0	0.01	830D HL	0.05	100
"1" Level	VOH	5.0	4.99	igini sou	4.99	5.0	JANOIS I	4.95	no Reserve	Vdd
. 2010	· OH	10	9.99	ry Enab	9.99	10		9.95	to sitt 1	100
		15	14.99	svol and	14.99	15	r, forci	14.95	fonyas s	of me
Noise Immunity #	VNL	V	rever les	idw noi	noilean	ice finds	rins de	zerfote	Tuqino	Vdd
(Vout 0.8 Vdc)	-WL	5.0	1.5	no- n	1.5	2.25	nun u mi	1.4	doi:4 1	180
(.V _{out} = 1.0 Vdc)		10	3.0	11000	3.0	4.50	- Contractor	2.9	110011	
(Vout 1.5 Vdc)	for	15	3.75		3.75	6.75	I Ingula	3.75	Protenti	aboi(
(V _{out} ≤ 0.8 Vdc)	Marie	5.0	1,4		1.5	2.25	of Vo	1.5	ticuate	Vdd
/ W . 10 Vdel	VNH	10	2.9		3.0	4.50		3.0		
(Vout 1.0 Vdc)		15	3.65	aby (3.75	6.75	eq\An I	3.75	mu\$7.me	desin?
(Vout 1.5 Vdc)	80.	15	3.00	2345300	3.75	0.75	H - H	3.75	vloore	Name of the last
Output Drive Current (AL Device)	ІОН		1.0		10			-0.7		mAd
(VOH = 2.5 Vdc) Source		5.0	-1.2		1.0	-1.7	nee-xa		sours y	POLIDON
(V _{OH} = 4.6 Vdc)	1 1	5.0	-0.25	- 1	-0.2	-0.36	les Usal	-0.14	sripta.l	regret.
(V _{OH} = 9.5 Vdc)		10	-0.62		-0.5	-0.9	vás:	-0.35	Voltage	Igau
(V _{OH} = 13.5 Vdc)		15	-1.8	-	-1.5	-3.5		-1.1		-
(VOL = 0.4 Vdc) Sink	OL	5.0	0.64	J 990 J	0.51	0.88	-well o	0.36	13G 10 8	mAd
(V _{OL} = 0.5 Vdc)		10	1.6	eteR sr	1.3	2.25	O#I	0.9	JIF YA	digital
(V _{OL} = 1.5 Vdc)		15	4.2		3.4	8.8	-	2.4	8506	antin
Output Drive Current (CL/CP Device)	ІОН									mAd
(VOH = 2.5 Vdc) Source		5.0	-1.0	-	-0.8	-1.7		-0.6	-	
(VOH = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36	-	-0.12	-	
(V _{OH} = 9.5 Vdc)		10	-0.5	-	-0.4	-0.9	-	-0.3	-	
(V _{OH} = 13.5 Vdc)		15	-1.4	-	-1.2	-3.5	-	-1.0	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	на Язо	0.44	0.88	-	0.36	-	mAd
(VOL = 0.5 Vdc)		10	1.3	III AUG	1.1	2.25	_	0.9	-	
(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	_	2.4		No. of Street,
Input Current (AL Device)	lin	15	-	+0.1	_	+0.00001	:0.1	2	±1.0	μAd
Input Current (CL/CP Device)	lin	15	_	±1.0	-	+0.00001	±1.0	-1	±1.0	μAde
Input Capacitance	Cin		7	-		5.0		75.77		pF
(V _{in} = 0)	oin					5.0				1
Quiescent Current (AL Device)	IDD	5.0	_	5.0		0.010	5.0	-o<	150	μAd
(Per Package)	L DD	10		10		0.020	10		300	мас
(i ci i dekage)		15		20		0.030	20	-1	600	41
011-011-011-011-011-011-011-011-011-011	1							-		-
Quiescent Current (CL/CP Device)	IDD	5.0	-	50		0.010	50	-	375	μAd
(Per Package)		10	-	100	-	0.020	100	~	750	100
		15	-	200	-	0.030	200	-	1500	-
Total Supply Current**1	I T	5.0				.6 μA/kHz)				μAd
(Dynamic plus Quiescent,		10				.2 µA/kHz)				
Per Package)	ha	15			IT = (4	.8 μA/kHz)	+ DD			1
(CL = 50 pF on all outputs, all	-		filemery	1 1						1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

^{*} T_{low} = -55°C for AL Device, -40°C for CL/CP Device. T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

†To calculate total supply current at loads other than 50 pF: $|T_{l}(C_{l})|^{2} = |T_{l}(S_{l})|^{2} + 1 \times 10^{-3} (C_{L} -50) V_{DD} f$ where: $|T_{l}|^{2} = |T_{l}(S_{l})|^{2} = |T$

SWITCHING CHARACTERISTICS*	(CL = 50 pF, TA = 25°C)

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH					ns
tTLH, tTHL = (3.0 ns/pF) CL + 30 ns	0	5.0	A -	180	360	o open-
tTLH tTHL = (1.5 ns/pF) CL + 15 ns	restablish 1886 to	10	S0% HAddre	90	180	
tTLH, tTHL = (1.1 ns/pF) CL+ 10 ns	PRES 207000	15		65	130	
Output Fall Time	tTHL	201	-tel les-20			ns
tTLH, tTHL = (1.5 ns/pF) CL + 25 ns		5.0	4 3576	100	200	
tTLH tTHL = (0.75 ns/pF) CL + 12.5 ns	1 2	10		50	100	
tTLH, tTHL = (0.55 ns/pF) CL + 9.5 ns	10.107	15	30130	40	80	
Clock Read Access Delay Time	taccc	n 7/41				ns
taccc = (1.7 ns/pF) CL + 1265 ns	-	5.0		1350	4000	
taccc = (0.66 ns/pF) C1 + 517 ns	A seds	10	-	550	1600	
taccC = (0.5 ns/pF) CL + 325 ns	- 208 - 208	15	-	350	1200	
Enable Access Delay Time	taccen	-0-3	00.0°pr			ns
t _{accEn} = (1.7 ns/pF) C _L + 160 ns	accEu	5.0	_	245	615	
tecc= = (0.66 ns/pF) C ₁ + 77 ns	1. 1560	10	1,200	110	265	
taccen = (0.5 ns/pF) CL + 50 ns	101gV	A 15	1 201 Par	75	190	
Clock Pulse Widtht	twH	5.0	450	150	_	ns
always go to the logic "1" state bet in the date is valid	stricting stell,	10	165	55	_	
seing successive "0's"		15	125	35	_	
et to "C" by Enable.	tWL	5.0	3600	1200	undan na d francisco	ns
	-442	10	1425	475	Assument	22 20 10 10
		15	1070	300	service 4	
Maximum Low Clock Pulse Width#	twL	5.0	2.0	10	ugal _	ms
THE STATISTICS AND ASSESSMENT OF THE PROPERTY	-44 F	10	0.9	3.0	_	1113
		15	0.1	0.3	_	
Address Setup-Time	t _{su(A)}	5.0	0	0	_	ns
7	-su(A)	10	1007	0	(0)(0)(D)	113
		15	0	0	MG (1)	
Address Hold Time	th(A)	5.0	0	0	_	ns
	(30)	10	0	0	_	113
VIII.		15	0	0	dan 3-	
Clock to Enable Setup Time	t _{su(cl)}	5.0	4275	1425	ngol_	ns
UBose,	30(01)	10	1725	575		110
"!" steps A	S	15	1295	400	_	
Clock to Enable Hold Time	\$1.7.0	5.0	11	0	DeG	
biley To and	th(cl)	10	75	bifue 0 874	PATO D	ns
		10	10	U	_	I

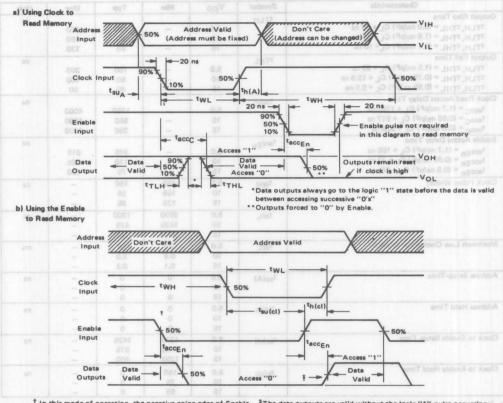
- * The formulae given are for typical characteristics only. ** Identity added to spee gridg as troops and including to a some
- † The clock can remain high indefinitely with the date remaining latched.

Sink current, address ROM to obtain a "0" on all four outputs (80 thru B3).

If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 - OUTPUT DRIVE CURRENT FIGURE 2 - SWITCHING TIME TEST CIRCUIT TEST CIRCUIT (Refer to timing diagram) Q VDD 9 VDD 16 -0-E B0 -O-E 80 0- A0 0- A0 <u></u> A1 81 0- A1 B1 -0 Pulse 0-A2 0- A2 0- A3 Pulse 0-A3 Generator B2 -0 A4 A4 0-0-A5 0- A5 B3 -0 ◆ Clock at 100 kHz 0-A6 Pulse 0- A6 10 Pulse Width = 300 ns A7 Generator 0- A7 VSS Scope Notes: Note: 1. Source current, address ROM to obtain a "1" Address ROM to obtain level change when on all four outputs (80 thru 83). clocking any one address line.

MEMORY READ CYCLE TIMING DIAGRAMS



† In this mode of operation, the negative going edge of Enable hould occur on or before the clock negative edge. †The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the austomer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}). Logic "1" is defined as a "high" Address input (V_{IH}).

WORD	-	RESS	A7	A6	A5	A4	А3	A2	A1	AO
Word	0	-	0	0	0	0	0	0	0	0
Word	1	SSITE.	0	0	0	0	0	0	0	1
Word	2	076190794	0	0	0	0	0	0	1	0
Word	3		0	0	0	0	0	0	1	1
						. /		-	200V (
									. 1	
Word	255	16/710/9	1	1	1	1	1	1	1.1	1

TRUTH TABLE

CLOCK	ENABLE	В0	B1	B2	B3
v _{DD} ¬ v _{SS}	1	(Address)	(Address)	< Address>	<address></address>
VSS VDD	1		OUTPUT		26264.3.2589
×	0	0	a rono or si	0	0000

X = Don't Care

Two methods may be used to transmit the custom memory pattern to Motorola.

METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

	DECIMAL CON- VERSION TABLE										
	OF SIF	D		CARD CHARACTER							
0 0 0	0000	0 0 1	0 1 0 1	0 1 2 3							
0 0 0	1	0 0 1 1	0 1 0 1	4 5 6 7							
1 1 1 1	0000	0 0 1 1	0 1 0 1	8 9 A B							
1 1 1	1	0 1 1	0 1 0 1	C D E F							

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

	318	ADDRESS INPUTS									SAMPLE WORD OUTPUTS			
WORD NUMBER	A7	A6	A5	A4	A3	A2	A1	AO	В3	B2	B1	В0	CARD	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	1	0	0	1	1	3	
2	0	0	0	0	0	0	1	0	0	0	1	1	3	
3	0	0	0	0	0	0	1	1 1	0	0	0	0	0	
	-22				11.		. [El.				15	
	55.				112		. 1		51.					
	22				517		. 1		011				7 .	
255	ec1	1	1 1	1	1	1	1	1	. 1	0	1	0	A	

Shown in columns 12 - 15 on card below

WORD NUMBER

Card No. -

^{*}Indicates contents of specified Address will appear at outputs as stated above.

11音

BRIARY

V= 38V

METHOD B: TRUTH TABLE

TRUTH TABLE

For customers who do not have access to punch cards, Motorola will accept Truth Tables. When filling out the table, use the 0 to F hexidecimal character in column "C".

CUSTOM PROGRAM for the MCM14524 Read Only Memory

	WORD (WORD	C		WORD	C	1	WORD	C
0	51		102		DOMAS DO	153			204	
0	52		103		CORAD RET	154		W-157 1 - PS 535	205	
0	53		104			155			206	
T	54		105		ndino parmet	156	-	decimel equit	207	1
	55		106		est ets chiso	157		hidulania a	208	sec.
	56	1	107		d order. 64 using the Bin	158	.,	mar mineral in	209	1
	57		108		and 78 are	159	100	steler organis	210	
	58		109	200	riggt order.	160		um daider au	211	and a
	59		110		eduamos pin	161	100	en in the telst	212	253
	60	-	111			162			213	
	61	TAN MININ	112	-	ini naoni	163	-	ROM SAI	214	\Box
	62	CHED CAR	113		MMARDORS	164		ING INUN	215	\vdash
	63	MPLE WOFE	114	1	100	165			216	\vdash
	64	OUTPUTS	115		SAL	166		10	217	\vdash
	65		116	-		167			218	-
	66	82 81	117		IA SA	168		AS AS	219	
	67	0 0	118	-	0 0	169		0 0	220	-0
	68	1 0	119	-	0 0	170	+	0 0	221	-
		1 0		+	1 0	100	\vdash	0 0	-	- 5
	69	0 0	120	-	1 0	171	-	0 0	222	- 8
	70	3 1 2	121	-		172	-		223	-
	71		122	1		173		10 10 1	224	-
	72	1 0	123			174			225	-
200	73		124		1	175			226	-
	74		125			176			227	
	75		126			177			228	
	76	1	127	RO	N .	178			229	
	77		128		Salar Salar	179			230	
	78	1111111	129	12	177777	180	2	0000000000	231	
	79		130	10	XXXXXX	181	18		232	
	80		131			182			233	
	81	113333333	132	1	00000000	183	11	annancer	234	
	82	1	133			184	-		235	
	83	1	134	1		185			236	
	84	-	135			186			237	\vdash
	85	-	136			187			238	\vdash
	86	100000000	137	100	288882581	188	-	应报答图图 5 0 1	239	0.0
	87	1 日本日本日本日	100	-	THE REPORT OF	189	25.6	GROBERDI	240	-
	88		139	-	11111111	190	1.1	13111111	240	11
22222						-				
	89	22222222		13	12222222	191	23	12222222	242	3.3
	90		141	-		192	-	cerce#8	243	
	91		142			193	-		244	0.0
11111	92		143	1	45555555	194	4.1	ED 1 2 2 2 2 2 3 1	245	4.5
	93		144			195			246	
	94	15555555		18	100555555	196	131	68888888	247	128
	95		146			197			248	
	96	10599933	147	10	100000000	198	4	2653333	249	2.5
	97		148			199			250	
	98	CLEASE S.	149	1	CHILLIAN.	200	1	4.52.5.5.5.1	251	4.0
	99		150	0		201	4.1		252	
	100	1000000	151		0000000	202			253	
E2800	101	00000000		0		203	8.0	enennen	254	0.0
	RNEGREGA	PRESENT		111	E B B B B B B B B	SHARE	15.0	001000001	255	



MCM14537

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14537 is a static random access memory (RAM) organized in a 256 x 1-bit pattern and constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of eight address inputs (A_n) , one data input (D_{in}) , one write enable input (\overline{WE}) , one strobe input (\overline{ST}) , two chip enable inputs $(\overline{CE_n})$, and one data output (D_{out}) .

Using both chip enable inputs as extensions of the address inputs. a 10-bit address scheme may be employed. Four MCM14537 devices may be used to comprise a 1024-bit memory without additional address decoding. The CE and ST inputs are dissimilary designed to enable usage of the memory in a variety of applications. An output latch is provided on the chip for storing the data read or written into memory, making a data-out storage register unnecessary. The CE inputs control the data output for third-state (high output impedance) or active operation which makes the memory very useful in a bus oriented system. When CE2 is high the chip is fully disabled. When CE1 is high the output is in the third state but data can be written into the output latch during a read cycle. This enables the use of the memory for fast reading by using the CE1 input to enable the latch. The memory is also designed so that dc signals can operate the memory with no maximum pulse width required on the CE and ST lines

Medium speed operation and micropower operation make the device useful in scratch pad and buffer applications where micropower or battery operation and high noise immunity are required.

- Quiescent Current = 0.5 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- 3-state Output Capability for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ VDD = 10 Vdc
- Fully Decoded and Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

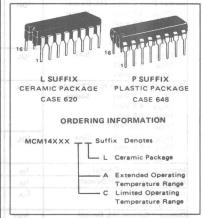
MAXIMUM RATINGS (Voltages referenced to VSS)

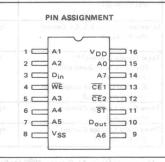
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdo
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (256 x 1) STATIC RANDOM ACCESS MEMORY





This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

ELECTRICAL CHARACTERISTICS

		VDD	T _{low} *		25°C			Thi	1	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05		0	0.05	-	0.05	Vdc
V _{in} - V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	DMEM	4.95	5.0	ARLOI	4.95	5128-61	Vdc
V _{in} = 0 or V _{DD}	0	10	9.95	-	9.95	10	_	9.95	_	
NFOWER CONFLEMENTARY MOS)	OUT	15	14.95	AR) -mon	14.95	1500	pizetz o	14.95	MONE or	1
Noise Immunity #	VNL		P-chann	SOM un	w bestsu	rango bna	metica	pid-l' w	In a 288	Vdd
(∴V _{out} ≤ 0.8 Vdc)	IAL	5.0	1.5	atenia .	1.5	2.25	10mm	1.4	M-chann	bins
(∠V _{out} ≤ 1.0 Vdc)		10	3.0	- Alman	3.0	4.50	edatti non	2.9	dT mud	Strue
(∧V _{out} ≤ 1.5 Vdc)		15	4.5	tonell ad	4.5	6.75	al places	4.4	- (- 1)	inni
(V _{out} ≤ 0.8 Vdc)	V _{NH}	5.0	1.4.	Henry	1.5	2.25	bes G	1.5	si al d ena	Vdc
(V _{out} ≤ 1.0 Vdc)	TINH	10	2.9	1200	3.0	4.50	110000000000000000000000000000000000000	3.0	DI SIGNITA	District Co.
(.\V _{out} ≤ 1.5 Vdc)		15	4.4	TODS SITU	4.5	6.75	ugni elds	4.5	mod flus	
Output Drive Current (AL Device)	ГОН		100000	100000	-		H Yam a			mAd
(VOH = 2.5 Vdc) Source	HO	5.0	-1.2	anounte	-1.0	-1.7	s sairq	-0.7	peen eq	520131
(V _{OH} = 4.6 Vdc)		5.0	-0.25	imilary o	-0.2	-0.36	CE and	-0.14	20000 131	adde
(VOH = 9.5 Vdc)	2000	10	-0.62	oatlons.	-0.5	-0.9	ii yaqanı	-0.35	opsqu si	disma
(V _{OH} = 13.5 Vdc)		15	-1.8	w to bas	-1.5	-3.5	e chip fe	-1.1	alveng ai	latel
(VOL = 0.4 Vdc) Sink	100	5.0	0.64	1835/30UT	0.51	0.88	100-038	0.36	OFF, OLD	mAd
(V _{OL} = 0.5 Vdc)	IOL	10	1.6	doh ou s	1.3	2.25	eqtuo e	0.36	signop at	mAd
(V _{OL} = 1.5 Vdc)		15	4.2	VIEW VI	3.4	8.8	oinw no	2.4	itos so i	eone.
		15	4.2	mut er o	3.4	0.0	C PRITTY	2.4	1997 (Feb. 170	2000.
Output Drive Current (CL/CP Device)	ПОН			b fud st		note at all	tugtue i	ets desire	a TSS	mAd
(V _{OH} = 2.5 Vdc) Source		5.0	-1.0	e sirLi e	-0.8	-1.7	dotal ru	-0.6	otni ne	nine
(V _{OH} = 4.6 Vdc)		5.0	-0.2	uari F3	-0.16	-0.36	pen amit	-0.12		SEU
(V _{OH} = 9.5 Vdc)		10	-0.5	o stenois	-0.4	-0.9 -3.5	Costa si s	-0.3	im self fr	note:
(V _{OH} = 13.5 Vdc)		15	-1.4	-				-1.0	WALL STREET	
(VOL = 0.4 Vdc) Sink	OL	5.0	0.52	LIG-DRAM	0.44	0.88	BUNENER	0.36	Auctual	mAd
(V _{OL} = 0.5 Vdc)		10	1.3	-	1.1	2.25	-	0.9	-890	116
(V _{OL} = 1.5 Vdc)		15 9	3.6	noisme	3.0	8.8	neits:	2.4	s melbs	11
Input Current (AL Device)	lin	15	TO MICE	± 0.1	sallegs	±0.00001	±0.1	in wra	±1.0	μAdc
Input Current (CL/CP Device)	lin	15	Ini uper	±1.0	Artil Fest	±0.00001	±1.0	edo-Ama	±14	μAdc
Input Capacitance (Vin = 0)	Cin	-	-	15 ¥dc	k lesiqy	5.0	7.5	Dunent	snozeju	pF
Quiescent Current (AL Device)	IDD	5.0	-	100	-	0.5	100	- wine	1800	μAdc
(Per Package)	טטי	10	_	200	Excussions.	1.0	200	ns(2-tuer	3600	Arioc
WWW. MALAS COMA TOTAL		15		400		1.5	400		7200	
Quiescent Current (CL/CP Device)	lee	5.0	-	100	101012.1	0.5	100	clore J.s.	1800	
(Per Package)	IDD	10		200	5V01	1.0	200	ie = 700	3600	μAdd
(Fer Fackage)		15	-	400		1.5	400		7200	
A STATE OF THE STA	-		-	400			Day 100 Control	D097080	7200	-
Total Supply Current**†	IT	5.0			T 5 (1	.46 µA/kHz) f + IDD			μAdd
(Dynamic plus Quiescent, Per Package)			Laurence Comme			.91 μA/kHz				0 0
(CL = 50 pF on all outputs, all		15	$I_T = (4.37 \mu A/kHz) f + I_{DD}$							
buffers switching)		15	-	1	1	T 0 0005	-	-	อกล์ คิ. ลาน	15
Three-State Leakage Current (AL Device)	ITL	15		± 0.1		+0.00001	± 0.1		±3.0	μAdo
Three-State Leakage Current (CL/CP Device)	ITL	15	-	±1.0	-	+0.00001	±1.0	-	±7.5	μAdo

^{*}T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either

^{2.0} Vdc min @ VDD = 10 Vdc and 2.5 Vdc min @ VDD = 15 Vdc

^{2.5} Vdc min @ VDD = 15 Vdc

1To calculate total supply current at loads other than 50 pF: $1_T(C_L) = 1_T(50 \text{ pF}) + 1 \times 10^{-3} (C_L - 50) \text{ VDD}$ where: $1_T \text{ is in } \mu\text{A} \text{ (per package)}, C_L \text{ in pF, VDD in Vdc, and f in kHz is input frequency.}$ **The formulas given are for the typical characteristics only at 25°C.

Characteristic		Figure_	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time		3	tTLH					ns
tTLH = (3.0 ns/pF) CL + 30 ns			1 -11	5.0	D	180	360	
tTLH = (1.5 ns/pF) CL + 15 ns				10	-	90	180	
t _{TLH} = (1.1 ns/pF) C _L + 10 ns				15	-0	65	130	1
Output Fall Time		3		10	0	- 00	130	-
		3	tTHL		-0			ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns				5.0	- 1	100	200	
tTHL = (0.75 ns/pF) CL + 12.5 ns				10	0-	50	100	
tTHL = (0.55 ns/pF) CL + 9.5 ns				15	0:	40	80	
Read Access Time from ST or CE2	00 V D-9	4,5	tacc(R)	88	-0			ns
t _{acc} = (1.4 ns/pr) C ₁ + 2480 ns			000(11)	5.0	400	2500	6000	100
t _{acc} = (0.7 ns/pF) C _L + 690 ns	(0)			10	150	700	2000	-
t _{acc} = (0.5 ns/pF) C _L + 393 ns	(0)			15	115	400	1500	
Output Enable Delay from CE1 or CE2		5,6	== .	5.0	70	300	900	_
output chable belay from CET of CE2	Surrend	5, 6	tacc(CEn)	10000				ns
	28,717,750,0			10	25	100	300	
				15	20	70	225	
Setup Time from An to ST or CE2	1 1	4, 5, 6, 7	t _{su(A)}	5.0	1800	600	-	ns
			22 V Q	10	600	200		
				15	450	140	-	
Hold Time from An to ST or CE2		4, 5, 6, 7	** (-)	5.0	600	200	_	
TOTAL TIME TOTAL AND TOTAL CEZ		4, 5, 6, 7	th(A)				_	ns
				10	240	80	_	
				15	180	55	-	
Data Hold Time	WHA LEGGE	7	th(D)	5.0	1400	480	-	ns
				10	500	160	_	
				15	375	110	-	
Data Setup Time		7	+ (0)	5.0	3600	1200		ns
and decap i iiii	1		t _{su(D)}	10	1800	600		1113
				100		420	_	
				15	1350	-		-
Write Enable Hold Time	7	th (WE)	5.0	150	50	-	ns	
Write Chable Hold Time	Pulse ()			10	60	20		10/18/
	1			15	45	15	-	
Write Enable Setup Time		7	t _{su} (WE)	5.0	720	240	_	ns
	Purise of		30(44)	10	240	80	_ =	
	- nonereneur			15	180	55	_	1
Write Enable to Dout Disable**				5.0	720	240	-	-
Witte Eliable to Dout Disable	· (pagG) sug	uO 4	tWE		240	4	-	ns
			0	10		80	-	
Special and a second			7110	1.5	180	55		-
Strobe or CE2 Pulse Width When Reading		4, 5, 6	tWL(R)	5.0	1350	450	5.1-	ns
				10	450	150	-	10,18
	1			15	340	100	-	-
Strobe, CE1 or CE2 Pulse Width When Writing		7	tWL(W)	5.0	2400	1200		ns
,		-	-44 F (44)	10	1260	600	_	
				15	945	420	_	
			-	10	343	420		-
Write Recovery Time		4	tR(W)	100				ns
t _W = (1.4 ns/pF) C _L + 219 ns				5.0	70	240	720	
$t_W = (0.7 \text{ ns/pF}) C_L + 70 \text{ ns}$				10	25	80	240	
$t_W = (0.5 \text{ ns/pF}) C_L + 47.5 \text{ ns}$	1			15	20	55	180	
CE1 or CE2 to Dout Disable Delay**		6	tCE _n	5.0	70	300	900	ns
Val.	THUSING	AC TEST O	FIGURE 3	10	25	100	300	
				15	20	70	225	
Read Setup Time	Y	A E		5.0	0	-100	-	-
tood detap time	0A	4,5	t _{su(R)}		1		-	ns
	1.6			10	0	-40	-	
				15	0	-30	_	-
Read Hold Time	2.4	4,5	th(R)	5.0	540	180	-	ns
	EA			10	240	60	-	
	0.0			15	180	45	_	
Read Cycle Time		4,5		5.0	-	2500	6000	
	GAL	4,5	tcyc(R)					ns
	9.0			10	-	700	2100	
	0.2			15	-	500	1575	-
Nrite Cycle Time	18	7	tcyc(W)	5.0	9 -	1400	4800	ns
				10	_	700	2100	
	399		-	15	-	500	1575	

^{*} The formulae given are for the typical characteristics only. ** 10% output change into a 1.0 k Ω load.

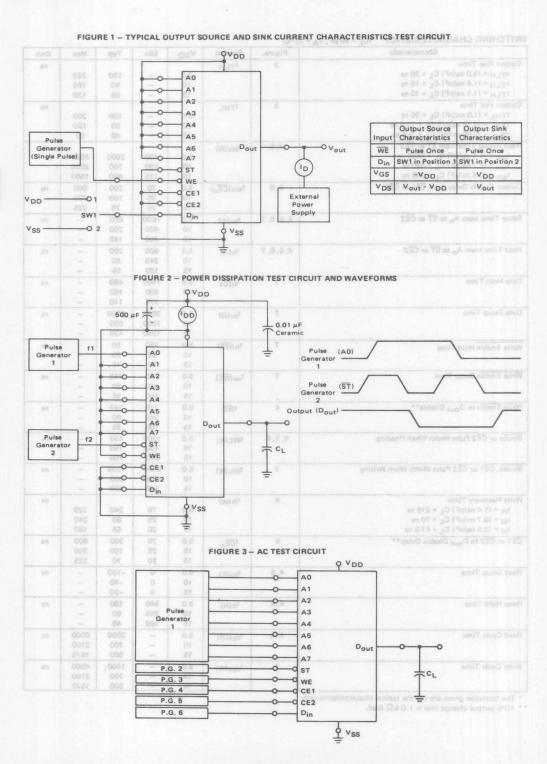
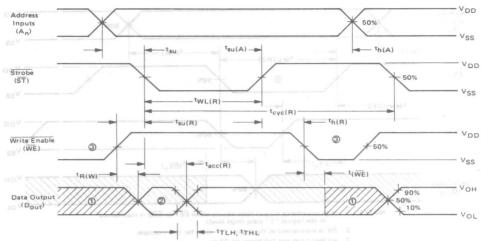
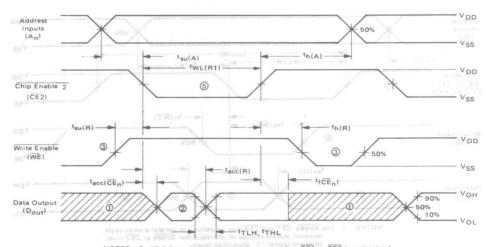


FIGURE 4 - READ CYCLE WAVEFORMS UTILIZING STROBE-TO-ACCESS MEMORY



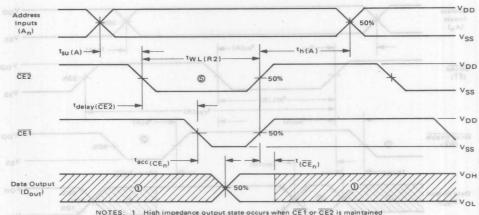
- NOTES: 1 High impedance output state occurs when WE is maintained as a logical
 - 2 The output momentarily displays data from the previous state.
 - 3 For read operation, WE may be maintained at a logical "1" (high level) during the complete cycle.
 - 4 CE1 and CE2 are maintained at a logical "O" state (low level).
 - 5 All input rise and fall times are 20 ns.

FIGURE 5 - READ CYCLE WAVEFORMS UTILIZING CE2 FOR ACCESS MEMORY



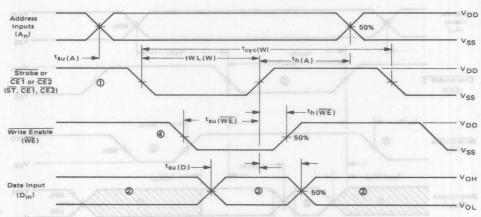
- NOTES: 1 High Impedance output state occurs when $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ is maintained in the logical "1" state (high level).
 - 2 The output momentarily displays data from the previous state.
 - 3 For read operation, WE may be maintained at a logical "1" (high level) during the complete cycle.
 - 4 All input rise and fall times are 20 ns.
 - 5 $t_{WL(R1)} \ge t_{acc}(R) max$

FIGURE 6 - READ CYCLE WAVEFORMS UTILIZING CE1 AND CE2 TO ACCESS MEMORY

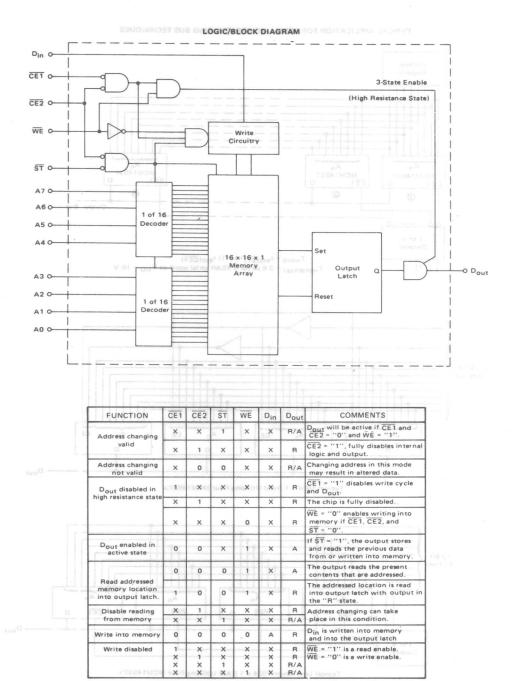


- NOTES: 1 High impedance output state occurs when $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ is maintained in the logical "1" state (high level).
 - 2 WE is maintained at the logical "1" state for this example.
 - 3 All input rise and fall times are 20 ns
 - 4 t_{delay(CE2)} minimum assuares that only data presently addressed will appear at the output.
 - tdelay(CE2) min. = taccR max. tacc(CE1) min.
 - 5 tWL(R2) ≥ t_{delay} (CE2) min + t_{acc} (CE_n) max

YROMAN 22355A FIGURE 7 - WRITE CYCLE WAVEFORMS DASH - 2 345514



- NOTES: 1 The Strobe, CE1 and CE2 may be utilized to control a write cycle, however, during changes of address either Strobe or CE2 must be in the logical "1" state (high level).
 - 2 Data input logic level is don't care during the indicated intervals.
 - 3 Data input logic level must remain fixed.
- 4 Write Enable may be maintained as a logical "0" during the write cycle.
 - 5 All input rise and fall times are 20 ns.



R = High resistance state at Dout

A = An active level of either VSS or VDD

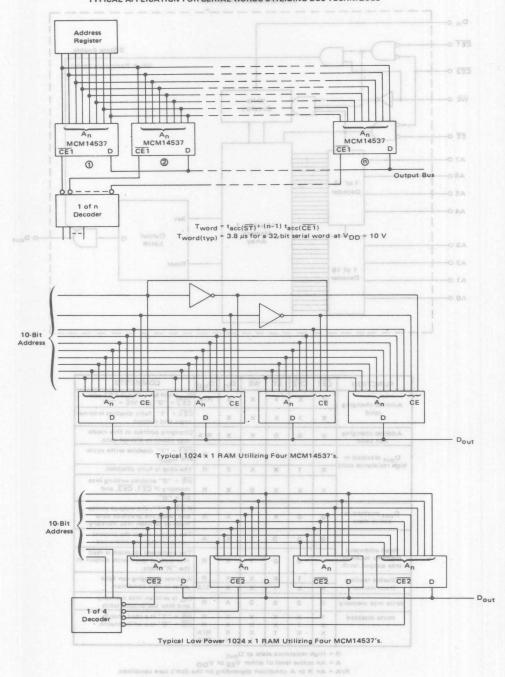
R/A = An R or A condition depending on the don't care condition

X = Don't care condition (must be in the "1" or "0" state)

1 = A high level at V_{DD}

0 = A low level at VSS

TYPICAL APPLICATION FOR SERIAL WORDS UTILIZING BUS TECHNIQUES





MC14543B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (B1), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display, the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Current = 5.0nA/package typical @ 5 Vdc
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to VSS).

MAXIMUM RATINGS (Voltages referenced to VSS)

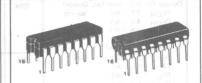
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C GG
Storage Temperature Rance	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	IOHmax IOLmax	10 Boemah Jamispa a	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	POHmax POLmax	ons be 05ken to a	mW
*POHmax = IOH (VOH - VDD) and POLmax =	IOL (VOL-	Vss)	

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

> for LIQUID CRYSTALS



L SUFFIX CERAMIC PACKAGE

P SUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating

TRUTH TABLE

10.61		INPUT	S							-	OU.	TPL	JTS	
LD	ВІ	Ph*	D	С	В	Α	а	b	с	d	е	f	9	Display
X	1	0	x	×	x	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
4	0	0	1	0	0	0	1	1	1	1	1	1	1	8
Mod	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
edia.	0	0	1.	1.	1	0	0	0	0	0	0	0	0	Blank
. 1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X		7		**				* *
74010	da i	ai q yr.	gdj	10	† I	10.	Co		se coina			out	ad	Display as abov

K = Don't care
= Above Combinations

* = For liquid crystal readouts, apply a square wave to Ph For common cathode LED readouts, select Ph = O.

For common anode LED readouts, select Ph = 1.

* = Depends upon the BCD code previously applied when LD = 1



ELECTRICAL CHARACTERISTICS

		VDD	Tlo	w		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0,05	-	0.05	Vdc
$V_{in} = V_{DD}$ or 0.		10	-	0.05	-	0	0.05	-	0.05	
1000		15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
V _{in} = 0 or V _{DD}		10	9.95	ARBOO	9.95	10	DIMETRI	9.95	V32-0T	COS
WPOWER COMPLEMENTARY MOST	07)	15	14.95	-	14.95	15	muru i	14.95	-	
nput Voltage# "0" Level	VIL									Vdc
(VO = 4.5 or 0.5 Vdc)		5.0	-	1.5	-	2.25	1.5	-	1.5	
(VO = 9.0 or 1.0 Vdc)	3	10	-	3.0	-	4.50	3.0	-	3.0	
(V _O = 13.5 or 1.5 Vdc)	- 1	15	nov i nb\t	4.0	lozal- 10	6.75	4.0	843B B	4.0	T.
"1" Level	VIH		flw betar	s constn	bus an	obset less	yno biug	I rithly so	u sot ber	sireb
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	soiesb s	3.5	2.75	CMIGS	3.5	lementur	Vdc
(VO = 1.0 or 9.0 Vdc)	du teel !	10	7.0	2 method	7.0	5.50	s itt end	7.0	r entrivers	raigs
(V _O = 1.5 or 13.5 Vdc)		15	11.0	make worth	11.0	8.25	South and	11.0		
Output Drive Current (AL Device)	ІОН		203	Land Land	Name I de		ed the	and also	f arti tra	mAdd
(VOH = 2.5 Vdc) Source	011	5.0	-3.0	1.86.1 .81	-2.4	-4.2	-	-1.7		110 100
(VOH = 4.6 Vdc)		5.0	-0.64	OJ_DSE	-0.51	-0.88	Hdezib r	-0.36	(18 <u>)</u> eni	blank
(VOH = 0.5 Vdc)	Steen I	10	(IQ)=1 ,81	102 438	4.0	-10.1	in 941 2	held_nes	rig skist	rituro
(V _{OH} = 9.5 Vdc)		10	-1.6 -4.2	SI SANA	-1.3 -3.4	-2.25 -8.8	(Out) in	-0.9 -2.4	spill mill.	tively
(V _{OH} = 13.5 Vdc) (V _{OI} = 0.4 Vdc) Sink	1	5.0	-	nomma	-	2010/2010	ing how	10 00193	busins el	oriz.
(V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc)	IOL	10	0.64	bezaam	0.51	0.88	to stug	0.36	yalozb s	mAde
(VOL = 9.5 Vdc)	1	10	1.0	bear to	1.3	10.1	coben 1	0.9	atriemps	the s
(VOL = 1.5 Vdc)		15	4.2	desile so	3.4	8.8	(#ED	2.4	ctime-trip	1 26
Output Drive Current (CL/CP Device)	ЮН		SE SIGIZ	no new	976 20	B KISID III	TOSTINU.	,87 8000	B1 3118010	mAdo
(VOH = 2.5 Vdc) Source	-OH	5.0	-2.5	_	-2.1	4.2	_	-1.7	_	MAG
(V _{OH} = 4.6 Vdc)	ARBD	5.0	-0.52	no 142/0	-0.44	0.88	nindani i	-0.36	noitezilar	A
(VOH = 0.5 Vdc)		10	aulita un	levil e tie	drawn wa	10.1	db =sta	-0.50	uon-s	drive
(VOH = 9.5 Vdc)		10	-1.3	-	-1.1	2.25	1 150 c	-0.9	No ottoine	e bins
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	8.8	n, a <u>n</u> d to	-2.4	NEST STREET IN	E KAYUS
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	-	0.36	-	mAdo
(VOL = 0.5 Vdc)	MCN	10	1.3	-	1.1	2.25	-	0.9	-	
(VOL = 9.5 Vdc)		10	3.6	aci m ise.	3.0	10.1	O HAROS	HUCH HE	gic _Circl	11 0
(V _{OL} = 1.5 Vdc)		15			3.0	8.8		2.4	-38/	d
nput Current (AL Device)	lin	15	-	± 0.1		± 0.00001	+0.1	nO To ep	11.0	μAdc
nput Current (CL/CP Device)	lin	15		± 0.3		±0.00001	± 0.3	State	± 1.0	μAdc
nput Capacitance (Vin 0)	Cin	-		znoit	nidmoC	5.0	7.5	nking or	adout Bl	pF
Quiescent Current (AL Device)	IDD	5.0	shttatja u	5.0	(añoum	0.005	5.0	BINGS) A	150	μAdc
(Per Package)	00	10	-	10	Vde	0.010	0.10	age Ran	300	18 .0
		15	WCO-WO	20	eo.l JT	0.015	20	priving	600	3 6
Quiescent Current (CL/CP Device)	IDD	5.0	Temos	20	smuE) als	0.005	20	becd J7	150	μAdc
(Per Package)		10	-	40	-	0.010	40	-	300	1
PA- D C B A B B C d 4 1 g 20	18 03	15		80		0.015	80	-	600	
otal Supply Current**†	IT.	5.0	100 V 40	W-11 1 11	I'T (1	.6 μA/kHz	200	10201001	100 7 700 1	μAde
(Dynamic plus Quiescent,	0 1	10				1.1 µA/kHz				MAIL
Per Package)	0 1	15				1.7 µA/kHz				
(C ₁ - 50 pF on all outputs, all	0 1				1 (3	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,				
buffers switching)	0 7									

*Tlow = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

=Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

tTo calculate total supply current at loads other than 50 pF

IT(CL) = IT(50 pF) + 3.5 x 10-3 (CL -50) VDDf

where: T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25° C.

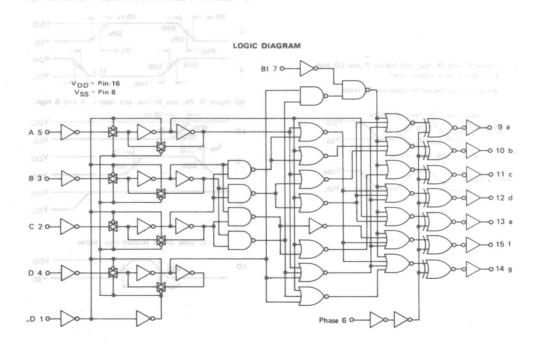
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

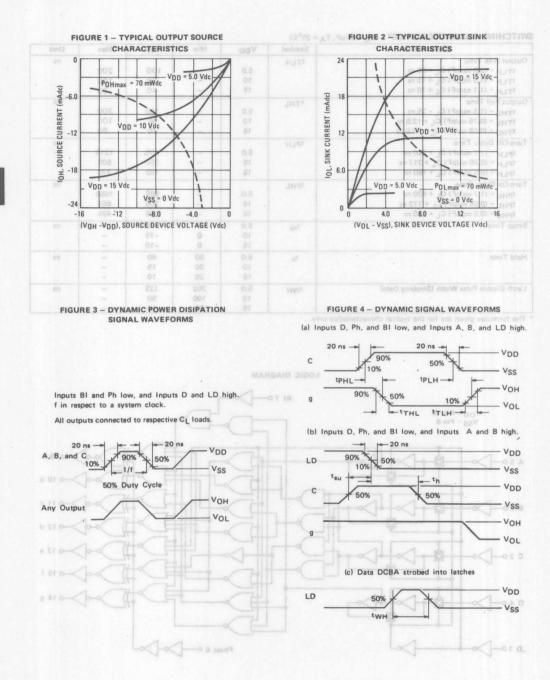
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either VSS or VDD).

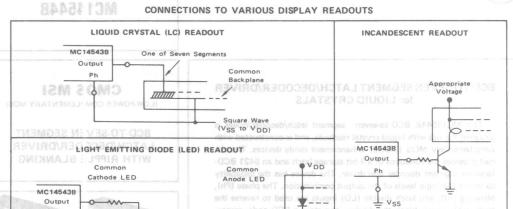
SWITCHING CHARACTERISTICS*	(CL = 50 pF, TA	= 25°C)
Characteristic	10	Symbo

Characteristic	Symbol	VDD	Min 800	Тур	Max	Unit
Output Rise Time tTLH = (3.0 ns/pF) CL + 30 ns tTLH = (1.5 ns/pF) CL + 15 ns tTLH = (1.1 ns/pF) CL + 10 ns	tTLH	5.0 10 15	30V II 7 00	100 50 40	200 100 80	ns
Output Fall Time tTHL = (1.5 ns/pF) CL + 25 ns tTHL = (0.75 ns/pF) CL + 12.5 ns tTHL = (0.55 ns/pF) CL + 12.5 ns	tTHL	5.0 10 15		100 50 40	200 100 80	ns
Turn-Off Delay Time tp_H = (1.7 ns/pF) C_L + 520 ns tp_H = (0.66 ns/pF) C_L + 217 ns tp_H = (0.5 ns/pF) C_L + 160 ns	tPLH .	5.0 10 15	=/	605 250 185	1210 500 370	ns
Turn-On Delay Time tpHL = (1.7 ns/pF) CL + 420 ns tpHL = (0.66 ns/pF) CL + 172 ns tpHL = (0.5 ns/pF) CL + 130 ns	tPHL	5.0 10 15	-0.5-	505 205 155	1650 660 495	ns
Setup Time 2001 302 1307 3317 30 3410 (827 - 107)	t _{su}	5.0 10 15	0 0	-40 -15 -10	 	ns
Hold Time	^t h	5.0 10 15	80 30 20	40 15 10		ns
Latch Disable Pulse Width (Strobing Data)	twH	5.0 10 15	250 100 80	125 50 40	- - -	ns

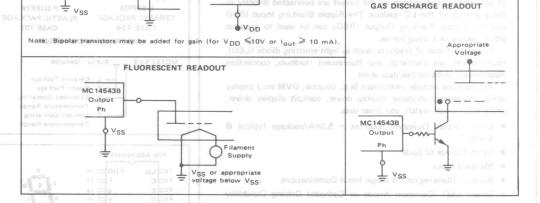
^{*} The formulae given are for the typical characteristics only.

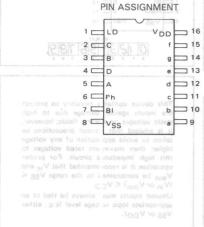






MC14543B Output





		Raung
	ggV	DISPLAY Spelled Vallege 200
	17/1	7 3 4 5 5 7 8 9 ~
	0 1	1 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1
	0 1 AT	2 3 4 5 6 7 8 9 eo/v9Q JA = egneB unutarectas (gracareQO eo/v9Q 90\JO
-65 to +150		Storage Temperature Range

CONNECTIONS TO SEGMENTS



MC14544B

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14544B BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. The Ripple Blanking Input (RBI) and the Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes.

For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

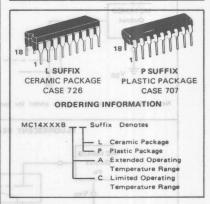
- Logic Circuit Quiescent Current = 5.0nA/package typical @ 5 Vdc
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capability for Suppression of Non-significant zero
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

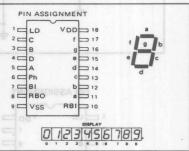
CMOS MSI

LIQUID CRYSTAL (LC) REACOUT

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING





MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage YAJIAIG	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		10	mAdd
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Rance	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current . (Source or Sink) per Output	IOHmax IOLmax	10	mAdo
Maximum Continuous Output Power* (Source or Sink) per Output	POHmax POLmax	70	mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} \leq (V_{in} or V_{out}) \leq V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

FLECTRICAL CHARACTERISTICS

	948	niN	VDD	Tic	w*		25°C		orac Thi	gh *	
Characteristic	c	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	2 _	0.05	-	0	0.05	BE +_0 /	0.05	Vdc
Vin = VDD or 0	8.0		10	-	0.05	-	0	0.05	11 + 40	0.05	FRIT
0.08	0.0	-	15	-	0.05	-	0	0.05	0.00	0.05	PHAT
	"1" Level	VOH	5.0	4.95	1947	4.95	5.0	_	4.95	with I	Vdc
Vin = 0 or VDD	001	011	10	9.95	_	9.95	10	- 10	9.95	le\r.±8.11	The Line of
0C f	80	-	15	14.95	_	14.95	15	2.5 ws	14.95	North Control	H Harris
Input Voltage#	"0" Level	VIL		1				2.5 ns	F) C ₁ =	Q 55 19/0	Vdc
(V _O = 4.5 or 0.5 Vdc)	0 2010.	-11	5.0	-	1.5	-	2.25	1.5	-	1.5	
(V _O = 9.0 or 1.0 Vdc)	308		10	- 50	3.0	_	4.50	3.0	sa resort	3.0	
(V _O = 13.5 or 1.5 Vdc)	280		15	-	4.0	-	6.75	4.0		4.0	1 11
(10.0 0) 1.50 (00)	"1" Level	VIH			4.0	_	0.70	en 0		10 1 2 0	10 10
(Vo = 0.5 or 4.5 Vdc)		*IH	5.0	3.5		3.5	2.75		3.5	19 1 6 9	Vdc
(VO = 1.0 or 9.0 Vdc)			10	7.0	714 <u>d</u> d1	7.0	5.50		7.0	ent7 ye	Vuc
(V _O = 1.5 or 13.5 Vdc)	909		15	11.0	_	11.0	8.25	187 U	11.0	tov-T-C	" JHS
Output Drive Current (AL	Davisa	1	13	111.0		11.0	8.25	44.50	11.0	-	mAd
(VOH = 2.5 Vdc)	Source	ІОН	5.0	-3.0	_	-2.4	-4.2	1877, 10	-1.7		mad
(VOH = 4.6 Vdc)	000100	0	5.0	-0.64	14	-0.51	-0.88	_	-0.36		mil o
(VOH = 0.5 Vdc)	-76	0	10	-	-	-	-10.1	_	-0.50		
(VOH = 9.5 Vdc)	914		10	-1.6	-	-1.3	-2.25	_	-0.9	_	1
(VOH = 13.5 Vdc)	0.6-	0.0	15	-4.2	-	-3.4	-8.8	_	-2.4	_	Last s
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.64	_	0.51	0.88	_	0.36	_	mAde
(VOL = 0.5 Vdc)	101	20	10	1.6	-	1.3	2.25	-	0.9	_	
(VOL = 9.5 Vdc)			10	-	-	-	10.1		- 1	_	
(VOL = 1.5 Vdc)	98.1	250	15	4.2	Hit	3.4	8.8	m (I—) od	2.4		soid a
Output Drive Current (CL/ (VOH = 2.5 Vdc)	(CP Device) Source	ІОН	5.0	-2.5		-2.1	4.2		-1.7		mAd
(VOH = 4.6 Vdc)	Source		5.0	-0.52	_						
(V _{OH} = 0.5 Vdc)	1		10	-0.52	_	-0.44	0.88	163HIVID	-0.36	-	1
(VOH = 9.5 Vdc)	- 1	- 1	10	-1.3	_	-1.1	2.25	_	-0.9	_	1
(VOH = 13.5 Vdc)		- 1	15	-3.6	_	-3.0	8.8	_	-2.4	_	1
(VOL = 0.4 Vdc)	Sink	lor	5.0	0.52	10 5100	0.44	0.88	_	0.36		mAd
(VOL = 0.5 Vdc)		·OL	10	1.3	Min 2400	1.1	2.25	_	0.9	1	IIIAu
(VOL = 9.5 Vdc)	1		10	er -	-	-	10.1	-	-	-	
(VOL = 1.5 Vdc)			15	3.6	18	3.0	8.8	-	2.4	_	
nput Current (AL Device)		lin	15	-	± 0.1	-	±0.00001	± 0.1	117 min s	± 1.0	μAdd
nput Current ICL/CP Device	ce)	1 _{in}	15	1	± 0.3		±0.00001	± 0.3	9209	± 1.0	μAdd
nput Capacitance (Vin = 0)		Cin			-	-	5.0	7.5	-	-	ρF
Quiescent Current (AL Devi	ice)	IDD	5.0	7.1-1	5.0	-	0.005	5.0	I	150	μAdo
(Per Package)		.00	10	12	10	-	0.010	10		300	-02
1.7	Hax I	9.	15		20	-	0.015	20	- 1	600	
Quiescent Current (CL/CP (Device)	IDD	5.0		20	-	0.005	20	4	150	μAdo
(Per Package)	7	.00	10	11	40		0.003	40	-	300	μΑσσ
1 81 0-0 0-0	Ta H	-	15	7-0	80	E	0.015	80	J. 1	600	
otal Supply Current**†		IT	5.0	11111	80	100		100		600	
(Dynamic plus Quiescen	4-0(=	T	10	F1 6			.6 μA/kHz				μAdd
Per Package)	1	11 1	15				3.1 μA/kHz				
(C ₁ = 50 pF on all outp	100 200		15	-5		T = (4	l.7 μA/kHz	סטי דיו			
buffers switching)	uts, all			1 1 1							1

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device. #Noise immunity specified for worst-case input combination.

[#]Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc

2.0 Vdc min @ VDD = 10 Vdc

2.5 Vdc min @ VDD = 15 Vdc

1 To calculate total supply current at loads other than 50 pF:

I_T(C_L) = I_T(50 pF) + 3.5 x 10-3 (C_L -50) VDDf

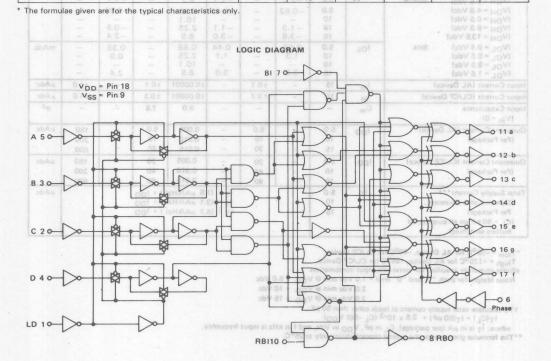
where: I_T is in \(\mu A \) (per package), C_L in pF, VDD in Vdc, and f in kHz is input frequency.

"The formulas given are for the typical characteristics only at 25°C.

SWITCHING	CHARACTERISTICS*	$(C_1 = 50 pF)$	$T_A = 25^{\circ}C$

100	Characteristic	2890		Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	n(N) x	Typ Mgs	Min	tTLH	nitif ab	Symbol V		Characterists	ns
tTLH = (3.0 ns/p	F) CL + 30 ns			1 0.05	5.0	Vot 1	100	200	Durgue Volt
tTLH = (1.5 ns/p	F) CL + 15 ns	0.0 0		80.0	10		50	100	Vin = Vr
tTLH = (1.1 ns/p	F) CL + 10 ns			0.05	_ 15	-	40	80	
Output Fall Time	4.95	6.0	4.95	THL	4.9	KOY	leveJ "f"	The state of the s	ns
tTHL = (1.5 ns/p	F) CL + 25 ns				5.0	-	100	200	Vin - 0 o
tTHL = (0.75 ns/	pF) CL + 12.5	ns		- 1	9 M 10	-	50	100	
tTHL = (0.55 ns/	pF) CL + 12.5	ns			15	-jjV	40	80	entioV teeni
Turn-Off Delay Time	e	2.26		tPLH	- 0.	8		IsbV 8.0 to	ns
tpLH = (1.7 ns/p	F) CL + 520 ns	4.50 J.G		0.0	5.0	-	605	1210	1.0 - DV)
tpLH = (0.66 ns/	pF) C1 + 217	ns at a		0.4	- 10	1 -	250	500	IVO = 13
tpLH = (0.5 ns/p					15	HIIV	185	370	
Turn-On Delay Time	3.0	27.70	3.3	tPHL	8.6 0.	e l		1904 6.9 10	ns
tpHL = (1.7 ns/p	F) C1 + 420 n	08.8		1	5.0	-	505	1650	0.1 = 0VI
tpHL = (0.66 ns/				- 1	10	4	205	660	11 - OV)
tpHL = (0.5 ns/p			1.0		15	1004	155	495	Output Drive
Setup Time	88.0-	- 88.0		t _{su}	5.0	0	-40	TobV &	ns
					_ 10 0	0	-15	tob V da	" NOV
	6.0-			- 1	1-15 0	0	-10	E Vole)	" MOVI
Hold Time	F-X	=		th	5.0	80	40	3,5 Vest	ns
sbAm -				- 1	10	30	15	(obV A	(VOL = 0
	8.0				15	20	10	(abV 8.	10A)
Latch Disable Pulse	Width (Strobin	g Data)	3.4	twH	5.0	250	125	.5 Vdet	ns
abAm		-			10	100	50	131 tomeo	Citizent Original
					15	80	40	There is	100000

^{*} The formulae given are for the typical characteristics only.



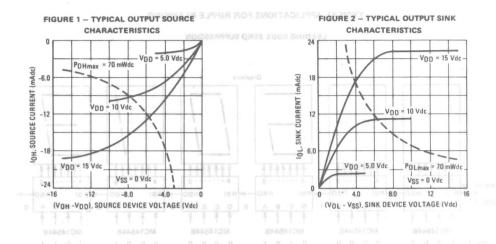
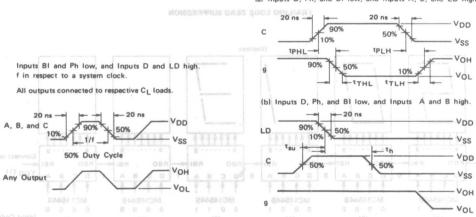


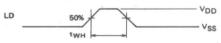
FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

FIGURE 4 - DYNAMIC SIGNAL WAVEFORMS

(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.

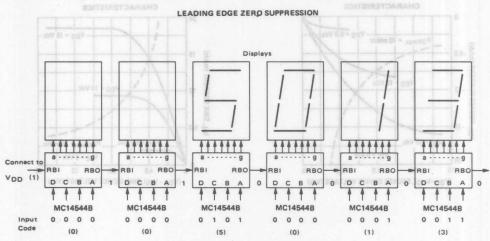


(c) Data DCBA strobed into latches

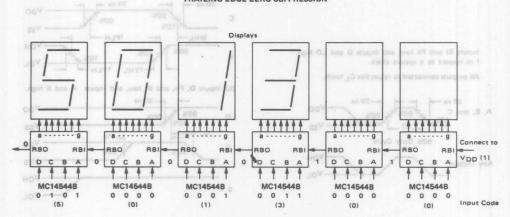






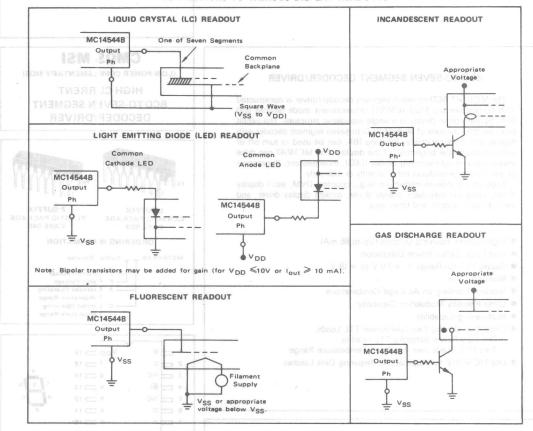


TRAILING EDGE ZERO SUPPRESSION



MC14547B

CONNECTIONS TO VARIOUS DISPLAY READOUTS



TRUTH TABLE

110	15	- 10	NPUTS		1			- 1				0	UTI	TUS	S	
RBI	LD	BI	Ph	D	C	В	A	RBO	a	b	c	d	e	f	9	DISPLAY
Х	X	1	0	X	X	X	X	#	0	0	0	0	0	0	0	Blank
1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	1	0	0	0	0	0	0	0	_1	1	1.	1	1	1	0	0
×	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0,0	1
X	1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	2
х	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	3
X	1	0	0	0	-1	0	0	0	0	1	-1	0	0	1	1	4
X	1.50	0	0	0	1	0	1	0	1	0	1	1	0	1	1	5
X	1.	0	0	0	1	1	0	0	1	0	1	1	1	1	1/1	6
X	1	0	0	0	1	1	1	0	1	1	1	0	0	0	0	7
X	10	0	0	01	0	0	0	0	- 1	1	1	1	1	1	1	8
X	1	0	0	- 1	0	0	1	0	. 1	1	1	1	0	1	1	9
X	1.	0	0	. 1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	10	0	0	-1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	10	0	0	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	1.	0	0	-1	1	0	1	0	0	0	0	0	0	0	0	Blank
х	1.	0	0	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	0	0	0	X	X	х	Х	#					.]		mi	bis big
Ŷ	1	Ť	1	i		0	0	0			nbini				Jon	Display as above

- X = Don't Care
- † = Above Combinations
- For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.
- ** = Depends upon the BCD Code previously applied when LD = 1.

MC14547B

MICTADA45

BDC-TO-SEVEN SEGMENT DECODER/DRIVER

CONNECTIONS TO VARIOUS DISPLAY READOUTS

The MC14547 BCD-to-seven segment decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of an 8421 BCD-to-seven segment decoder with high output drive capability. Blanking (BI), can be used to turn off or pulse modulate the brightness of the display. The MC14547 can drive seven-segment light-emitting diodes (LED), incandescent, fluorescent or gas discharge readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- High Current Sourcing Outputs (Up to 65 mA)
- Low Logic Circuit Power Dissipation
- Supply Voltage Range = +3.0 V to +18 V
- Blanking Input
- Readout Blanking on All Illegal Combinations
- Lamp Intensity Modulation Capability
- Multiplexing Capability
- Capable of Driving Two Low-Power TTL Loads,
 One Low-Power Schottky TTL Load or
 Two HTL Loads over the Rated Temperature Range
- Use MC14511B for Applications Requiring Data Latches

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	Vin	V _{DD} to -0.5	Vdc
Operating Temperature Range MC14547BAL MC14547BCL/CP	ure Range MC14547BAL TA		°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	IOHmax	65	mA
Maximum Continuous Power Dissipation	POHmax	1200*	mW

*See power derating curve (Figure 1).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

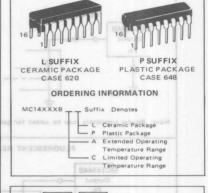
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

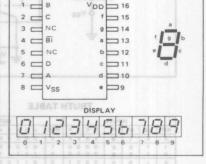
CMOS MSI

LIGUID CRYSTAL (LC) READOUT

(LOW-POWER COMPLEMENTARY MOS)

HIGH CURRENT BCDTO-SEVEN SEGMENT DECODER/DRIVER





TRUTH TABLE

1 10	INF	TU	S	0	1	0.	. 0		OU	TPI	JTS	×
BI	D	C	В	Α	a	b	c	d	е	f	9	DISPLAY
0	X	×	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	1	1	0	0	1	3
1	0	1	0	0	0	1	1	0	0	1	1	4
1	0	1	0	1	1	0	1	1	0	1	1	5
1	0	1	1	0	0	0	1	1	1	1	1	6
1	0	1	1	1	1	1	1	0	0	0	0	7
-1	1	0	0	0	1	1	1	1	1	1	1	8
1	1	0	0	1	1	1	1	0	0	1	1	9
1	1	0	1	0	0	0	0	0	0	0	0	Blank
1	1	0	1	1	0	0	0	0	0	0	0	Blank
1	1	1	0	0	0	0	0	0	0	0	0	Blank
1	1	1	0	1	0	0	0	0	0	0	0	Blank
1	1	1	1	0	0	0	0	0	0	0	0	Blank
1	1	1	1	1	0	0	0	0	0	0	0	Blank

X = Don't care

DS9807

ELECTRICAL	CHARACTERISTICS
------------	-----------------

half right Cha	aracteri	istic			Symbol	VDD	Tlo	w		25°C	orten a new	Thi		Unit
xsM Max	enlyf	gy.T		Max	Vete blin	Vdc	Min	Max	Min	Тур	Max	Min	Max	
Output Voltage	0411	9800.0∃e	"0"	Level	15	5.0	1 -	0.05	-	0	0.05	ve tt u	0.05	ig ina
$V_{in} = V_{DD} \text{ or } 0$					VOL	10	-	0.05	-	0	0.05	7.7	0.05	Vdc
34110					02.01	15	-	0.05		0	0.05		0.05	
			11111	Level		5.0	4.1		4.4	4.6	_	4.3		
$V_{in} = 0 \text{ or } V_{DD}$					VOH	10	9.1	_	9.4	9.6	DEMENDO.	9.3	1	Vdc
VID - O OL VDD					- VOH	15	14.1	_	14.4	14.6	-	14.4	4.4	, 400
- 000	- 20	510.0	11011	00	- 31	10	1.4		1-11	11.0				
nput Voltage #	20.		0	Level	- 0.8	- 0				2.25	O. E.		1.5	1500
$(V_0 = 3.8 \text{ or } 0.5 \text{ Vdc})$					- VIL 01	5.0	1	1.5	-	2.25	1.5	-	1.5	Vdc
$(V_0 = 8.8 \text{ or } 1.0 \text{ Vdc})$					20	10	1	3.0		4.50	3.0	-	3.0	0.550
$(V_0 = 13.8 \text{ or } 1.5 \text{ Vd})$	c)					15	-	4.0		6.75	4.0		4.0	
$(V_0 = 0.5 \text{ or } 3.8 \text{ Vdc})$)		"1"	Level	0.0	5.0	3.5	-	3.5	2.75	-	3.5	-	The state
$(V_O = 1.0 \text{ or } 8.8 \text{ Vdc})$)				VIH	10	7.0	-	7.0	5.50	-	7.0	-	Vdc
$(V_0 = 1.5 \text{ or } 13.8 \text{ Vd})$					61	15	11.0	-	11.0	8.25	_	11.0	_	
Output Drive Voltage (A		ce)			_									-
$(I_{OH} = 5.0 \text{ mAdc})$			Sou	ırce			4.0		4.2	4.3		4.3	1	100
// 10 11							7.0	n	4.1	4.3	_	-	-	
					Sec. 7	5.0	3.8	- ·	3.9	4.2	MANAG	4.0	(30)	Vdc
$(I_{OH} = 20 \text{ mAdc})$					1 1		3.0	8.74.1	3.7	4.0	we UTIA	4.0		do
							3.1	udmoa	3.2	3.7	rol ba	3.0	1008 (18)	a Action
$(I_{OH} = 65 \text{ mAdc})$							-	-	57 19	((N) D)	de Ti			dissin.
$(I_{OH} = 5.0 \text{ mAdc})$					1		9.1	-	9.2	9.3	Von	9.3	-	
$(I_{OH} = 10 \text{ mAdc})$					VOH		-	-	9.1	9.3	V 650	in To l	7	attorner
$(I_{OH} = 20 \text{ mAdc})$						10	8.8	-	9.0	9.2	V 50 B	9.2		Vdc
$(I_{OH} = 40 \text{ mAdc})$							-	-	8.9	9.0	-	-	-	
$(I_{OH} = 65 \text{ mAdc})$					1 1		8.4	-	8.5	8.8		8.1	-	
(IOH = 5.0 mAdc)	0 mAdc)						14.0	_	14.2	14.3	-	14.4	_	
$(I_{OH} = 10 \text{ mAdc})$					1 1		1 1.0	_	14.1	14.3	_		_	
$(I_{OH} = 20 \text{ mAdc})$					1 1		13.8	_	14.0	14.2	_	14.2	_	
					1	15	15.0		13.8	14.0		17.2		Vdc
$(I_{OH} = 40 \text{ mAdc})$					1 1	15	13.5	_	13.5	13.7		13.3		Vuc
(I _{OH} = 65 mAdc)					-		13.5		13.5	13.7	_	13.3		
Output Drive Voltage (C	L/CP L	Device)	_											
$(I_{OH} = 5.0 \text{ mAdc})$			Soi	ırce	1 1		3.9	10 E	4.1	4.3	BATO	4.2	5.41	OTES
$(I_{OH} = 10 \text{ mAdc})$					-	5.0			4.0	4.3		-	2	Vdc
$(I_{OH} = 20 \text{ mAdc})$							3.6	stic	3.8	0 4.2	-	3.9	-	
$(I_{OH} = 40 \text{ mAdc})$							-	-	3.5	4.0	_	-	_	
$(I_{OH} = 65 \text{ mAdc})$					1 1		3.0	_	3.0	3.7		2.9		
$(I_{OH} = 5.0 \text{ mAdc})$							8.9	-	9.1	9.3	-	9.2		fugruf
$(I_{OH} = 10 \text{ mAdc})$					VOH		_	-	9.0	9.3	-	-	-	
$(I_{OH} = 20 \text{ mAdc})$						10	8.6	-	8.8	9.2	-	9.0	-	Vdc
$(I_{OH} = 40 \text{ mAdc})$							-	-	8.5	9.0	=		_	Tu of un
$(I_{OH} = 65 \text{ mAdc})$					1 1		8.0		8.1	8.8	-	8.0	_	
$(I_{OH} = 5.0 \text{ mAdc})$							13.9	-	14.1	14.3	-	14.2	_	
$(I_{OH} = 10 \text{ mAdc})$							10.0		-14.0	14.3		17.2	_	
$(I_{OH} = 20 \text{ mAdc})$						15	13.6		13.8	14.3		14.0		Vdc
					1	10	13.0		13.5	14.2	577 T	14.0		Vuc
$(I_{OH} = 40 \text{ mAdc})$ $(I_{OH} = 65 \text{ mAdc})$							13.0	_	13.0	13.7		13.0	_	
		10	1149	2	+		13.0	-	13.0	13.7		13.0		
	L Devic		0:			F 0	0.00		0.00	0.44		0.10		
Output Drive Current (A			Sin	k	IOL	5.0	0.32		0.26	0.44		0.18		mAd
Output Drive Current (A (V _{OL} = 0.4 Vdc)					.OL	10	0.80	-	0.65	1.13	-	0.45	-	
Output Drive Current (A $(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$					1 1	15	2.10	-	1.7	4.4	roi Tar	1.2	a pT	O MISI
Output Drive Current (A (V _{OL} = 0.4 Vdc)	-	I dr												
Output Drive Current (A (VOL = 0.4 Vdc) (VOL = 0.5 Vdc) (VOL = 1.5 Vdc)	L/CP D	l dr		-										
Output Drive Current (A (VOL = 0.4 Vdc) (VOL = 0.5 Vdc) (VOL = 1.5 Vdc) Output Drive Current (C	L/CP D	l dr	Sin	k		5.0	0.26	_	0.22	0.44	_	0.18	_	
Output Drive Current (A (VOL = 0.4 Vdc) (VOL = 0.5 Vdc)	L/CP D	l dr	Sin	k	loL	5.0 10	0.26 0.65	_	0.22	0.44	_	0.18	-	mAd

ELECTRICAL CHARACTERISTICS (Continued)

Characteris	tic		9990	Symbol	VDD	Tic	w*		25°C	Mean	Thi	gh*	Unit
and nim Characteris	uc	Nilm	Max	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Offic
Input Current (AL Device)	0	-	0.05	lin 04	15	-	±0.1	100	± 0.00001	±0.1	-	± 1.0	μAdc
Input Current (CL/CP Device)	0 1		20.0	lin	15	-	±0.3	-	± 0.00001	±0.3	-9	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	a x			Cin			-	-	5.0	7.5	-	-	pF
Quiescent Current (AL Device) (Per Package)	9.6	9.4		IDD OF	5.0 10 15	-	5.0 10 20	-	0.005 0.010 0.015	5.0 10 20		150 300 600	μAdc
Quiescent Current (CL/CP Devic (Per Package)	ce)		3.0	IDD	5.0 10 15	-	20 40 80	1 -	0.005 0.010 0.015	20 40 80	v a:0	150 300 600	μAdc
	2.75 5.60 8.26	3.5 7.0 11.0	=	8 0.1 01 17 0.1 01 180	5.0 10 15		IT IT IT	= (3.	9 μΑ/kHz) 8 μΑ/kHz) 7 μΑ/kHz)	f + 10	D	0.5 or 1.0 or 1.5 or	μAdc

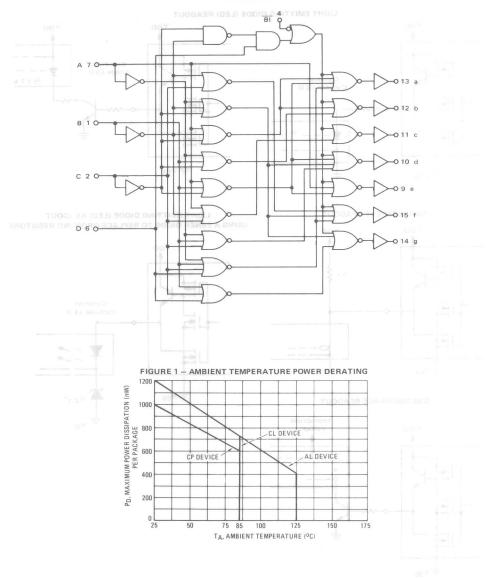
- * T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device Thigh = +125°C for AL Device, +85°C for CL/CP Device # Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

- † To calculate total supply current at loads other than 50 pF: IT (CL) = IT (50 pF) + 3.5 × 10 $^{-3}$ (CL $^{-50}$) VDDf where: IT is in μ A (per package), CL in pF, VDD in Vdc, and the label is least feed. and f in kHz is input frequency.
- ** The formulas given are for the typical characteristics only at 25°C. characteristics only at 25°C.

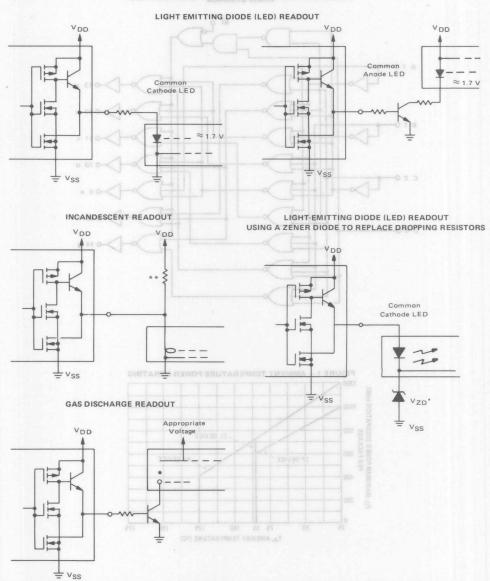
SWITCHING CHARACTERISTICS (C₁ = 50 pF, T_{\Delta} = 25°C)

2.9	-	4.2	haracter	ristic	3.6	tr.C.		Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
2.9 -			3.0						5.0	-	40	80	(de
Output Rise Time								tTLH	10	-	40	80	ns
								,	15	-	40	80	OB
9.0 - Vdc	-	9.2	8.8	-	8.6	01			5.0	-	125	250	all I
Output Fall Time								tTHL	10	-	75	150	ns
- 0.8								11112	15	-	70	140	OU.
14.2 - 1	1 - 1	14.3	14.1	-	13.9				5.0	-	750	1500	(lo
								tPLH	10	- 1	300	600	ns
18.0 - Vdc								1 211	15	-	200	400	00
Data Propagation De	lay Time	0.01							5.0	-	750	1500	Oll
								tPHL	10	_	300	600	ns
								1111	15	U=0	200	400	Grud C
obAm - 81.0		88.0	0.26	-	156.0	6,8	1 100	Surk	5.0	-	750	1500	(V)
								tPLH	10	- 1	300	600	ns
Blank Propagation D	elay Time	e b b						TEN	15	-	200	400	OVI
									5.0	CLO	500	1000	dolu0
								tPHL	10	-	250	500	ns
0.45 - 01500								1111	15	_	170	340	191





CONNECTIONS TO VARIOUS DISPLAY READOUTS



- ** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.
- V_{ZD} should be set at V_{DD} 1.3 V V_{LED}. Wattage of zener diode must be calculated for number of segments and worst-case conditions.



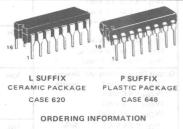
MC14549B MC14559B

집중요약하는 이렇게 되는 것 같아요 한다.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

SUCCESSIVE APPROXIMATION REGISTERS



MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

PIN ASSIGNMENT

		/ A 7 3	
1 🖂	Q4	VDD	16
2 =	Q5	□ Q3	15
3 =		Q2	1 4
4 =	Q7	ο ° α1	13
5 🗀	Sout	00	12
6 =	D	EOC	11
7 =	С		10
8 =	VSS	sc	9
1 1	CP David	JOL Ineru	

* For MC14549B Pin 10 is MR input For MC14559B Pin 10 is FF input

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $v_{SS}\, \mbox{or}\, v_{DD}$).

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analogto-digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable 0
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

obAu 0.1: Rating 10:	10000	Symbol	Value	Unit
DC Supply Voltage - 2.04	10000	· V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs - 25	0.6	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		1 -	10	mAdc
Operating Temperature Range - AL Dev CL/CP Dev		TA	-55 to +125 -40 to +85	°C =
Storage Temperature Range	arus	T _{stg}	-65 to +150	°C

	-bAu	MC14	549B		TRUTH TAE			M	C14559	9B 0
sc	SC(t-1)	MR	MR (1-1)	Clock	Action	sc	SC(t-1)	EOC	Clock	Action
×	X	×	×	7_	None	×	×	X	~_	None
×	×	1	×		Reset	1	0	0	7	Start Conversion
1	0	0	0		Start Conversion	×	1	0	7	Continue Conversion
1	×	0	1		Start Conversion	0	0	0 .	56V 0.	Continue
1	1	0	0		Continue Conversion	0	×	. 1	aby 8	Retain Conversion Result
0	×	0	×	7	Continue Previous Operation	1	X ransupsi	1 Fuga	i e(s)4)	Start Conversion

X = Don't Care

t-1 = State at Previous Clock



		VDD	Tio	w *		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
Vin VDD or 0		10	-	0.05	-	0	0.05		0.05	-
	031	15	-	0.05	-	0	0.05	-	0.05	
"1" Level	VOH	5.0	4.95	and a	4.95	5.0	and the s	4.95	0000	Vdc
V _{in} 0 or V _{DD}	I SOL	10	9.95	EG[STE	9.95	10	PITTIA.	9.95	เมลกร	
REGISTERS		15	14.95	-	14.95	15		14.95	W 0.55	
Input Voltage# "0" Level	VIL		and the	- Instant	Lastetle		The Later of	- dune	23.0	Vdc
(VO = 4.5 or 0.5 Vdc)		5.0	angle ion	1.5	tazigib	2.25	1.5	гедикег	1.5	5381
(VO = 9.0 or 1.0 Vdc)		10	pisaskuot	3.0	u-golens	4.50	3.0	MS8337IS	3.0	SIGHT.
(V _O = 13.5 or 1.5 Vdc)	Street I	15	ine Mast	4.0	control	6.75	4.0	1 5 Parts	4.0	SARE
"1" Level	VIH	2	Dill Usite	pileta 3(7)	111 DS1	DDB1 SI GI	PECKI ON	19(1) (1)(0	(3310)	19971
(VO = 0.5 or 4.5 Vdc)	200	5.0	3.5) briswrio	3.5	2.75	0 936 2H	3.5	rester i	Vdc
(V _O = 1.0 or 9.0 Vdc)	2 Hor	10	7.0	End_of-C	7.0	5.50	torralisan t	7.0	45598 il	MIC
(VO = 1.5 or 13.5 Vdc)	27	15	11.0	_	11.0	8.25	ed Lessi	11.0	upsazi (C	160
Output Drive Current (AL Device)	la		-gelans :	Dutani 8	BEERTO	FI DAS BUS	MC148	erit nor ar	00/162/100	mAde
(V _{OH} = 2.5 Vdc) Source	ІОН	5.0	-1.2	274	-1.0	51691.7	eith_ceria	-0.7	one letie	b-ol
(V _{OH} = 4.6 Vdc)	IARES	5.0	-0.25		-0.2	-0.36	2112-101	-0.14	THOSE - HOTE	-
(V _{OH} = 9.5 Vdc)	5	10	-0.23		-0.2	-0.36		-0.14		
		15	-1.8		-1.5	-3.5	is Opera	CANADAM STATE	ptaffy Syr	0
(V _{OH} = 13.5 Vdc)						-		-1.1	wester O III	-
(V _{OL} = 0.4 Vdc) Sink	IOL	5.0	1.28	-	1.02	1.76	nain	0.72	au2 slan	mAde
(VOL = 0.5 Vdc) Q Outputs	KRIDN I	10	3.2	-	2.6	4.5		1.8	Moo Tilling	
(V _{OL} = 1.5 Vdc)	1	15	8.4	-	6.8	17.6	-	4.8	EI UU-SI'II	5.0
(VOL = 0.4 Vdc) Sink		5.0	0.64	-	0.51	0.88		0.36	6190m/10	10
(VOL = 0.5 Vdc) Pin 5, 11 only	Total II	5.0	1.6	MayE pol	1.3	2.25	viithig V	0.9	Left transport	0 0
(VOL = 1.5 Vdc)		10	4.2	-	3.4	8.8	co.T.6M	2.4	DAT'TA	
Output Drive Current (CL/CP Device)	ІОН									mAde
(VOH = 2.5 Vdc) Source	.011	5.0	-1.0	_	-0.8	-1.7	-6A11/50,	-0.6	Datation III	1 4
(V _{OH} = 4.6 Vdc)		5.0	-0.2	-	-0.16	-0.36	ige ± 3.0	-0.12	bV yaqqa	20
(V _{OH} = 9.5 Vdc)		10	-0.5	ds. One	-0.4	-0.9	Twe Lo	-0.3	o simos	0 0
(V _{OH} = 13.5 Vdc)		15	-1.4	on Readt	-1.2	-3.5	wT-o.b	-1.0	u di - uni	6
(V _{OL} = 0.4 Vdc) Sink	la.	5.0	1.04	-	0.88	1.76	_	0.72	one El-mar	mAde
(VOL = 0.5 Vdc) Q Outputs	OL	10	2.6		2.2	4.5		1.8	ander only	1
(V _{OL} = 1.5 Vdc)		15	7.2	_	6.0	17.6		4.8		
	0			_	10000					
(VOL = 0.4 Vdc) Sink	1	5.0	0.52	-	0.44	0.88	-	0.36	-	
(V _{OL} = 0.5 Vdc) Pin 5, 11 only		10	1.3	-	1.1	2.25	-	0.9		
(V _{OL} = 1.5 Vdc)		15	3.6	-	3.0	8.8	Liber Table	2.4	MATTIN	MAIN
nput Current (AL Device)	lin	15	- 1	± 0.1	ladin	±0.00001	± 0.1	g all of	± 1.0	μAdc
nput Current (CL/CP Device)	lin	15 V	- 814	± 0.3	100	±0.00001	± 0.3	-	±1.0	μAdo
Input Capacitance	Cin	o bV	8.0.4 6	nV er 8.0	V	5.0	7.5	- 11	ignt-KA a	pF
(V _{in} = 0)			1	10				100	TSD DIETE	top cuid
Quiescent Current (AL Device)	I _{DD}	5.0	- 301	5.0		0.005	5.0		150	μAdd
(Per Package)	.DD	10	- 381	10	- 4	0.010	10	No.	300	1
(Clock = VSS		15	- 40	20	-	0.015	20	-	600	1
Quiescent Current (CL/CP Device)	la a	5.0	1	20	1 00	0.005	20		150	μAdo
(Per Package)	DD	10		40	_	0.005	40		300	μΑσο
(Clock = VSS		15		80		0.015	80		600	
	1-		171077	00	-				000	-
Total Supply Current * 1 944 FOM TO	IT	5.0				0.8 µA/kHz				μAdo
(Dynamic plus Quiescent,	6 0 1	10				1.6 µA/kHz				50%
Per Package)		15			T = (2.4 µA/kHz	I + IDD			1
(CL = 50 pF on all outputs, all										0
buffers switching)	No.	a ministra						-		

MOTOROLA

^{*}T_{IOW} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ VDD = 5.0 Vdc 2.0 Vdc min @ VDD = 10 Vdc

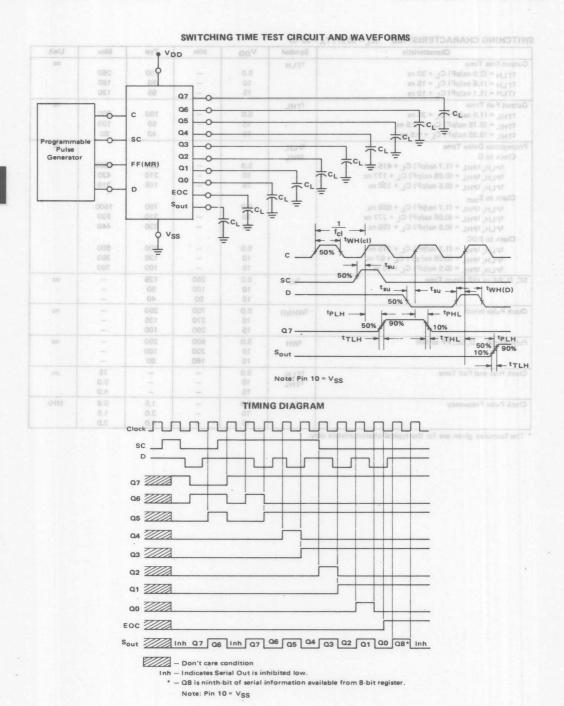
^{2.5} Vdc min @ V_{DD} = 15 Vdc

^{2.5} Vdc min @ V_{DD} = 15 Vdc 1TO calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + 2 \times 10^{-3} (C_L - 50) \text{ V}_{DD}$ where: I_T is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. "The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C1 = 50 pF, TA = 25°C) TEST SMIT DAMAGEMENT

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	[†] TLH					ns
tTLH = (3.0 ns/pF) CL + 30 ns		5.0	-	180	360	
tTLH = (1.5 ns/pF) CL + 15 ns		10		90	180	
tTLH = (1.1 ns/pF) CL + 10 ns		15	02 - 0	65	130	
Output Fall Time	^t THL					ns
t _{THL} = (1.5 ns/pF) C _L + 25 ns		5.0	-	100	200	
t _{THL} = (0.75 ns/pF) C _L + 12.5 ns		10	0-0-00	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	-0-140	40	80	
Propagation Delay Time	tPLH,		03			ns
Clock to Q	tPHL.					11 C 10 C 10 C
tpLH, tpHL = (1.7 ns/pF) CL + 415 ns		5.0		500	1000	
tpLH, tpHL = (0.66 ns/pF) CL + 177 ns		10	0 00	210	420	
tpLH, tpHL = (0.5 ns/pF) CL + 130 ns	10末 1	15	0	155	310	
Clock to Sout	1024		0- 201			
tpLH, tpHL = (1.7 ns/pF) CL + 665 ns,	100	5.0	0- 0	750	1500	
tp_H, tpHL = (0.66 ns/pF) CL + 277 ns	-2	10	_	310	620	
tpLH, tpHL = (0.5 ns/pF) CL + 195 ns		15	-	220	440	
Clock to EOC			88			
tpLH, tpHL = (1.7 ns/pF) CL + 215 ns		5.0	_	300	600	
tpLH tpHL = (0.66 ns/ pF) CL + 97 ns	V 3	10	_	130	260	
tpLH, tpHL = (0.5 ns/pF) CL + 75 ns	5.0	15	_	100	200	1
SC, D, FF or MR Setup Time	t _{su}	5.0	250	125	_	ns
(C)MW ¹ ··· ·· ·· ·· ·· ·· ·· ·· ·· ·· ·· ··	- 6	10	100	50	-	
503		15	80	40	_	
Clock Pulse Width	tWH(cl)	5.0	700	350	_	ns
V 380 N	,,,,,,,,,	10	270	135	_	
101		15	200	100	-	
Pulse Width - D, SC, FF or MR	twH	5.0	500	250		ns
W. W. O. T.	Sour	10	200	100	_	
CTYT-IN THE		15	160	80	_	
Clock Rise and Fall Time	tTLH,	5.0	_	-	15	μs
2aV ~ 0	THL	10	2-	_	5.0	
		15	_	- "	4.0	
Clock Pulse Frequency	A FIFCH O	5.0	_	1.5	0.8	MHz
		10	_	3.0	1.5	
		15	m m m	4.0	2.0	

^{*} The formulae given are for the typical characteristics only.



OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock

Operation of the various terminals is as follows:

C = Clock — A positive-going transition of the Clock is required for data on any input to be strobed into the circuit

SC = Start Convert — A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles

D = Data In — Data on this input (usually from a comparator in A/D applications) is entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and quaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B only) — Resets all output to 0 on positive-going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B only) — Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output following the least significant bit of the circuit to FF.E.g.,

for a 6-bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Note that Q1 and Q0 will still operate and must be disregarded.

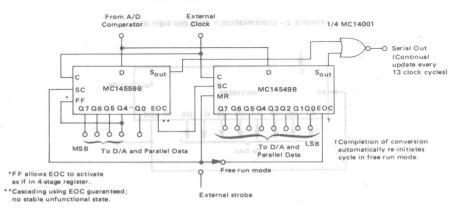
For 8-bit operation, FF is tied to Vss.
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Trying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (Sout) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while Sout of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs — After a conversion is initiated the O's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

 $EOC=End\ of\ Convert$ — This output goes high on the negative-going transition of the clock following FF = 1 (for the MC14559B) or the conditional reset of QO. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

Sout = Serial Out — Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 - 12-BIT CONVERSION SCHEME



TYPICAL APPLICATIONS

Externally Controlled 6-Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8-Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12-Bit ADC (Figure 4)

Because each successive approximation register (SAR) has a capability of handling only an eight-bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch-on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non-functional condition.

This 12-bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of

FIGURE 2 - EXTERNALLY CONTROLLED 6-BIT ADC

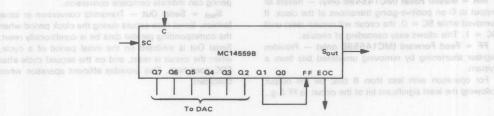
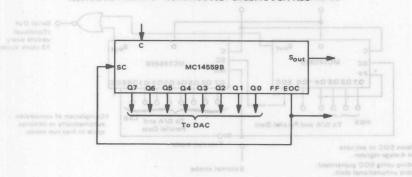
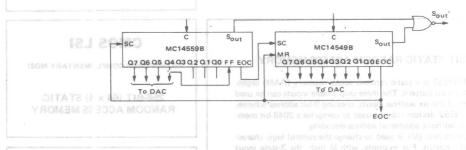


FIGURE 3 - CONTINUOUSLY CYCLING 8-BIT ADC



2





the 12-bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

Externally Controlled 12-Bit ADC (Figure 5)

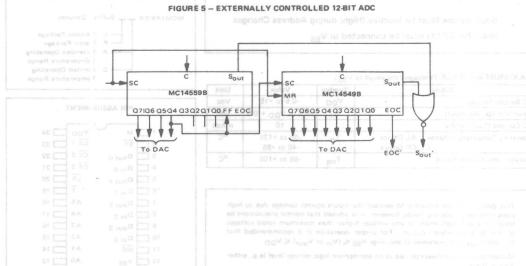
In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

Additional Motorola Parts for Successive Approximation ADC

Monolithic digital-to-analog converters - The MC1408/ villdixell (c.1508 converter has eight-bit resolution and is available with 6, 7, and 8-bit accuracy. The amplifier-comparator block - The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adiustable window.

With these two linear parts it is possible to construct SA-ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN-716.





MCM14552

MC14548E9 MC14559B

256-BIT STATIC RANDOM ACCESS MEMORY

The MCM14552 is a static random access memory (RAM) organized in a 64×4 bit pattern. The three chip enable inputs can be used as extensions of the six address inputs, creating 9-bit address scheme. Eight MCM14552 devices may be used to comprise a 2048-bit memory (512×4) without additional address decoding.

The mode control (M) is used to change the control logic characteristic of the circuit. For example, with M high, the 3-state input (T) fully controls the 3-state characteristic of the output. With M low, the output 3-state characteristic is controlled by chip enable inputs (CE), write enable input (WE) and T.

The memory is designed so that dc signals may operate the memory, with no maximum pulse width restrictions.

Medium speed, micropower operation, and control flexibility make the device useful in scratch pad or buffer applications where battery operation or high noise immunity are required.

- Quiescent Current = 50 μA/package typical @ 5 Vdc
- Noise Immunity = 45% of VDD typical
- 3-state Output Capability for Memory Expansion
 - Output Data Latch Eliminates Need for Storage Buffer
 - Access Time = 700 ns typical @ VDD = 10 Vdc
- Fully Decoded and Buffered
 - Supply Voltage Range = 3.0 Vdc to 18 Vdc
 - Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Note: Strobe Must be Inactive (High) during Address Changes Note: Pin 20(LE) must be connected to $\rm V_{SS}$

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1 1	10	mAdo
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

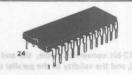
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{\mbox{SS}}$ or $V_{\mbox{DD}}$.

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

256-BIT (64 x 4) STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MCM14XXX Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

PIN ASSIGNMENT 1 M VDD 24 2 ST CE 1 23 CE 2 22 3 Dout 0 CE 3 21 20 20 7 4 Din 0 5 Dout 1 T 19 A5 18 T 6 Din 1 7 Dout 2 8 Din 2 A4 17 9 Dout 3 A3 16 10 Din 3 A2 15 11 WE A1 14 A0 13 12 VSS

ar the serial

ta is started

ELECTRICAL CHARACTERISTICS

			VDD	Tle	w*		25°C			igh [*]	
Character	istic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage	"0" Level	VOL	5.0	-	0.05		0	0.05	_	0.05	Vdc
Vin VDD or 0		0.2	10	-	0.05		0	0.05	-	0.05	
50			15	-	0.05	_	0	0.05	-	0.05	
	"1" Level	VOH	5.0	4.95	_	4.95	5.0	_	4.95	_	Vdc
Vin Oor VDD	1 20001	VOH	10	9.95	La Gara	9.95	10	201 1 218	9.95	N. N. CHOUSE	HO YIN
VIN OUT VID			15	14.95	(30°C)	14.95	15	GUT TREET	14.95	41117 2011	1011
state guist	"0" Level	V/	0110	14.55	- Control in	17.00	10		14.00		Vdc
Input Voltage#		VIL	5.0	HLITE	1.5	_	2.25	1.5		1.5	Vac
(V _O = 4.5 or 0.5 Vd			10		2007.50	-	2500000	3.0	H J (Title	3.0	CUTT
(V _O = 9.0 or 1.0 Vd		_	(No. 1)	-	3.0		4.50	4.0	- 7 <u>5</u> (40	4.0	LITT
(V _O = 13.5 or 1.5 V	dc)		15	-	4.0		6.75	4.0	4 5 1 1	4.0	177
	38 "1" Level	VIH				1				W JF IS	HURRING
(V _O = 0.5 or 4.5 Vd			5.0	3.5		3.5	2.75	- Art. 24.0	3.5	Jan 7 11 4	Vdc
(V _O = 1.0 or 9.0 Vd			10	7.0	-	7.0	5.50	25 ms_	7.0	25.30	100
(V _O = 1.5 or 13.5 V	dc) ^{Ge}		15	11.0	-	11.0	8.25	80 <u>8</u> 0.57	11.0		
Output Drive Current (AL Device)	ГОН	10.7						30 4 414		mAdc
(VOH = 2.5 Vdc)	Source	-	5.0	-1.2	1.2	-1.0	-1.7	-	-0.7	BOTH THE	V J BERR
(VOH = 4.6 Vdc)		-	5.0	-0.25	-	-0.2	-0.36	-	-0.14	-	
(VOH = 9.5 Vdc)		-	10	-0.62		-0.5	-0.9		-0.35		
(VOH = 13.5 Vdc)	1200		15	-1.8	3,4	-1.5	-3.5	-	-1.1	e all elo	O strill
(V _{OL} = 0.4 Vdc)	Sink	- 1-	5.0	0.64	-	0.51	0.88		0.36		mAdc
	SINK	OL	10	1.6	_	1.3	2.25	_	0.36	-	MAGC
(V _{OL} = 0.5 Vdc)			15		E1	3.4	8.8		2.4	81 272 m	agentib/
(V _{OL} = 1.5 Vdc)	608 00	191	0.015	4.2	9-11	3.4	8.8	_	2.4		
Output Drive Current (ОН	(3/1 (3/2)								mAdc
(V _{OH} = 2.5 Vdc)	Source	35	5.0	-1.0	-	-0.8	-1.7		-0.6		-
(V _{OH} = 4.6 Vdc)	08 8	18	5.0	-0.2	5-,1	-0.16	-0.36	-	-0.12	STOP DE	ndonis
(V _{OH} = 9.5 Vdc)		01	10	-0.5	-	-0.4	-0.9	-	-0.3	-	
(V _{OH} = 13.5 Vdc)		275	15	-1.4	_	-1.2	-3.5	_	-1.0		
(VOL = 0.4 Vdc)	Sink	IOL	5.0	0.52	2,4	0.44	0.88	sumiT s	0.36	nd of De	mAdc
(VOL = 0.5 Vdc)		08	0110	1.3	-	1.1	2.25	-	0.9	-	
(VOL = 1.5 Vdc)		69	8115	3.6	_	3.0	8.8	-	2.4	_	
Input Current (AL Devi	(e) (e)	lin	15	1. 3% bet	± 0.1	-	±0.00001	± 0.1	ploid seen	±1.0	µАdc
Input Current (CL/CP I			15	A. 12 (A.)	±1.0	1	±0.00001	±1.0	_	±14.0	μAdc
	Device)	lin	15		21.0	-		-		-	-
Input Capacitance		Cin	0.2		1,2	-	5.0	7.5	ile Patter	LAT TOP	pF
(V _{in} = 0)	450	701	0.0	FR)_1567	20.63		Branchina co		1900 00 110011		
Quiescent Current (AL	Device)	IDD	5.0	-	5.0	F	0.050	5.0	-	150	μAdc
(Per Package)	007	00	10	-	10	-	0.100	10		300	-
	1200	300	15	003.1700	20	-	0.150	20	16977,4 210	600	11 1000 111
Quiescent Current (CL/	CP Device)	IDD	5.0	-	50		0.050	50	_	375	μAdc
(Per Package)	200	135	10		100		0.100	100		750	MAGC
in -		0	15	(34) 422	200		0.150	200	_	1500	Read Set
Total Supply Current*	* USA-	0 1-	5.0	+	200						0.1-
A CONTRACTOR OF THE PROPERTY O		o IT	10	1			.98 µA/kHz				μAdc
(Dynamic plus Quie	scent,	6.8	and the second	CHINE			.96 µA/kHz				H basi
Per Package)		24	15	111/11/		'T = (5	.86 μA/kHz	סטי + דון			
(CL = 50 pF on all c	outputs, all	181	87								
buffers switching)				-							
Three-State Leakage Cu	rrent	ITL	15	(Q)=01	± 0.1	-	+0.00001	± 0.1		±3.0	μAdc
(AL Device)	902	10/2	0.1								
Three-State Leakage Cu	rrent	ITL	15		±1.0		+0.00001	± 1.0	_	± 7.5	μAdc
(CL/CP Device)	200	ins.	0.8	(G)vi2	A P		1			word 1	lo H

^{*}T_{IOW} = -55° C for AL Device, -40° C for CL/CP Device. Thigh = $+125^{\circ}$ C for AL Device, $+85^{\circ}$ C for CL/CP Device. "Noise immunity specified for worst-case input combination. Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc 2.0 Vdc min @ V_{DD} = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc †To calculate total supply current at loads other than 50 pF: $|T_{\uparrow}(C_{\downarrow})| = |T_{\uparrow}(50 \text{ pF})| + 4 \times 10^{-3} \text{ (C}_{\downarrow} -50) \text{ V}_{DD} \text{ f}$ where: $|T_{\downarrow}| \text{ is in } \mu\text{A (per package), } C_{\downarrow} \text{ in pF, V}_{DD} \text{ in Vdc, and f in kHz is input frequency.} **The formulas given are for the typical characteristics only at 25°C.$

								Symbo			
		DIOTION			0-1						
NG CHA	W. C		" (CL = 5	O pF, TA		20 64	200				
	Charac	teristic				Symbol	VDD	Min	Тур	Max	Un
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			9,50	-		- 1		1 7			- OV
			6.75								- 01
	.,				1	*****		Half Nam		100	ns
	oF) C1 +	25 ns							100	200	- GV
							10		50	100	- 01
= (0.55 ns	/pF) CL	+ 9.5 ns		0.41	-		15	1 -	40	80	isO Just
le Time	50		7.1.	67-	1, 2	tcvc(R)	5.0	1 -	2000	6000	ns
							0.210	-	750	2200	HOV
	'8E 0-		-0.9	-0.5		-0.62	01 15	-	500	1650	HO
cle Time				8.1	3,4	tcyc(W)	815.0	-	1200	3600	- ns
	0.36			0.51		18.0	0.810	101	750	2200	- JOY
	0.9		2.25	E.	1 - 5	1.8	-	-		100000000000000000000000000000000000000	- 101
to Strobe S	etup Tim	ie _		2.4	1,3	t _{su(A-ST)}					ns
							-	14 (1)	the state of the s	1	HQ NU
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Address F	The state of the s	100			1,3						Hins
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o Chin En	able Serui	n Time		-	2.4		-	_	-	-	n
o omp en					-,-			-			= 10)
	2.4			0.1		as	15	450	150	1.5 Videl	- 303
ble to Add	ress Hold	Time	1.5000 0±		2,4	th(CE-A)	5.0	450	150	nt fall Des	ns
		0.1+				-	10	300	100	POLICE IN	Curre
		3.5	0.3			-	15	225	75	#GHAZE	scha Du
Chip Ena	ole Pulse	Width Wh	en Reading		1,2	tWL(R)	5.0			-	ns
								400		JALInspu) triess
	T		001.0		03		100	_	+	Tomas	100 Par
Chip Ena	ble Pulse	Width Wh	en Writing	-	3,4	tWL(W)	45 3 - C- (CT)			-	ns
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op time					1 000	'su(H)	100				-
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ld Time		001	(=140) An an	31.5	1	th(R)	5.0	540	180	-	ns
				PARTY IN			10	240	60	the ner Roll	12 12
							15	180	45	Ipnidatava	exet) us
up Time		1.6 ±			3,4	t _{su(D)}	5.0	1800	600	Leamage Co	n
							10	600	200	- (60)	VL Dev
			.coooo.o+		1.0.1		15	450	150	Leakage C	818124
854					3,4	th(D)	5.0	600 150	200	Dayles	90 ns
d Time							1 10		50	_	
	NG CHA ise Time = (3.0 ns/i = (1.5 ns/i = (0.75 ns = (0.75 ns = (0.75 ns = (0.55 ns	NG CHARACTE Charactise Time = (3.0 ns/pF) C _L + = (1.5 ns/pF) C _L + = (1.5 ns/pF) C _L + all Time = (1.5 ns/pF) C _L + = (0.75 ns/pF) C _L - = (0.55 ns/pF) C _L - ele Time Address Hold Time o Chip Enable Seru Chip Enable Pulse Chip Enable Pulse	NG CHARACTERISTICS Characteristic ise Time = (3.0 ns/pF) C _L + 30 ns = (1.5 ns/pF) C _L + 25 ns = (1.1 ns/pF) C _L + 10 ns all Time = (1.5 ns/pF) C _L + 25 ns = (0.75 ns/pF) C _L + 25 ns = (0.55 ns/pF) C _L + 9.5 ns de Time O Strobe Setup Time Address Hold Time O Chip Enable Serup Time Chip Enable Pulse Width Who Chip Enable Pulse Width Who Chip Enable Pulse Width Who Time	NG CHARACTERISTICS* (C _L = 5) Characteristic ise Time = (3.0 ns/pF) C _L + 30 ns = (1.5 ns/pF) C _L + 25 ns = (1.1 ns/pF) C _L + 10 ns all Time = (1.5 ns/pF) C _L + 25 ns = (0.75 ns/pF) C _L + 12.5 ns = (0.75 ns/pF) C _L + 9.5 ns the Time Address Hold Time Address Hold Time Chip Enable Pulse Width When Reading Chip Enable Pulse Width When Writing Time	NG CHARACTERISTICS* (C _L = 50 pF, T _A Characteristic ise Time = (3.0 ns/pF) C _L + 30 ns = (1.5 ns/pF) C _L + 25 ns = (1.5 ns/pF) C _L + 10 ns all Time = (1.5 ns/pF) C _L + 25 ns = (0.75 ns/pF) C _L + 9.5 ns de Time Chip Enable Serup Time Address Hold Time Chip Enable Pulse Width When Reading Chip Enable Pulse Width When Writing Description: Address Hold Time Chip Enable Pulse Width When Writing Chip Enable Pulse Width When Writing Chip Enable Pulse Width When Writing	NG CHARACTERISTICS*	NG CHARACTERISTICS* (CL = 50 pF, TA = 25°C)	NG CHARACTERISTICS* (C _L = 50 pF, T _A = 25°C)	Characteristic Figure Symbol VDD Min	Characteristic Figure Symbol Vod Min Typ	NG CHARACTERISTICS* (CL = 50 pF, TA = 25°C)

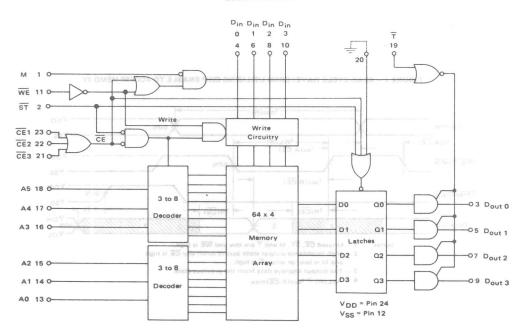
^{*} The formulae given are for the typical characteristics only.

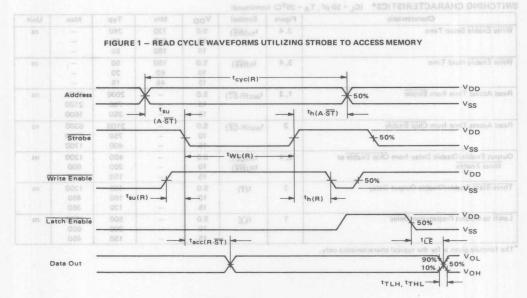
SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C}$) (continued)

Characteristic	Figure	Symbol	VDD	Min	Тур	Max	Unit
Write Enable Setup Time VROM3M SERGODA OT SECRETS	3, 4 DWISIJIT	t _{su(WE)}	5.0 10 15	720 240 180	240 80 55	- - -	ns
Write Enable Hold Time	3, 4	th(WE)	5.0 10 15	150 60 45	50 20 15	-	ns
Read Access Time from Strobe	1,3	t _{acc} (R-ST)	5.0 10 15	- X	2000 700 350	6000 2100 1600	ns
Read Access Time from Chip Enable	2	tacc(R-CE)	5.0 10 15	=	2100 750 400	6300 2250 1700	ns
Output Enable/Disable Delay from Chip Enable or Write Enable	2, 4	tR(CE), tR(WE)	5.0 10 15		400 200 150	1200 600 450	ns
Three-State Enable/Disable Output Delay	2	t(T)	5.0 10 15	(H)	400 160 120	1200 480 360	ns
Latch to Output Propagation Delay	1	tE	5.0 10 15	-	500 200 150	1500 600 450	ns

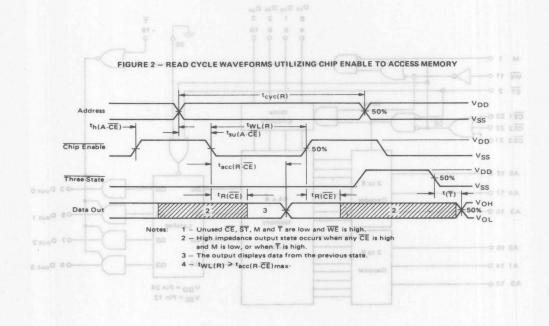
^{*}The formula given is for the typical characteristics only.

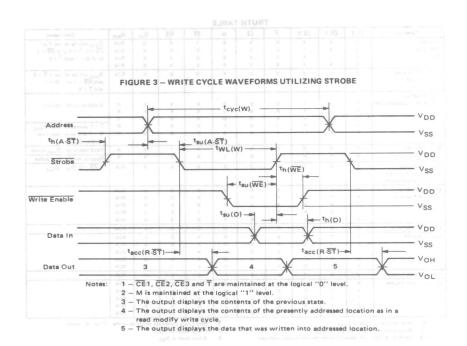
LOGIC DIAGRAM

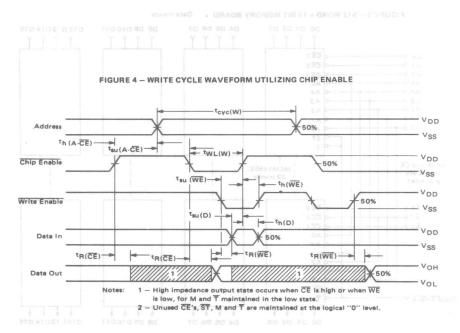




Notes: $1 - \overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and \overline{T} are low, M is high. $2 - \overline{WE}$ may be held high during the complete read cycle.





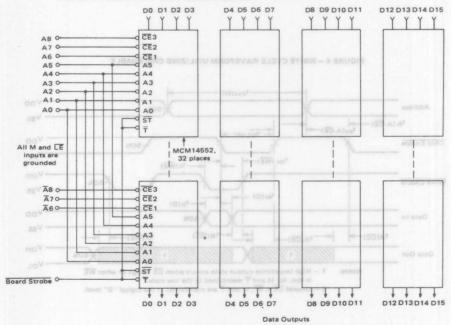


Function	CE 1	CE 2	CE 3	Ŧ	LE	M	ST	WE	Din	Dout	Comments
Address	×	X	×	X	X	×	1	×	×	R/A	Dout will be active if all
Changing	×	×	1	X	X	X	×	X	X	R/A	CE = 0, T = 0 and WE = 1
Valid	×	1	×	X	X	×	×	×	×	R/A	or if M = 1 and T = 0
	1	×	X	×	х	×	·X	×	X	R/A	
Address Changing	0	0	0	X	×	X	0	X	X	R/A	Dout will be active if T = 0
Not Valid		STRO	PISHO	TU BIN	VEPOR	PE MA	DYO BI	- WRE	E BRU	PIG	and $\overline{WE} = 1$ or if $M = 1$ and $\overline{T} = 0$
Dout Disabled											
(in high resistance state)	×	X	1	X	×	0	×	X	X	R	Disables write circuitry
	X	1	X	X	X	0	X	X	X	R	
05V	1	X	X	X	X	0	X	X	X	R	
	X	×	X	1	X	X	X	X	X	R	T = 1 always disables Dout
88V	×	×	×	×	×	0	×	0	×	R	M = 0 and write operation disables D _{out}
Dout Enabled	0	0	0	0	X	X	X	1	X	A	Read operation, Dout active
(in active state)	X	X	X	0	×	1	×	×	X	A	Read or write, Dout active
Read Addressed Memory Location Into Output Latch	0	0	0	X	0	×	0	×	×	R/A	If WE = 0, D _{in} = D _{out}
Disable Reading	×	×	1	X	×	×	X	×	×	R/A	
From Memory	X	1	1 X	×	X	X	×	X	×	R/A	aldend eritig
aaV	1	×	X	×	X	X	×	X	×	R/A	
00.	X	X	X	X	X	X	1	X	×	R/A	
	×	X	X	X	×	X	×	0	×	R/A	
Write Into Memory	0	0	0	X	×	×	0	0	A	R/A	
Write Disabled	Х	X	1	X	×	X	X	X	×	R/A	NI WAG
22V	X	1	×	X	×	X	×	X	×	R/A	
	1	X	X	X	×	X	×	X	X	R/A	
HOV	X	X	X	X	×	X	1	×	×	R/A	
AC.	X	X	X	X	×	X	X	1	X	R/A	24 G 828 G
Output Latch Enabled	0	0	0	X	0	×	0	×	×	R/A	
Output Latch Disabled	×	×	" laling	X	X	X	X	X	X	R/A	Notes
	×	1	×	X	X	×	X	X	×	R/A	
	1	×	X	×	×	V	×	×	×	R/A	
	×	×	X	×	1	X	X	×		R/A	
0.717.00	X	×	X	×	X	X	1 sales	X	X	R/A	

R - High resistance state at D_{out} X = Don't care condition (must be in the "1" or "0" state)
A - An active level of either VDD or VSS
I/A - An R or A condition depending on the don't care condition.

O - A low level at VSS
O - A low level at VSS

FIGURE 5 - 512 WORD x 16 BIT MEMORY BOARD , Data Inputs





MC14558B

BCD-TO-SEVEN SEGMENT DECODER

The MC14558B decodes 4-bit binary coded decimal data dependent on the state of auxiliary inputs, Enable and RBI, and provides an active high seven-segment output for a display driver.

An auxiliary input truth table is shown, in addition to the BCD to seven-segment truth table, to indicate the functions available with the two auxiliary inputs.

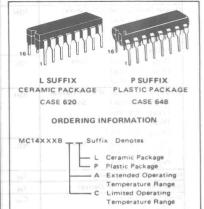
Leading Zero blanking is easily obtained with an external flip-flop in time division multiplexed systems displaying most significant decade first.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Segment Blanking for All Illegal Input Combinations
- Lamp Test Function
- Capability for Suppression of Non-Significant Zeros
- Lamp Intensity Function
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT DECODER



MAXIMUM RATINGS (Voltages referenced to Voc.)

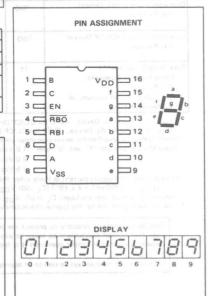
1.0	Rating	ac	300.0	Symbol	Value	Unit
DC Supply Voltage		40	010.0	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inp	outs	08	3,016	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per	Pin	not th	A/kHz)	1-112	10	mAdc
Operating Temperatur		AL Devic		TAT	-55 to +125 -40 to +85	°C
Storage Temperature	Range			T _{stg}	-65 to +150	°C

AUXILIARY INPUT TRUTH TABLE

Enable Pin 3	RBI Pin 5	BCD Input Code	RBO Pin 4	Function Performed
0	0.	×	0	Lamp Test
0	-1	×	1	Blank Segments
11 115130	30 4 018/8	0	1 1	Display Zero
Sind Since	0	0	0	Blank Segments
1	X	1.9	1	1-9 Displayed

X = Don't Care

RBI = Ripple Blanking Input RBO = Ripple Blanking Output



ELECTRICAL CHARACTERISTICS

		VDD	110	ow*		25°C		1 h	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
V _{in} V _{DD} or 0		10	-	0.05		0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
tona on"1" Level	VOH	5.0	4.95		4.95	5.0	=	4.95	0.00	Vdc
V _{in} 0 or V _{DD}	0	10	9.95	NEGO	9.95	10	FAEMS	9.95	08_	
		15	14.95	-	14.95	15	-	14.95	-	
nput Voltage# "0" Level	VIL									Vdc
(Vo. 4.5 or 0.5 Vdc)		5.0	ra dense	h 1.5 ins	h b ab oo	2.25	1.5	s588 de	1.5	T
(VO 9.0 or 1.0 Vdc)		10	s estrivo	3.0	S bas a	4.50	3.0	cus to et	3.0	dent
(VO 13.5 or 1.5 Vdc)		15	-	4.0	of the Tank	6.75	4.0	.m	4.0	witne
BROODER THE N'I' Level	VIH				7			Tuani v		A
(VO - 0.5 or 4.5 Vdc)		5.0	3.5	or noint	3.5	2.75	tath tat	3.5	SUXTIFAL I	Vdc
(VO = 1.0 or 9.0 Vdc)		10	7.0	lons avail	7.0	5.50	table, to	7.0	augas-nar	04.03
(VO = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	- 4	11.0	sifixus ov	it orlt
Output Drive Current (AL Device)	ГОН		doll dill	211132 XV 1	in three b	misted to	SECTION ST. B.	estribution of	tay Suipe	mAdc
(VOH 2.5 Vdc) Source	·OH	5.0	-3.0	t trom p	-2.4	-4.2	baxalqi	-1.7	ne divisi	13 101
(VOH 4.6 Vdc)	Str.	5.0	-0.64		-0.51	-0.88	_	-0.36	B first.	decad
(VOH = 9.5 Vdc)		10	-1.6		-1.3	-2.25	_	-0.9	_	
(VOH = 13.5 Vdc)	77	15	-4.2	_	-3.4	-8.8	_	-2.4	_	
(V _{OI} = 0.4 Vdc) Sink	la.	5.0	0.64	_	0.51	0.88		0.36		mAdc
(VOL = 0.5 Vdc)	IOL	10	1.6		1.3	2.25		0.36		MAGC
(VOL = 1.5 Vdc)		15	4.2	sbV 8 F	3.4	8.8	λn Ω.∂ =	2.4	Dujescent	
1.0[1977	15	4.2	30A 0 -						
Output Drive Current (CL/CP Device)	ЮН		0.5	- Constant	SPV 8	OF SHV (inge = 3.	H agano	A Aiddne	mAdc
(VOH = 2.5 Vdc) Source		5.0	-2.5	rations	-2.1	4.2	I IIA 101	-1.7	tnempe	0.
(V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc)		5.0	-0.52	-	-0.44	-0.88	- 776	-0.36	enT sms.	
			-1.3	SQIBZ	neo11.1	-2.25	0.01583.00	-0.9	aili d sqs0	- 05
(V _{OH} = 13.5 Vdc)	N. 17353	15	-3.6	-	-3.0	-8.8	กฮเฮอก	-2.4	ent uma.	-0
(VOL - 0.4 VOC) SINK	10L	5.0	0.52	ds, One	0.44	0.88	Two Lo	0.36	o el d agaű	mAdc
(V _{OL} = 0.5 Vdc)		10	1.3	tire Rate	ray bishe	2.25	wTho b	0.9	chottiky	1 1 1 1 1
(VOL = 1.5 Vdc)		15	3.6	-	3.0	8.8	-	2.4	ne Planute	
nput Current (AL Device)	lin	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	μAdc
nput Current (CL/CP Device)	lin	15	-	± 0.3	-	±0.00001	± 0.3	-	± 1.0	μAdc
nput Capacitance	Cin	_	-	-	-	5.0	7.5	-	_	pF
(V _{ID} = 0)	-111									
Quiescent Current (AL Device)	IDD	5.0	-	5.0		0.005	5.0		150	μAdc
(Per Package)	יטטי	10	_	10	_	0.003	10	_	300	
PIN ASSIGNMENT		15	_	20	_ 12	0.015	20	SS (Volt	600	UMIX
Julescent Current (CL/CP Device)	lon	5.0	1	20	Today	0.005	20	Sume		
(Per Package)	IDD	10	811	20	_ggv	0.005	40	-	150	μAdc
(rei rackage)		15	188+	40	wV	0.010	80	- 21	300	siloV to
	1		10415	00	1111	-			600	-
otal Supply Current**1	IT	5.0				.2 μA/kHz)				μAdc
(Dynamic plus Quiescent,	11	10	128			.4 μA/kHz)				T gnits
Per Package)	2 023	15	88		IT = (3	.6 μA/kHz)	f + IDD			
(C _L - 50 pF on all outputs, all	3 0		II nar							noT one

^{*}Tlow -55°C for AL Device, -40°C for CL/CP Device. Thigh = +125°C for AL Device, +85°C for CL/CP Device.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < (V_{in} or V_{out})

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

⁼Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" fevel = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

1To calculate total supply current at loads other than 50 pF:

IT(C_L) IT(50 pF) + 4 x 10⁻³ (C_L -50) V_{DD}f

where: |T| is in μ A (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency. **The formulas given are for the typical characteristics only at 25° C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C; see Figure 1)

Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time	tTLH .	k	k	R		ns
tTLH = (3.0 ns/pF) CL + 30 ns	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	5.0	(\ -	100	200	
tTLH = (1.5 ns/pF) CL + 15 ns		10	-	50	100	
tTLH = (1.1 ns/pF) CL + 10 ns	A A	15	A -	40	80	1
Output Fall Time	THL		-	4	-3	ns
tTHL = (1.5 ns/pF) CL + 25 ns		5.0	l -	100	200	1
tTHL = (0.75 ns/pF) CL + 12.5 ns		10	D - /	50	100	
t _{THL} = (0.55 ns/pF) C _L + 9.5 ns		15	-	40	80	
Propagation Delay Time	tPLH					ns
tpLH = (1.7 ns/pF) CL + 495 ns	-	5.0	-4	580	1160	-
tpl H = (0.66 ns/pF) CL + 187 ns		10	h - /	220	440	
tpLH = (0.5 ns/pF) CL + 120 ns		15	-	145	230	
Propagation Delay Time	tPHL	FF	T T	T	T'	ns
tpHL = (1.7 ns/pF) CL + 695 ns		5.0		780	1560	
tpHL = (0.66 ns/pF) CL + 242 ns		10	-	275	550	
tpHL = (0.5 ns/pF) CL + 160 ns		15	-	185	370	

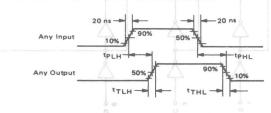
^{*} The formulae given are for the typical characteristics only.

TRUTH TARL

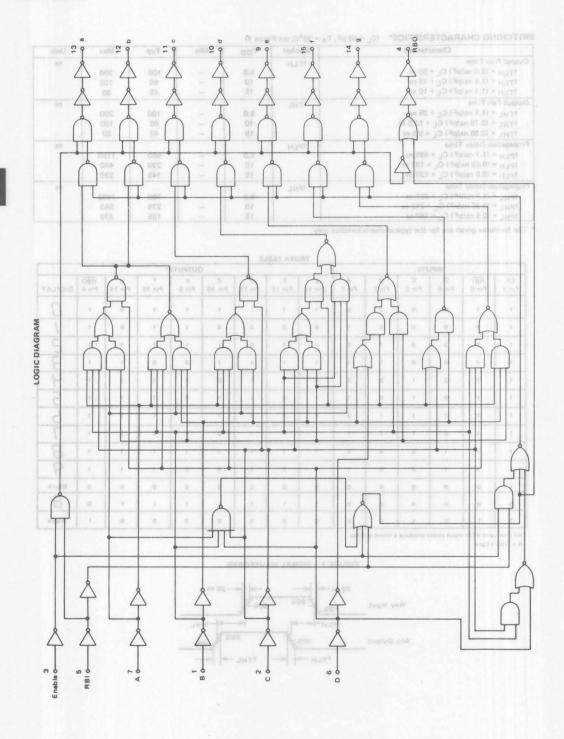
		INP	UTS							OUTPUT!	5.	9-0-		
En Pin 3	RBI Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	RBO Pin 4	DISPLA
1	1	0	0	0	0	13	1	1	1	1	1	0	1	0
1	×	0	0	0	1	0	0	0	0	1	1	0	1	1
1	×	0 7	0	1	0	15	21	0	7	15	0	15	1	2
1	×	0	0	1	1	1	1	1	1	0	0	1	1	3
1	×	0	1	0	0	0	1	1	0	0	1	1	1	4
1	×	0	1	0	1	1	0	1	. 1	0	1	1	1	5
1	×	0	1	1	0	0	0	1	1		1	1	1	Ь
1	×	0	1	1	1	1	1	1	0	0	0	0	1	7
1	×	1	0	0	0	1	1	4-19	1	1	1	1	1	8
1	×	, 1	0	0	1	1	1	1	0	0	1	1	1	9
1	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
0	0	×	×	×	×	1	1	1	1	1	1	1	0	8
0	1	×	×	×	×	0	0	0	0	0	0	0	1	Blank

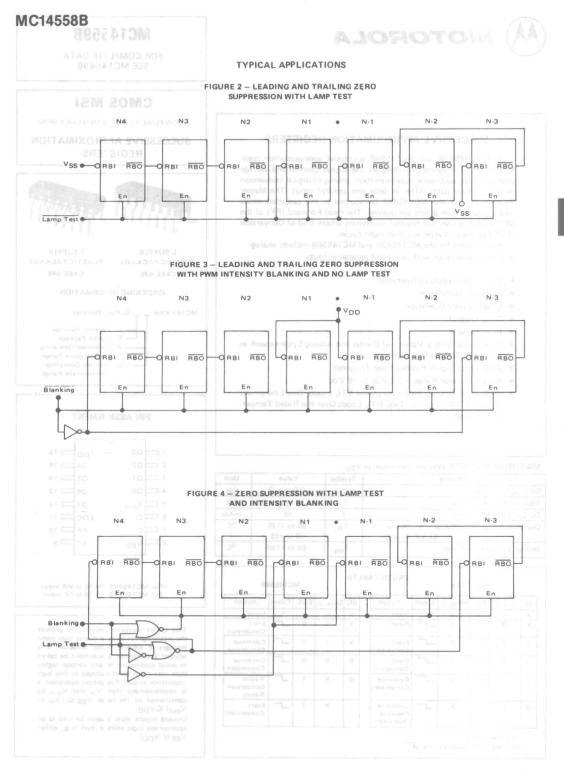
^{*}All non-valid BCD input codes produce a blank display.

FIGURE 1 - SIGNAL WAVEFORMS



X = Don't Care







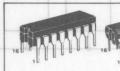
MC14559B

FOR COMPLETE DATA SEE MC14549B

CMOS MSI

LOW-POWER COMPLEMENTARY MOS

SUCCESSIVE APPROXIMATION REGISTERS



L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

PIN ASSIGNMENT

		V
Q3	VDD	1 6
Q2	04	15
Q1	Q5	14
00	Q6	13
Sout	Q7	12
D	EOC	11
С	FF	10
VSS	sc	9
	Q3 Q2 Q1 Q0 Sout D	Q2 Q4 Q1 Q5 Q0 Q6 Sout Q7 D EOC C FF

#For MC14549B Pin 10 is MR input For MC14559B Pin 10 is FF input

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or V_{DD}).

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549B and MC14559B successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analogto-digital conversion, with serial and parallel outputs.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

	MC145498				TRUTH TABLES					MC14559B						
sc	SC(t-1)	MR	MR (t-1)	Clock	Action	sc	SC(t-1)	EOC	Clock	Action						
×	×	×	X	7_	None	×	×	X	~	None						
X	×	1	×	7	Reset	1	0	0	7	Start Conversion						
1	0	0	0	7	Start Conversion	×	1	0	7	Continue						
1	×	0	1	7	Start Conversion	0	0	0	7	Continue						
1	1	0	0	7	Continue Conversion	0	×	1	7	Retain Conversion Result						
0	×	0	x	7	Continue Previous Operation	1	×	1	۲	Start Conversion						

X = Don't Care

t-1 = State at Previous Clock



MC14568B

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

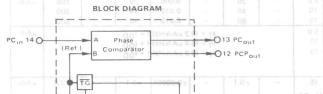
The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/or high noise immunity.

This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used separate of the programmable divide-by-N counter, for example cascaded with MC14569B (CTL low), MC14522B or MC14526B.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{sto}	-65 to +150	ос



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS



CERAMIC PACKAGE

CASE 620

P SUFFIX
PLASTIC PACKAGE

CASE 648

ORDERING INFORMATION

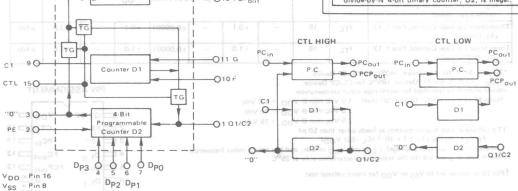
Suffix Denotes

L Ceramic Package
P Plastic Package
A Extended Operating
Temperature Range
C Limited Operating
Temperature Range

TRUTH TABLE

F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.





METASSER **ELECTRICAL CHARACTERISTICS**

		VDD	Tic	w*		25°C		Th	igh *	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0	_	0.05	-	0	0.05	-	0.05	Vdc
V _{in} V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	
CMOC MCI		15	-	0.05	W.S-121	TAOAS	0.05	PHIAS	0.05	
"1" Level	VOH	5.0	4.95	-00	4.95	5.0	WWAF	4.95		Vdc
Vin VO or VDD 19MOO REMOVE	OH I	10	9.95	- 671	9.95	10	univara	9.95		
		15	14.95	a divide	14.95	15	s be-attri	14.95	861 SM 6	17
Input Voltage#† "0" Level	VIL	-	nenid ri	I A VI-vd	divide	demmen	ong a b	ns notice	00 001	Vdc
(VO - 4.5 or 0.5 Vdc)	-15	5.0	lannada-9	1.5	w beta	2.25	1.5	bus-muitio	1.5	nuo
(VO 9.0 or 1.0 Vdc)		10	ALCOHOL: 1	3.0		4.50	3.0	CON-BAILTE	3.0	
(V _O = 13.5 or 1.5 Vdc)		15	HI (SOM)	4.0	idwga)	6.75	4.0	sanangs.	4.0	bite.
"1" Level	V	15	-	4.0	-	0.75	4.0	thic stru	-	personal services
	VIH		naivy no	prijuneti	0 to 850	righted for	been de	58B has	a MC145	IT.
(V _O = 0.5 or 4.5 Vdc)		5.0	3 5	synthes	3.5	2.75	000 M-v	3.5	eldimme	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	er dissipu	7.0	5.50	engiteb	7.0	locked by	searlo
(V _O = 1.5 or 13.5 Vdc)		15	11.0		11.0	8.25	-	11.0	-	
Output Drive Current (AL Device)	ІОН		de bose			draw de	an bonne	and com	and the same	mAdc
(VOH = 2.5 Vdc) Source	1538	5.0	-1.2	10023583	-1.0	-1.7	M Dush	-0.7	adivide si	11
(V _{OH} = 4.6 Vdc)	M Jac 1	5.0	-0.25	po meud	-0.2	-0.36	191/11/00	-0.14	aut_to 1	697LIO
(V _{OH} = 9.5 Vdc)		10	-0.62	d-abivit	-0.5	-0.9	10 91616	-0.35	no Ligin	JTO)
(V _{OH} = 13.5 Vdc)		15	-1.8	w), WC1	-1.5	-3.5	it riziw b	0-1.10	igmaxe r	101,101
(VOL = 0.4 Vdc) Sink	lou	5.0	0.64	_	0.51	0.88		0.36	526B	mAdc
(VOL = 0.5 Vdc) HDANDA9 DH		10	1.6	-	1.3	2.25	8.0 mA	0.9	O 17 -1 329i	0 0
(VOI = 1.5 Vdc)		15	4.2	_	3.4	8.8		2.4	the Coles	0 0
Output Drive Current (CL/CP Device)	1	-	-	-	- 1913	1 81 23 301	102 = 0	0.0571.006	Hav Alde	mAdc
(V _{OH} = 2.5 Vdc) Source	ІОН	5.0	-1.0	J enG ,	-0.8	-1.7	woul own	-0.6	to aldso	mAdc
		5.0	And the Park of the St. T.	e Rated	-0.16		OWT 10	-0.6	T yelltor	-80
(V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc)		10	-0.2	-		-0.36		1	a Range.	
	MET SILE	2.7	-0.5		-0.4	-0.9	-	-0.3	-	
(V _{OH} = 13.5 Vdc)	4	15	-1.4	-	-1.2	-3.5		-1.0	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	erefer mi	0.36	MATTAR	mAdc
(V _{OL} = 0.5 Vdc)	1	10	1.3	rulsV	1.1	2.25	-	0.9		-
(VOL = 1.5 Vdc)		15	3.6	MIN'S	3.0	8.8	-	2.4	-	
nput Current (AL Device)	lin	15	1 0	± 0.1	Too	±0.00001	± 0.1		± 1.0	μAdc
Input Current (CL/CP Device)	lin	15	1030 + 3	± 0.3	F	±0.00001	± 0.3	_ 0	±1.0	µAdc −
Input Capacitance		SDAM		01	1	5.0	7.5	- 1	1110	pF
(1)	Cin	50	128	- 55 to 1	A7	5.0	7.5	- sons R	mperature	Pr
ALCOHOL: THE SELECT		-	1		-	-	mund a	-		
Quiescent Current (AL Device)	IDD	5.0		5.0	-	0.005	5.0	-	150	μAdc
(Per Package)	Lung	10	- 081	- 100	-615	0.010	10	99/11	300	maT ag
COMMISSION CONTRACTOR	112.4	15	-	20	-	0.015	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0	-	20	-	0.005	20		150	μAdc
(Per Package)		10	-	40		0.010	40	SOTE	300	
0 64		15	-	80	- 1	0.015	80		600	2 11
Total Supply Current**†	IT	5.0			110	2 4 /1-11-1	6 + 1			μAdc
(Dynamic plus Quiescent,		10).2 µA/kHz)				OAL
Per Package)	b sdT	15).4 µA/kHz)				
(CL = 50 pF on all outputs, all	ebivib	13	1		17-10).9 µA/kHz)	1 + IDD			
buffers switching)		1								
		45	-	-0.4		T 0 0000	0.4			-
Three-State Leakage Current, Pins 1, 13	ITL	15	-	±0.1	- 1	± 0.00001	±0.1	- 10	± 3.0	μAdc
(AL Device)	1.0	TELLISIS.								
Three-State Leakage Current, Pins 1, 13	ITL	15		± 1.0	-	±0.00001	± 1.0	- 0	± 7.5	μAdc
(CL/CP Devices)			The same	OT	0				Imped !	

*T_{Iow} = -55°C for AL Device, -40°C for CL/CP Device.
Thigh = +125°C for AL Device, +85°C for CL/CP Device.

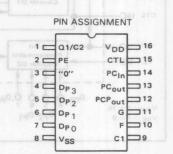
*Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF: $I_T(C_L)$ = $I_T(50 \text{ pF})$ + 1 x 10⁻³ (C_L -50) $V_{DD}f$

where: I is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

†Pin 15 is connected to V_{SS} or V_{DD} for input voltage test.

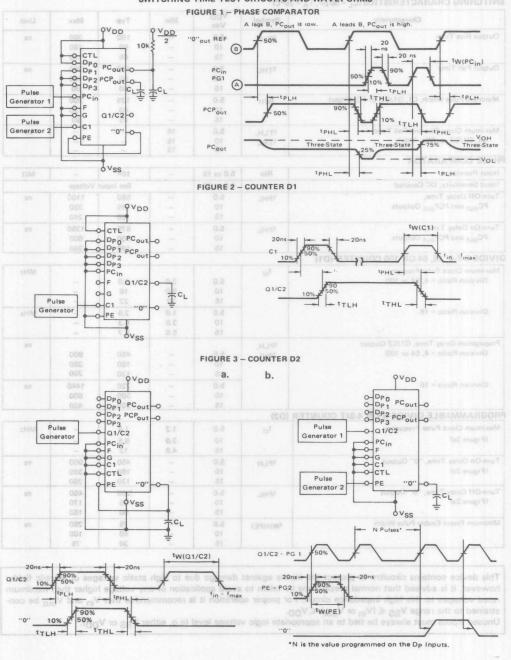


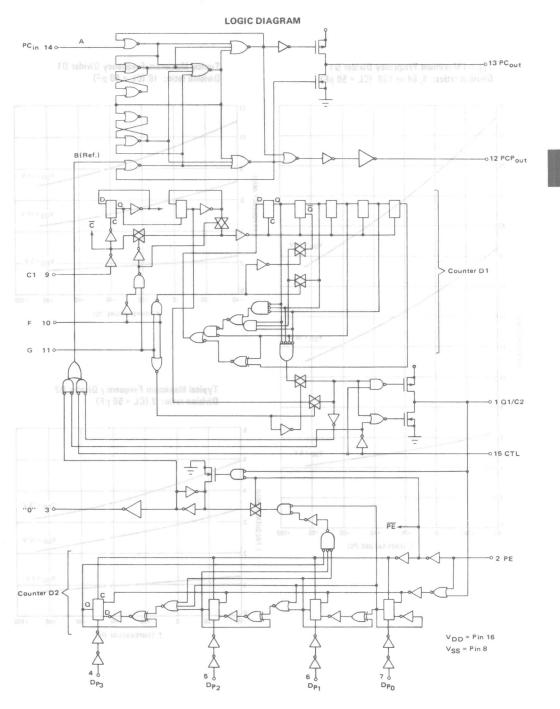
SWITCHING CHARACTERISTICS (CL = 50 pF, TA = 25°C)

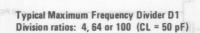
^t TLH	5.0				
-	5.0		180	360	ns
	10	- 3	90	180	
	15	-	65	130	
tTHL	5.0	- 0	100	200	ns
	10	-	50	100	
	15	-,04	40	80	
twH	5.0	_ =	125	250	ns
area No	10	-	60	120	
1	15	-	45	90	offe L
tTLH,	5.0	15	-0-0	-	μs
tTHL	10	15	-		
	15	15			
Rin	5.0 to 15	-	106	-	MΩ
rd BBT N UOS	5.0 to 15		See Input	Voltage	
tPHL	5.0	- 1	550	1100	ns
	10	-	195	390	
	15	-	120	240	
tPHL	5.0	-	675	1350	ns
20-0	10	- 0-	300	600	
13	15	-	190	380	
fcl					MHz
	5.0	3.0	6.0		
0.4402	10	8.0	16		
-	15	10	22	- 14	
	5.0	1.0	2.5	976	MHz
	10	3.0	6.3	_	
	15	5.0	9.7	_	
tPLH.					ns
tour	5.0	-	450	900	
ALIAN PARCO	10	-	190	380	
	15	-	130	260	
	5.0	_	720	1440	ns
	10	- 1	300	600	
	15	- 0-	200	400	
R (D2)		0-	100 FO	2	
fcl	5.0	1.2	1.8	807,7	MHz
	10	3.0	2010/04/2010	roleved	
	15	4.0	12		
tPLH	5.0	_	450	900	ns
	10	_	190	380	113
				260	
	15		130		
	-	-5-			ne
tPHL	15 5.0 10		225	450 170	ns
	5.0		225	450	ns
[†] PHL	5.0 10 15		225 85 60	450 170 150	
	5.0 10		225 85	450 170	ns
	TLH, tTHL Rin TPHL TPHL tPHL tPLH, tPHL R (D2)	15	15	15	15

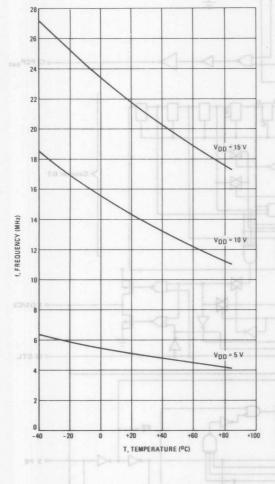
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

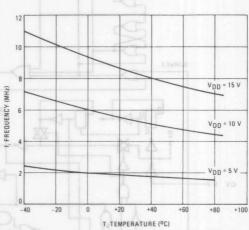




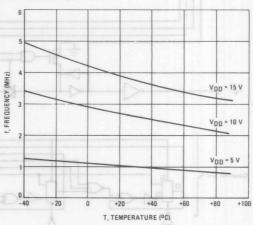




Typical Maximum Frequency Divider D1 Division ratio: 16 (CL = 50 pF)



Typical Maximum Frequency Divider D2 Division ratio: 2 (CL = 50 pF)



and a second manual SIISINTARIA CHARACTERISTICS (In a Preset Enable input enables that

The MC14568B contains a phase comparator, a fixed divider (\div 4, \div 16, \div 64, \div 100) and a programmable divide-by-N 4-bit counter.

PHASE COMPARATOR and to secure 8 tigit, the significant digit, the secure of the secur

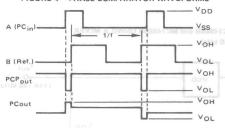
The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to Zero.

FIGURE 4 - PHASE COMPARATOR WAVEFORMS



If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A, and low otherwise.

Under the same conditions of frequency difference, the output will vary between VOH (or VOL) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

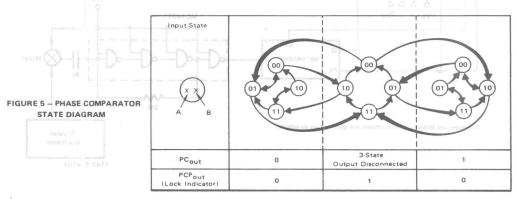
Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies.

DIVIDE BY 4. 16. 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to V_{DD} allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS}.

The different division ratios have been chosen to generate the reference frequences corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals



MC14568B

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs Dpo . . .

operation is obtained when the Control input is con-

Dp3 (pins 7 . . . 4). The Preset Enable input enables the parallel preset inputs Dp0 . . . Dp3. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

unters D1 transport range. The comparator is provided with a locked unters D1 to the comparator is provided with a locked unters.

FIGURE 6 - CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

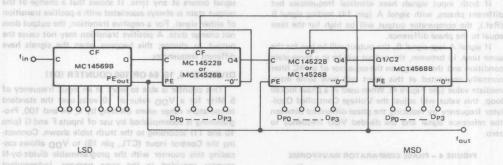
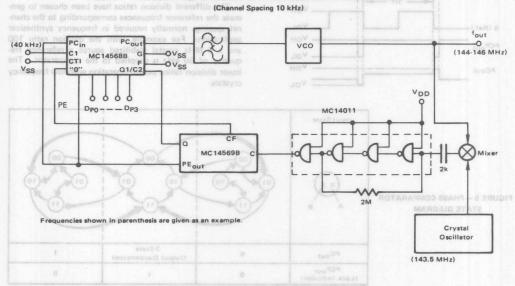


FIGURE 7 - FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER



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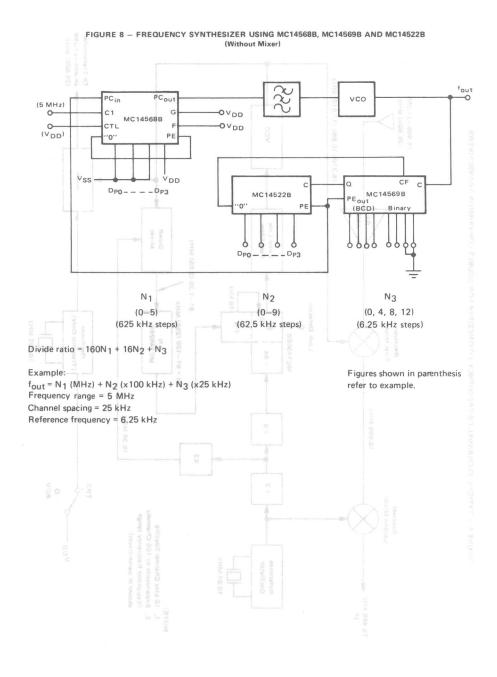
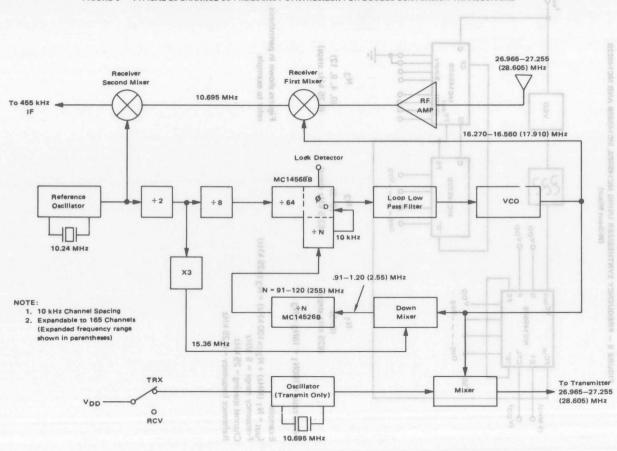


FIGURE 9 - TYPICAL 23-CHANNEL CB FREQUENCY SYNTHESIZER FOR DOUBLE CONVERSION TRANSCEIVERS





MC14573 MC14574 MC14575

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER QUAD PROGRAMMABLE COMPARATOR DUAL/DUAL PROGRAMMABLE AMPLIFIER-COMPARATOR

The MC14573, MC14574, and MC14575 are a family of quad operational low power amplifiers and comparators using the complementary P-channel and N-channel enhancement MOS devices in a single monolithic structure. The operating current is externally programmed with a resistor to provide a choice in the tradeoff of power dissipation and slew rates. The operational amplifiers are internally compensated.

These low cost units are excellent building blocks in consumer, industrial, automotive and instrument applications. Active filters, voltage reference, function generators, oscillators, limit set alarms, TTL-to-CMOS or CMOS-to-CMOS up converters, A-to-D converters and zero crossing detectors are some applications. These units are useful in both battery operated and line operated systems.

- Low Cost Quads
- Power Supply Single 3.0 to 15 Vdc

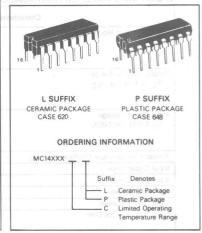
Dual ± 1.5 to ± 7.5 Vdc

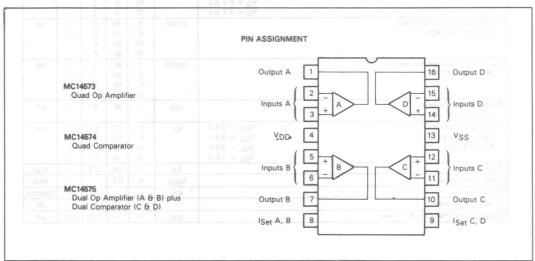
- Wide Input Voltage Range
- ullet Common Mode Range 0.0 to $V_{DD}-2.0$ Vdc for Single Supply
- Externally Programmable Power Consumption with One or Two Resistors
- Internally Compensated Operational Amplifiers
- High Input Impedance
- Comparators JEDEC B-Series Compatible

CMOS MSI

QUAD PROGRAMMABLE
OPERATIONAL AMPLIFIER
QUAD PROGRAMMABLE
COMPARATOR
DUAL/DUAL PROGRAMMABLE

OUAL/DUAL PROGRAMMABLE OPERATIONAL AMPLIFIER-COMPARATOR





DS9834

MAXIMUM RATINGS (Voltages referenced to Vss)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to $+18$	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain per Pin	1	10	mAdc
Programming Current Range	Set	2	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Package Power Dissipation*	PD	800 AOTA	mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{Out}) \leq V_{DD}$

MOTOROLA

DUAL/DUAL PROGRAMMABLE

RECOMMENDED OPERATING RANGE

Rating		Symbol	Value	Unit
DC Supply Voltage	sea a family of quad opera-	V _{DD} to V _{SS}	+3.0 to +15	Vdc
Programming Current	$V_{DD} = 3V$ 5 V < $V_{DD} < 15 V$	Set	2 to 50 2 to 750	μΑ

OPERATIONAL AMPLIFIER ELECTRICAL CHARACTERISTICS (I_{Set} = 20 μA, R_L = 10 MΩ, C_L = 15 pF, T_A = 25 °C)

Characteri	stic -ni remuenco ni stoold pri	Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
nput Common Mode Voltage Range	limit set alarms, TTL-to- A-to-D converters and zero tess units are useful in both		3 5 10 15	0 0 0	oltenu AGM stotoe	1.5 3.5 8.5 13.5	Vdc
Output Voltage Range R _L = 1 MΩ to VSS		Yor	3 5	0.05	= = (trial	2.95	Vdc
L SUFFIX P SUFFI		to 15 Vdc	10 15	0.05	Al <u>d</u> dr	9.95 14.90	9.8
Input Offset Voltage MC14573, MC14575	DE	VIO	3 5	epst	±5 ±8	±30 ±30	mVdc
ORDERING INFORMATION			10	nefl mma	± 10 ± 10	±30 ±30	0 0 0 50
Average Temperature Coefficient of V _{IO}	ΔV _{IO} /ΔΤ	-	-	15	mo l eig	μV/°C	
Input Capacitance	olifiers	Cin	aC-ba	eme	5	10	n pF
Input Bias Current		IIB		narche	arel in	50	II pA
Input Bias Current	$T_A = -40$ °C to $+85$ °C	1B	2.6-0.5	ОЭН	~ 2001	1	nA
Input Offset Current		110	-	-	-	100	pA
Open Loop Voltage Gain	V _O = 1 V p-p V _O = 3 V p-p	AVOL	3 5	2 8	8	_	V/m\
	$V_0 = 6 V p-p$		10	8	12	-	
	$V_0 = 9 V p-p$		15	8	12	-	
Power Supply Rejection Ratio MC14573, MC14575	PSRR	3 5 10 15	45 54 54 54	57 67 67 67	-	dB	
Common Mode Rejection Ratio MC14573, MC14575	Output A	CMRR	3 5 10 15	45 50 54 54	70 73 75 75	- HOM HO-	dB
Output Source Current VOH = VDD -0.6 V	A slugal	ЮН	-	55	80	-	μА
Output Sink Current $V_{in} += V_{DD}/2 + 0.5$ $V_{in} -= V_{DD}/2 - 0.5$	V _{OL} = 0.4 V V _{OL} = 0.4 V V _{OL} = 0.5 V V _{OL} = 1.5 V	lOL	3 5 10 15	2.1 2.5 5.5 15	4.2 5.0 - 11.0 30	10L 10L	mA
Slew Rate and	B atuqni	SR	-	0.6	0.8	-	V/µs
Unity Gain Bandwidth	- 3	G _{BW}	5	0.5	1	-	MHz
Phase Margin	h-1	, φM	0 T)	-	45	TUBE	Degree
THE RESIDENCE OF THE PARTY OF T	2010 10	3-11	THE PERSON NAMED IN	80	-C-	dB	
Channel Separation	Channel Separation Supply Current Per Pair (R ₁ = ∞)				00	CPU .	

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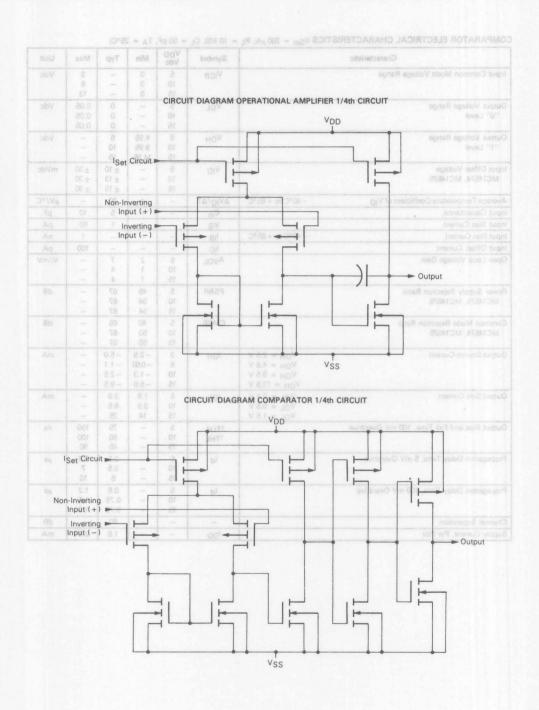
^{*}Derate above 25°C @ 4.6 mW/°C

			Charact	eristic		Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Input Common Me	ode Volta	age Rang		VICE		VICR	5	0	st_W	3	Vdc
							10	0	-	8	
8.5	-	.0	07				15	0	1-	13	
Output Voltage Ra						VOR	5	0.1	-	4.8	-
$R_L = 100K \text{ to } $	SS						10	0.1	Parg	9.8	Turnuf
60.0	- U		DI -				15	0.1	_	14.8	Vdc
Input Offset Volta						VIO	5	-	±8	± 30	mVdd
MC14573, MC14	15/5					1	10 15	-	± 10 ± 12	±30 ±30	idatul
Average Temperat	uro Coo			7707		ΔV _{IO} /ΔΤ	-	-	20		μV/°(
		incient of	V10				-	-	5		-
Input Capacitance		14.95				C _{in}	-	-		10	pF
Input Bias Current	8.		- 6	- OrV		IB	-	-	1	50	pA
Input Bias Current	84	-	- 8		$\Gamma_{A} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	IB	-	-	(CI#57)	M 16	nA
Input Offset Curre		-	- 01			10	-	-	-	100	pA
Open Loop Voltage	e Gain				$V_0 = 3 V p-p$	AVOL	5	1	2	-	V/m\
					$V_O = 6 V p-p$	OlA.	10	111400	3	-	Milking &
Hg 01	- 2	-			$V_O = 9 V p-p$		15	1	4	6,500	Lituan
Power Supply Rej		atio				PSRR	5	45	54	7	dB
MC14573, MC14	45/5					1	10	54	67	11-7	1100
				17/		01100	15	54	67	-	1770
Common Mode R		Hatio				CMRR	5	40 50	55 67	100	dB
MC14573, MC14	45/5					1	15	50	70	_	
Output Source Cu	rrent		- 01		V _{OH} = V _{DD} - 1.5 V	ГОН	-	550	800	_	μΑ
Output Sink Curre					V _{OH} = 0.4 V	loL	5	2.2	4.2	_	mA
odipat oli k odiro					$V_{OH} = 0.5 V$,OL	10	5.0	10.0	V III u	1110
					V _{OH} = 1.5 V		15	15	30	M _ 1	- 1
Slew Rate	587	5-4	ar.			SR	-	5	7	_	V/µs
Unity Gain Bandw	idth	23.	P	CMRR		GBW	5	1.5	3	-	MHz
Phase Margin	68	50	8	147179162		φM	-	-	48	N - 1	Degree
Channel Separation	n	24	D1			-	-	-	80	_	dB
Supply Current Pe		1 = 00)	81			IDD	<u> </u>	-	2.6	3.4	mA
очррку синстите	000 -	C2. U =	E	HO	A 9.7 = HOA	םטי ו			2.0	3.4	IIIA
			154								

COMPARATOR ELECTRICAL CHARACTERISTICS (ISet = 20 µA, RL = 10 MQ, CL = 50 pF, TA = 25°C) V_{DD} Vdc Symbol Min Тур Unit Characteristic VICR 1.5 Vdc Input Common Mode Voltage Range 0 5 0 3.5 10 0 8.5 15 0 13.5 0.05 Output Voltage Range VOL 3 0 Vdc "0" Level 0 0.05 10 0 0.05 15 0 0.05 3 2.95 3 Vdc Output Voltage Range VOH _ "1" Level 5 4 95 5 10 9.95 10 15 14.95 15 3 Input Offset Voltage VIO ±8 ±30 mVdc MC14574, MC14575 ±8 ±30 ± 10 10 ±30 ±30 15 ±10 Average Temperature Coefficient of VIO ΔVIO/ΔΤ 15 μV/°C Input Capacitance Cin _ 5 10 pF Input Bias Current IIB 50 pA Input Bias Current $T_{\Delta} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ IIB 1 nA Input Offset Current pA 100 10 Open Loop Voltage Gain 3 20 V/mV VOL)To 5 10 10 1 6 15 6 Power Supply Rejection Ratio PSRR 3 45 57 dB MC14574, MC14575 5 67 10 54 67 15 54 67 CMRR Common Mode Rejection Ratio 3 45 55 dB 50 MC14575, MC14575 65 10 54 67 15 54 67 $V_{OH} = 2.6 V$ 3 -0.35-065 Output Source Current mA $V_{OH} = 2.5 V$ 5 -2.5 -5.0 VOH = 4.6 V 5 -0.60-1.1 $V_{OH} = 9.5 V$ $V_{OH} = 13.5 V$ _ 10 -1.3-2.5 15 -5.0-9.5 V_{OL} = 0.4 V Output Sink Current 3 1.3 2.6 _ mA IOL $V_{OL} = 0.4 V$ 5 19 38 _ $V_{OL} = 0.5 V$ 10 3.5 6.5 - $V_{OL} = 1.5 V$ 15 14 25 Output Rise and Fall Time, 100 mV Overdrive tTLH, 3 140 250 THL 5 100 180 10 120 200 15 140 250 Propagation Delay Time, 5 mV Overdrive 3 15 30 td μS 5 10 20 10 _ 12 24 15 15 30 Propagation Delay Time, 100 mV Overdrive td 3 4 8 5 2 4 10 3 6 15 4 8 Channel Separation 80 dB Supply Current, Per Pair IDD 250

COMPARATOR ELECTRICAL CHARACTERISTICS (ISet = 200 μ A, RL = 10 M Ω , CL = 50 pF, TA = 25°C)

Characteristic		Symbol	V _{DD} Vdc	Min	Тур	Max	Unit
Input Common Mode Voltage Range		VICR	5 10 15	0 0 0	-	3 8 13	Vdc
Output Voltage Range ''0'' Level	agV	VOL	5 10 15	- - -	0 0 0	0.05 0.05 0.05	Vdc
Output Voltage Range "1" Level		Voн	5 10 15	4.95 9.95 14.95	5 10 15	-	Vdc
Input Offset Voltage MC14574, MC14575	Lagrana	VIO	5 10 15		± 10 ± 13 ± 15	±30 ±30 ±30	mVdc
Average Temperature Coefficient of V _{IO}	-40°C to +85°C	ΔV _{IO} /ΔΤ	-	Dimney	20	_	μV/°C
Input Capacitance		Cin	-	rie in	5	10	pF
Input Bias Current	- Jane	IFB	4 ,	E Difference	1	50	рА
Input Bias Current	-40°C to +85°C	IIB		1-2 10	gal —	1	nA
Input Offset Current	1 1	10	1 -	-	-	100	рА
Open Loop Voltage Gain		AVOL	5 10 15	2 1 1	7 4 4	-	V/mV
Power Supply Rejection Ratio MC14574, MC14575		PSRR	5 10 15	45 54 54	67 67 67	-	dB
Common Mode Rejection Ratio MC14574, MC14575		CMRR	5 10 15	40 50 50	65 67 67	-	dB
Output Source Current	VOH = 2.5 V VOH = 4.6 V VOH = 9.5 V VOH = 13.5 V	ЮН	3 5 10 15	-2.5 -0.60 -1.3 -5.0	-5.0 -1.1 -2.5 -9.5	-	mA
Output Sink Current	V _{OL} = 0.4 V V _{OL} = 0.5 V V _{OL} = 1.5 V	DA JOL DA	5 10 15	1.9 3.5 14	3.8 6.5 25	-	mA
Output Rise and Fall Time, 100 mV Overdrive	tTLH, tTHL	5 10 15		75 50 45	150 100 90	ns	
Propagation Delay Time, 5 mV Overdrive	ПЩ	td	5 10 15	-	2.5 3.5 5	5.0 7 10	μS
Propagation Delay Time, 100 mV Overdrive		td	5 10 15	-	0.6 0.75 0.75	1.2 1.5 1.5	μS
Channel Separation	Lucy for	J -	-	-	80	entres.	dB
Supply Current, Per Pair		IDD	-		1.8	2.5	mA



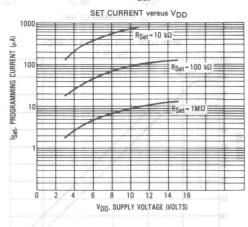
The programming current I_{Set} is fixed by an external resistor R_{Set} connected between V_{SS} and either one or both of the I_{Set} pins (8 and 9). When two external programming resistors are used, the set currents for each op amp pair or comparator are given by:

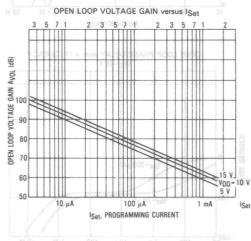
$$I_{Set} (\mu A) \approx \frac{V_{DD} - V_{SS} - 1.5}{R_{Set} (M\Omega)}$$

Pins 8 and 9 may be tied together for use with a single programming resistor. The set currents for each op amp pair or comparator pair afe then given by:

ISet A, B = ISet C, D (
$$\mu$$
A) $\approx \frac{VDD - VSS - 1.5}{2 \text{ Rset } (M\Omega)}$

The total device current is typically 13 times I_{Set} per pair if the outputs are in the low state, and 5 times I_{Set} per pair if the outputs are in the high state. For op amps with an output in the linear region the device current will be between the values of 5 times and 13 times I_{Set}.





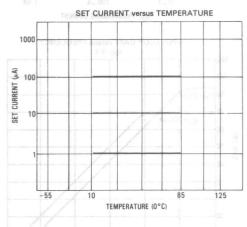
If a pair of op amps is not used, the I_{Set} pin for that pair may be tied to V_{DD} for minimum power consumption. To minimize power consumption in an unused pair of comparators this is not effective. The comparators should use a high value set resistor and the inputs should be set to a voltage that will force the output to V_{DD} (i.e., + in = V_{DD} , - in = V_{SS}).

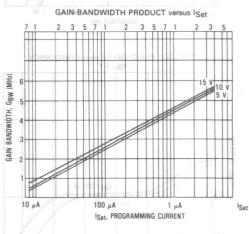
It should be noted that increasing I_{Set} for comparators will decrease propagation delay for that comparator.

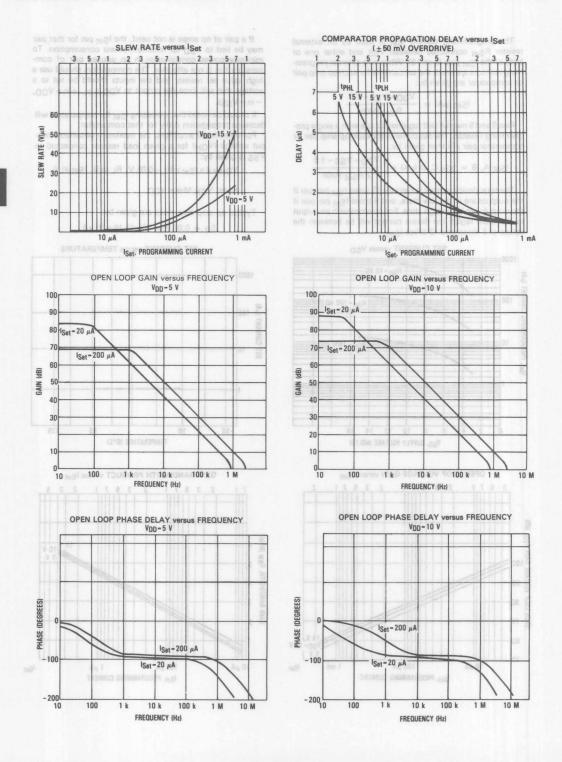
For operational amplifiers, the maximum obtainable output voltage (VOH) for a given load resistor connected to VSS is given by:

Note: VOH Max = VDD

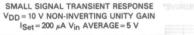
Typical op amp slew rates are given by:

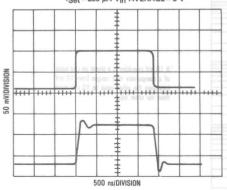




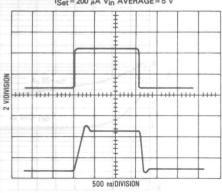


MC14573+MC14574+MC14575

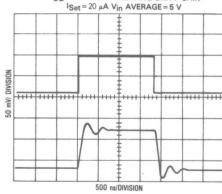




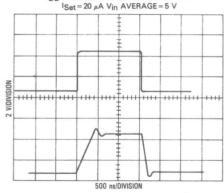




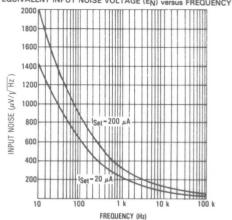
SMALL SIGNAL TRANSIENT RESPONSE $V_{DD} = 10 \text{ V}$ NON-INVERTING UNITY GAIN $I_{Set} = 20 \text{ } \mu\text{A} \text{ } V_{In} \text{ AVERAGE} = 5 \text{ V}$



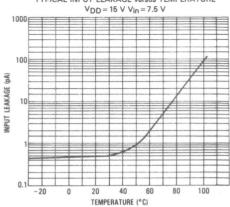
LARGE SIGNAL TRANSIENT RESPONSE $V_{DD} = 10 \text{ V}$ NON-INVERTING UNITY GAIN

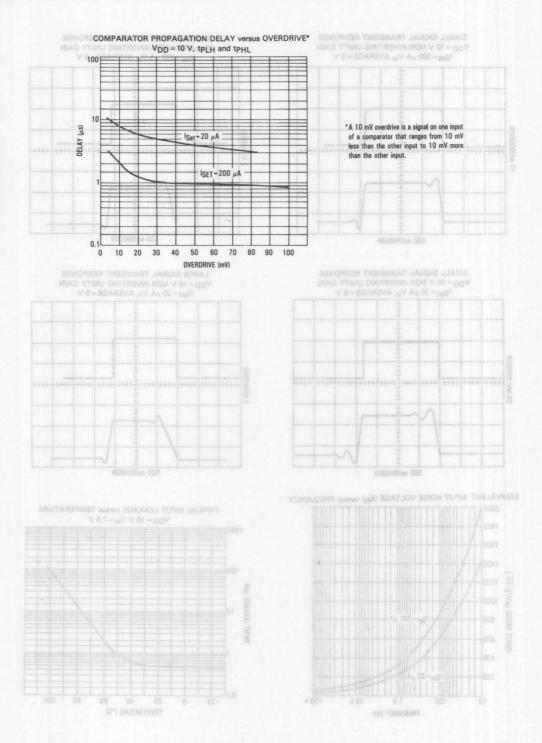


EQUIVALENT INPUT NOISE VOLTAGE (EN) versus FREQUENCY



TYPICAL INPUT LEAKAGE versus TEMPERATURE







4 x 4 MULTIPORT REGISTER

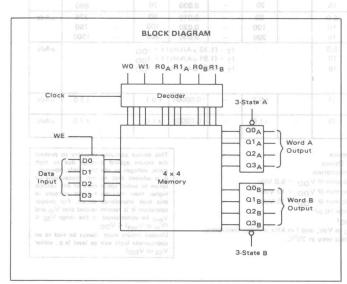
The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin Compatible with CD40108

MAXIMUM RATINGS (Voltages referenced to VSS)

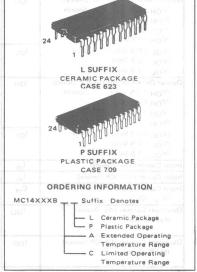
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	or o vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin	00.02	10	mAdo
Operating Temperature Range – AL Device CL/CP Device	TA	-55 to +125 -40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

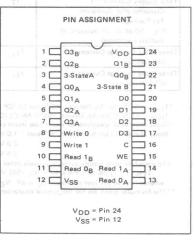


CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER





ELECTRICAL CHARACTERISTICS

		VDD	Tio	w*		25°C		Thigh*		
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Unit
Output Voltage "0" Level	VOL	5.0		0.05	-	0	0.05	-	0.05	Vdd
V _{in} V _{DD} or 0		10	-	0.05	-	0	0.05	-	0.05	1
		15	-	0.05	GHSTE	090	0.05	AZA	0.05	
12 Level	VOH	5.0	4.95	-	4.95	5.0	vel à s	4.95	35. x 150. x	Vdd
V _{in} 0 or V _{DD}		10	9.95	ITUDEN JE	9.95	10	-	9.95	SHA CINE A	
		15	14.95	endinos (14.95	15	dauRigue	14.95	im bag n	STRIGE
nput Voltage# "O" Level	VIL		mapringe	CHIL SAVEN	0.31 .21	priesidale	8591018	\$160 Yes	20 0118	Vdc
(VO 4.5 or 0.5 Vdc)		5.0	Approprie	1.5	id te byo	2.25	1.5	DW DWI	1.5	DEST
(V _O 9.0 or 1.0 Vdc)		10	-	3.0	-	4.50	3.0	10 400 /	3.0	Maritan
(V _O = 13.5 or 1.5 Vdc)		15	ent to eg	4.0	901-10	6.75	4.0	ns enign	4.0	PA.
A TRIBER HOST "1" Level	VIH		SILA MOSS		the cor	put is low,	ni sidan	STILL S	it usuM.	clock
(V _O = 0.5 or 4.5 Vdc)		5.0	3.5	-	3.5	2.75	bowstle	3.5	3020 0 05 9	Vdc
(V _O = 1.0 or 9.0 Vdc)		10	7.0	-	7.0	5.50	No zonis	7.0	ric Swine	610
(V _O = 1.5 or 13.5 Vdc)		15	11.0	-	11.0	8.25	-	11.0	printing one	
Output Drive Current (AL Device)	ІОН			- 6.61	10 1 H6-5	DE 25174 10	lock Imp	One on U	Hestrict	mAdd
(VOH = 2.5 Vdc) Source		5.0	-3.0	-	-2.4	-4.2	-	1.7	tuC also	88 0
(V _{OH} = 4.6 Vdc)		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
(V _{OH} = 9.5 Vdc)		10	-1.6	-	-1.3	-2.25	-	-0.9	nesitif stg	e Silv
(V _{OH} = 13.5 Vdc)		15	-4.2	Tob Vi	-3.4	-8.8	g\An 01	-2.4	O Difference	0.0
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.64	-	0.51	0.88	0.0 = 8	0.36	loV ylar	mAdd
(V _{OL} = 0.5 Vdc)		10	1.6	-	1.3	2.25		0.9	HON AIGH	00.0
(VOL = 1.5 Vdc)		15	4.2	S, Omi Li	3.4	8.8	vo t ow	2.4	to alder	0 Cap
Output Drive Current (CL/CP Device)	ІОН		Temper-	Dellin ari	28AO S	HTL Lose	OW I TO	bsol J	T yallto	mAd
(VOH = 2.5 Vdc) Source		5.0	-2.5	-	-2.1	-4.2	-	-1.7	egn a fil en	206
(V _{OH} = 4.6 Vdc)		5.0	-0.52	-	-0.44	-0.88	OPTIO:	-0.36	Compa	a Pil
(V _{OH} = 9.5 Vdc)		10	-1.3	-	-1.1	-2.25	-	-0.9	-	
(V _{OH} = 13.5 Vdc)		15	-3.6	-	-3.0	-8.8	-	-2.4	-	
(VOL = 0.4 Vdc) Sink	IOL	5.0	0.52	-	0.44	0.88	ra rager est	0.36	MITAH	mAde
(V _{OL} = 0.5 Vdc)		10	1.3	Pulp¥	1,1000	2.25		0.9	A -	
(V _{OL} = 1.5 Vdc)		15	3.6	018.0-	3.0	8.8	-	2.4	Touris	V ylag
nput Current (AL Device)	lin	15	(m) + /	± 0.1	1-1	± 0.00001	± 0.1	- /	± 1.0	μAdd
nput Current (CL/CP Device)	lin	15	-	± 0.3		±0.00001	± 0.3	- 0	±1.0	μAdd
nput Capacitance	Cin	-00	201	€ o788-		5.0	7.5	- Sinch	niul a rson	pF
(Vin = 0)	KARDAK		11 36		1 4			- agricultur	astrite sortis	Di Dini
Quiescent Current (AL Device)	1 _{DD}	5.0	- 031	5.0	1-	0.010	5.0	0.01.07	150	μAdd
(Per Package)	.00	10	001	10	11.9	0.020	10	- ugni	300	1000
L- P Plastic Pockage		15	-	20	-	0.030	20	-	600	
Quiescent Current (CL/CP Device)	IDD	5.0		50		0.010	50		375	μAdo
(Per Package)	100	10		100	_	0.010	100		750	μΑσι
Temberature Range		15	-	200	_	0.030	200	_	1500	
otal Supply Current**†	IT	5.0			1 11	.18 µA/kHz	1411			μAdd
(Dynamic plus Quiescent,	-1	10				.18 μΑ/KHZ				имас
Per Package)		15				.67 μA/kHz				
(CL = 50 pF on all outputs, all					1	METATIO				
buffers switching)										
hree-State Leakage Current	ITL	15		±0.1		1.0.00001	± 0.1		±3.0	μAdo
(AL Device)	11	13		20.1838	The Things	0.00001	2 0.1	-	23.0	μΑσο
The state of the s	I	15		+10		0.00001	± 1.0		± 7.5	1
Three-State Leakage Current	ITL	15	-	±1.0		0.00001	± 1.0	Labora .	2 /.5	μAdd

^{*}T_{low} = -55°C for AL Device, -40°C for CL/CP Device.

Thigh = +125°C for AL Device, +85°C for CL/CP Device.

*Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc

This device contains circuitry to protect This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{in} be constrained to the same Voc 6. Vout be constrained to the range VSS ≤ (Vin or Vout) ≤ VDD.

MOTOROLA

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

^{2.0} Vdc min @ VDD = 10 Vdc 2.5 Vdc min @ V_{DD} = 15 Vdc

^{2.5} Vdc min @ VDD = 15 Vdc

1To calculate total supply current at loads other than 50 pF:

1T(CL) = IT(50 pF) + 4 x 10⁻³ (CL -50) VDDf

where: IT is in µA (per package), CL in pF, VDD in Vdc, and f in kHz is input frequency.

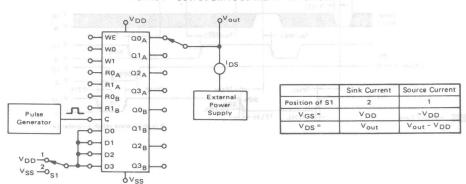
**The formulas given are for the typical characteristics only at 25°C.

WITCHING CHARACTERISTICS*	(C) = 50 pF TA = 25°C)	

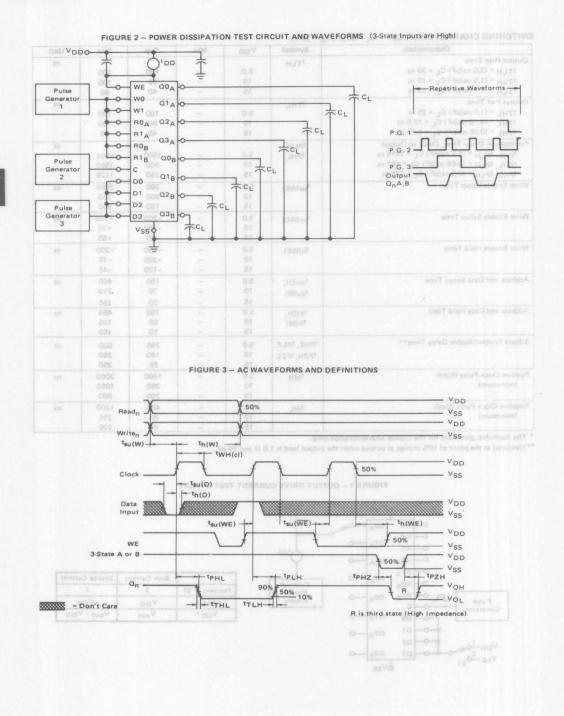
Characteristic	Symbol	VDD	Min	Тур	Max	Unit
Output Rise Time t _{TLH} = (3.0 ns/pF) C _L + 30 ns t _{TLH} = (1.5 ns/pF) C _L + 15 ns	^t TLH	5.0 10	1.	100 50	200	ns
t _{TLH} = (1.1 ns/pF) C _L + 10 ns		15	_	40	80	
Output Fall Time tTHL = (1.5 ns/pF) CL + 25 ns tTHL = (0.75 ns/pF) CL + 12.5 ns tTHL = (0.55 ns/pF) CL + 9.5 ns	17HL	5.0 10 15		100 50 40	200 100 80	ns
Propagation Delay Time, Clock to Output tPHL, tpLH = (1.7 ns/pF) CL + 1415 ns tPHL, tpLH = (0.66 ns/pF) CL + 467 ns tPHL, tpLH = (0.5 ns/pF) CL + 325 ns	tPLH, tPHL	5.0 10 15	-	1500 500 350	4500 1500 1125	ns
Write Enable Setup Time	† _{su} (WE)	5.0 10 15	o	800 300 180	2000 750 550	ns
Write Enable Setup Time	t _{su} (WE)	5.0 10 15		-300 -100 -60	+150 +75 +55	ns
Write Enable Hold Time	[†] h(WE)	5.0 10 15	=	-800 -300 -180	-200 -75 -45	ns
Address and Data Setup Time	^t su(D), ^t su(W)	5.0 10 15		150 70 50	450 210 160	ns
Address and Data Hold Time	th(D), th(W)	5.0 10 15	-	160 65 50	480 195 150	ns
3-State Enable/Disable Delay Time**	tPHZ, tPLZ, tPZH, tPZL	5.0 10 15	-	355 140 85	900 350 250	ns
Positive Clock Pulse Width (minimum)	HW [‡]	5.0 10 15	_	1000 350 200	3000 1050 800	ns
Negative Clock Pulse Width (minimum)	tWL	5.0 10 15	-	400 85 60	1200 255 200	ns

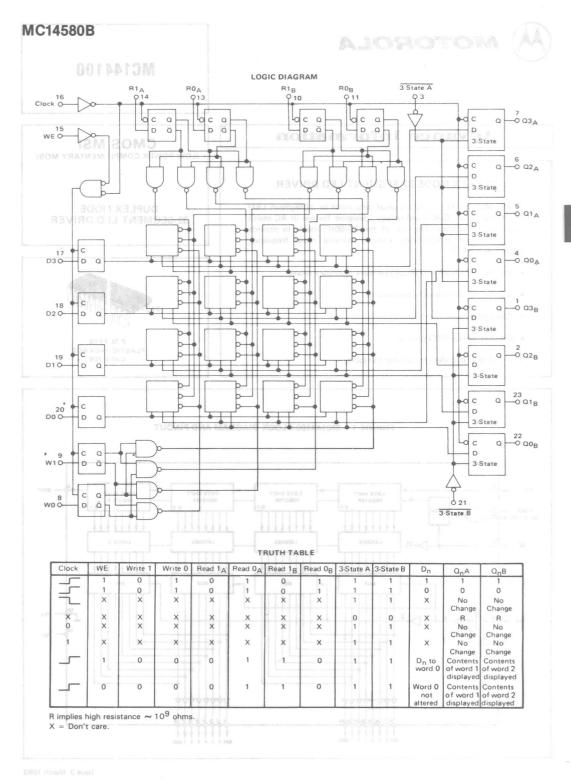
* The formulae given are for the typical characteristics only.

FIGURE 1 - OUTPUT DRIVE CURRENT TEST CIRCUIT



^{**} Measured at the point of 10% change at output when the output load is 1.0 Ω and 50 pF .







MC144100

#C145808

Advance Information

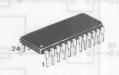
DUPLEX MODE 32-SEGMENT LED DRIVER

The MC144100 is a 32-bit serial data input to 32-segment LED driver realised in CMOS technology, designed for use in AC mains powered applications. The use of the 50/60Hz mains to provide the two phase multiplexing ensures minimal radio frequency interference (RFI).

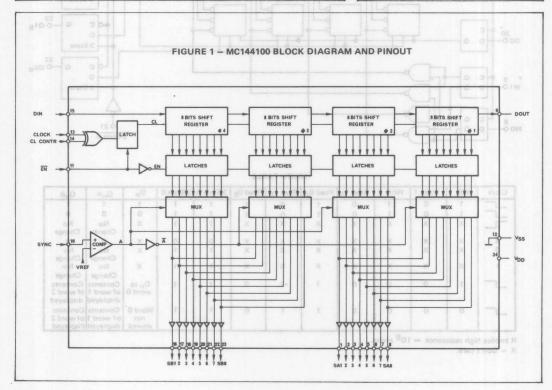
- · Minimal RFI from two phase sine wave multiplex driver
- Suitable for radio/clock applications
- Cascadable
- On-chip bipolar NPN drivers
- No on-chip decoder—for greater flexibility

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

DUPLEX MODE 32-SEGMENT LED DRIVER



P SUFFIX
PLASTIC PACKAGE
CASE 709



Issue 3 March 1983

2

MAXIMUM RATINGS (Voltages referred to VSS, pin.12) TARBEO TIUDEID

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to 6.5	V DC
Input Voltage, All Inputs	VIN	-0.5 to VDD + 0.5	V DC
DC Current Drain per Input Pin		are of med on.	mA
DC Current Drain per Output Pin	control s	ett li tudo 50 Mt	mA
Output Voltage, Segment Output	VSOFF	V _{SS} -6 to V _{DD} + 0.5	V DC
Operating Temperature Range	TA	0 to 70	C
Storage Temperature Range	TSTG	-65 to 150	С
ABLET			Terroic

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{\rm In}$ and $V_{\rm OUT}$ be constrained to the range $V_{\rm SS}$ ($V_{\rm in}$ or $V_{\rm OUT}$) $V_{\rm DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g. either $V_{\rm SS}$ or $V_{\rm DD}$).

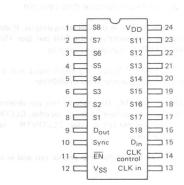
ELECTRICAL CHARACTERISTICS (TA = 0 to 70 C)

Characteristic	do Pin	888 188 888 Condition		//OMin	Max	Unit
Supply Voltage Supply Current	12, 24 outsmut 6	V _{IN} =0, I _{OUT} =0	VDD IDD	3.0 30 bag bath	6.0	V DC
Input Voltage High Input Voltage Low Input Current	15, 13 14, 11	V _{IN} = 0, I _{OUT} = 0 V _{IN} = 0 to V _{DD}	VIH VIL IIN	0.7 X VDD	0.3 X VDD	V DC V DC μA
Input Voltage High Input Voltage Low Input Current	10	VIN = 0 to VDD	VIHS VILS VINS	VDD - 0.5	V _{DD} - 2	V DC V DC μA
Output Drive Capability	9	VOL = 0.5V VOH = VDD - 0.5V	IOL IOH	200 -200	-	μA μA
Voltage Drop	1 to 8 16 to 23	IOUT = 30mA, VDD = 5V	VDD - VSOH VDD - VSOH	-	1.2 0.75 0.1	V DC V DC mA
Leakage Current Power Dissipation (on-chip)		VOUT = 0	PMAX	-	500	mW

SWITCHING CHARACTERISTICS (VDD = 5V + 10%, TA = 0 to 70°C)

Characteristic	Figure	Symbol	Min	Max	Unit
Clock High Time	2, 3	tCH	2	02 90	μs
Clock Low Time	2,3	tCL TO	2	M.A.S.	μs
Clock Rise Time	2,3	tCR	ent_to i	2	μs
Clock Fall Time	2,3	tCF	e day	2	μs
Enable Lead Time	2,3	tELead	200	197 XT9	ns
Enable Lag Time	2,3	t E Lag	200	-	nseer
Data Set-up Time	2,3	tDSup	200	TUD	ns
Data Hold Time	2, 3	tDHold	dida u	916	μs
Serial Data Out Delay	niverbas	TDOUT	naticum cted ada	eford	μs
Multiplexer Lead Time	4	tMLead	-	10	μs
Multiplexer Lag Time	4	tMLag	_	10	μs

PIN ASSIGNMENT



CIRCUIT OPERATION

The circuit operation can be followed by reference to the block diagram Figure 1.

Data are fed serially into the circuit via the data input pin DIN, which is controlled by the CLOCK and chip enable, \overline{EN} , pins—this latter enables the circuit when it is low i.e. at logical '0'. When \overline{EN} goes high, to logical '1', the clock idle state is stored in a latch; thus permitting the use of a positive or negative going clock.

Four 8-bit words are loaded into a 32-bit shift register, made up of four 8-bit registers, when $\overline{\text{EN}}$ is low. At the next rising edge of $\overline{\text{EN}}$ the data in the shift register are loaded into latches.

The shift in the register takes place on the falling edge of the clock when the clock control input, CLCONTR, is low, logical '0'. Conversely, when CLCONTR is high, logical '1', the shift takes place on the clock's rising edge. See Figures 2 and 3.

Word number 1 is the first shifted and number 4 the last.

The output DOUT serves as a cascading output.

Multiplexing is controlled by the SYNC input whose switching threshold occurs just before the LED segments are turned on. A current limiting resistor is necessary for this input if the control signal swings outside the limits of VDD + 0.5V to VSS - 0.5V.

The relationship between the SYNC input and the displayed word is shown in the table below:

TABLE 1

Segments	SYNC	Word
SA1 - SA8	low	1
SA1 - SA8	high	2
SB1 - SB8	low	3
SB1 - SB8	high	Citracterist

Because decoding is a function of an external circuit, for example the microprocessor in a radio synthesizer application, there is no decoding circuitry in this device.

INPUT/OUTPUT FUNCTIONS

DIN - (pin 15) This is the serial data input pin.

DOUT — (pin 9) This is the cascading output. If desired this pin can be tied directly to the DIN pin (pin 15) of a further MC144100 for cascading purposes.

CLOCK — (pin 13) This is the clock input and is able to accept a clock frequency of up to 250kHz.

CLCONTR = (pin 14) The state of this pin determines whether the data are shifted on the rising edge, CLCONTR = logical '1', or an the falling edge, CLCONTR = logical '0', of the clock signal.

EN - (pin 11) This is the chip enable pin and is active

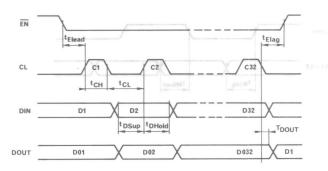
when low, logical '0'. When high it causes the clock idle state, at the time of the positive going transition, to be stored in a latch.

SYNC — (pin 10) The status of this input determines which of the four input words are displayed. See Table 1. If the control signal applied to this pin goes more positive than VDD + 0.5V or more negative than VSS — 0.5V an external current limiting resistor will be necessary.

OUTPUT DRIVERS - (pins 1 to 8 & 16 to 23) These are on-chip NPN emitter followers each requiring an external current limiting resistor. In the off state they are protected against voltages down to VSS - 6V.

FIGURE 2 - TIMING DIAGRAM - CL CONTR HIGH

a) POSITIVE CLOCK/RISING EDGE SHIFT (CL CONTR = H) / FALLING EDGE DOUT



b) NEGATIVE CLOCK/RISING EDGE SHIFT (CL CONTR = H) / FALLING EDGE DOUT

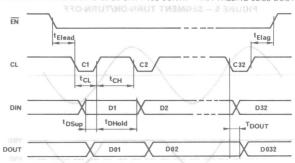
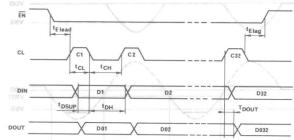


FIGURE 3 - TIMING DIAGRAM - CL CONTR LOW

a) POSITIVE CLOCK/FALLING EDGE SHIFT (CL CONTR = L) / RISING EDGE DOUT



b) NEGATIVE CLOCK/FALLING EDGE SHIFT (CL CONTR = L) / RISING EDGE DOUT

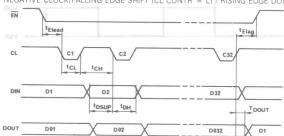
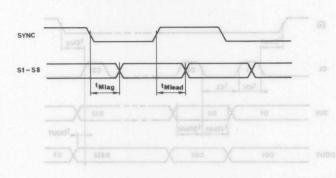
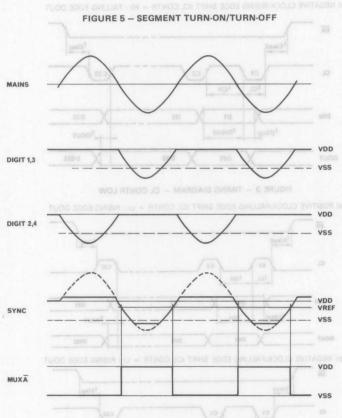
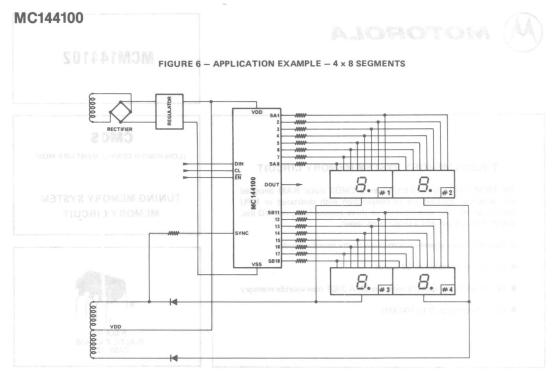
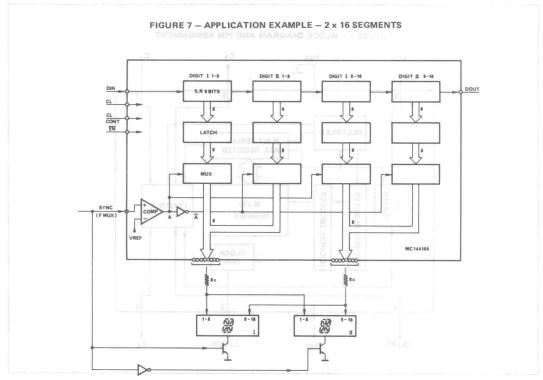


FIGURE 4 - SEGMENT CHANGE DELAY









MCM144102

UUIAAIJB

2

TUNING MEMORY SYSTEM MEMORY CIRCUIT

The MCM144102 is a 16-bit/16-word CMOS static RAM designed for consumer applications in conjunction with dedicated or MPU based systems. The chip consists of three control lines, one I/O pin, one chip enable pin and a single clock input.

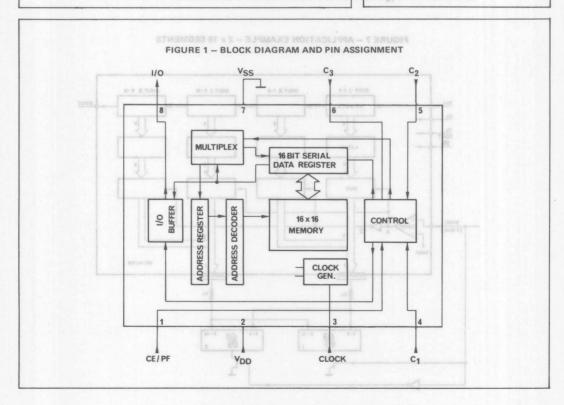
- Extremely low power consumption in the standby mode
- Directly expandable to 32 words
- Functionally compatible with the SMA 2001 non-volatile memory
- Clock frequency: 0 to 100 kHz

CMOS

(LOW-POWER COMPLEMENTARY MOS)

TUNING MEMORY SYSTEM MEMORY CIRCUIT





GURE 6 - APPLICATION EXAMPLE - 4 x 8 SEGMENTS

MAXIMUM RATINGS (Voltages referenced to V_{SS} , Pin 7.) + = 0.0 V , 0. 0.7 $\pm 0.0 \text{ V}$

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	7 to 0.5	Vdc
Input Voltage, All Inputs	Vin	V _{DD} +0.5 to -0.5	Vdc
DC Current Drain per Pin	JPS.	10	mAdc
Operating Temperature Range	TA	-40 to +70	≥°C
Storage Temperature Range	T _{stg}	- 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in})$ or $V_{out} \leqslant V_{DD}$.

ELECTRICAL CHARACTERISTICS

0	138	VDD	- 40	°C	2,	25°C		+7	Unit	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур	Max	Min	Max	Oiiit
Output Voltage										
V _{IN} = V _{DD} or OV "0" Level	VOL	5V	- Noole	0.05	or: 67, 6	0	0.05	_	0.05	Vdc
$V_{IN} = V_{DD}$ or OV "1" Level	V _{OH}	5V	4.95	NAZ-	4.95	5	nontries	4.95	th vitter of	Vdc
Input Voltage ''0'' Level	V _{IL}			(5	arn) Radit	ed thin so	capicitan	mbari is	ria) Yr dii Qi	Vdc
$(V_O = 4.0V \text{ or } 0.5V)$		4.5V	-	1.35V	-	-	1.35V	-	1.35V	
$(V_O = 4.5V \text{ or } 0.5V)$		5.0V	-	1.5V	-	-	1.5V	-	1.5V	
$(V_0 = 6.0V \text{ or } 0.5V)$		6.5V	T FUNC	1.95V	LNakk	-	1.95V		1.95V	
"1" Level	VIH	- year	ATS	driv	.abnow !	ld-31 .8	qu enora	neo yao	T30. 1/T	Vdc
$(V_0 = 0.5V \text{ or } 4.0V)$		4.5V	3.15	-nois	3.15	1	d-E-s y	3.15	таки на	const
$(V_0 = 0.5V \text{ or } 4.5V)$	tiue of	5.0V	3.50	-	3.50	se it ee	nich_may	3.50	itrail <u>o</u> de n	s and a
$(V_0 = 0.5V \text{ or } 6.0V)$		6.5V	4.55	-boir	4.55	91 10 10	l b o tnes	4.55	iour a ni	REAG
Input Current (all inputs)	nd of bes	retions n	nzeni	-	01-01-11-0	incol Inti	req inc		Text	(DS) 1)
Low of TUO AT VIN = OV	ns, atteep	6.5V	1124	-1	of bern	-	-1	n/To	-1	μAdc
high impedance state. High	e of Heave	6.5V	gru <u>o</u>	1 giris	ed to n		ed 1or at	sb Trit da	1	μAdc
Output Current.	-			Vital	metric suces	are data	bear read	rit gnati ritani w	Cl 20d B	the vi
MSTRUCTION CODES(O/I stad)	- 1 318	AT							VICTOR	mism s
$V_{OH} = V_{DD} - 0.8V$ Source	^I ОН	-	- 2	- orit	-1.4 OA 38	to seray	ni adt v	-1		mAdc
VOL = 0.8V Sink	loL	02_03	102		1.4			nger j an	no zi n	mAdc
Tri-state output				the	ata in to	ths the r	ris , boins	u Joola	umi ioi	no) mage
(Data I/O Leakage Current)	Standby	1 1	0				OLA BULB	nem erb	en es abb	U9109
$V_{OT} = V_{DD}$	TH	0 - 1	0-				nil1,dpp	9VH 06	2. 1	μAdc
V _{OT} = 0V 0 toO a		7= 1	0_	- 1	irbed by ine. =		vernau _{tals} t mat	stra y id pis To	ment to	μAdc
Quiescent Current	No Cond	0 0	1	lsub	en this	lw. yinC	- 3.18.	ID ENV	FAILUS	Haws
Operating	IDDOP	5V	-	50	ched, A.	lise girl: monition	50	, f = ,dg wo⊤gni	350	μAdc
Standby	IDDSTB	1.2V	_		transfer	arsh au		enibiovi	80	μAdc

Parameter	Pin	Symbol	Min	Тур	Max	Unit	90
Clock Frequency (f _{CL} = 1/t _{CL})	3(1)	fCL	olaV	ā.0-	100	kHz	agns8 a
Clock Hold Time High	957 pl	t _{CLH}	4×	0.5 to	20	μs	amqui
Low .ogv>	hov.	tCLL	4	0.5		μs	
Clock Rise and Fall Time		^t CLF	slaArm		1	μs	per Pin
Write Time (per word)		^t WRITE	1 clock cycle	+70	os 0A—	AT	iture Ronge
Read Time (per word)		^t READ	1 clock cycle	+ 150	ot 88 -	gaz Y	ua Range
Data Out Delay	-8(3)	t ₁ (2)	50n		3	μs	HARACTERIST
Data In Set Up Time	25°C	t ₂	2		T	μs	
Instruction Set up Lead	4,5,6(1)	t ₃	2	and the same	eev .	μs	nistic
Lag	Typ	t ₄	50	Min		ns	

NOTES :

- The maximum pin capacitance is 10pF to VSS for : C1, C2, C3 and clock
- t₁ applies only during data transition as the data format is NRZ
- The output external loading capacitance will be 10pF (max)

INPUT/OUTPUT FUNCTIONS

READ — The memory can store up 16, 16-bit words, with all functions controlled by a 3-bit parallel instruction bus and an applied clock, which may be free running.

A READ instruction, presented for one clock period moves data from memory and parallel loads it in to the shift register.

A SERIAL DATA OUT instruction, presented for 16 clock pulses, causes the data to be moved out of the chip on the I/O bus. During this time the data are internally recirculated to allow further read out without accessing the memory array.

WRITE — This is basically the inverse of READ. The address can be changed and data serially loaded in to the chip over 16 clock cycles. The WRITE instruction, presented for one clock period, shifts the data in to the selected address in the memory array.

CLOCK — This is active high. In all modes, other than WRITE, the memory array remains undisturbed by the presence, or absence, of signals on the clock line.

POWER FAIL/CHIP ENABLE — Only when this dual purpose pin is high, = 1, is the chip selected. At all other times, including low power conditions, the memory is disabled thus avoiding erroneous data transfer and excessive drain on the standby battery due to intermediate levels on the inputs.

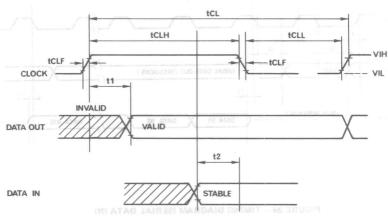
STANDBY — When this instruction is received the memory goes in to a quiescent state, when only a 1.2V battery is necessary to supply the device's modest power requirements.

INSTRUCTION SEQUENCES — The READ and WRITE instructions need to be presented for one clock cycle only. All instructions, except SERIAL DATA OUT, force the output data driver to a high impedance state.

TABLE 1 - INSTRUCTION CODES

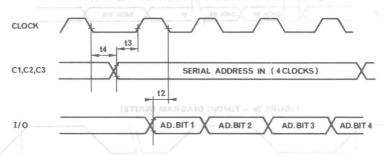
C1	C2	C3	INSTRUCTION	CLOCK	FREQUENCY
				MIN	MAX
1	1	1	Standby	0	100kHz
0	0.	1	No operation	- again	_
0	1	0	Write	0	100kHz
0	1	_1	Serial Data Out	0	100kHz
0	0	0	No Operation		
1	0	0	Serial Address In	0	100kHz
1	0	_1	Serial Data In	0	100kHz
1	1	0	Read	0	100kHz
			1 = high 0 = low		

FIGURE 2a - TIMING DIAGRAM (GENERAL)



Note: Figure 2A defines VH and VL levels for all figures

FIGURE 2b - TIMING DIAGRAM (SERIAL ADDRESS IN)



DATA IN



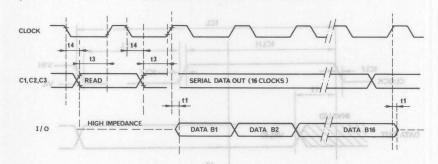


FIGURE 2d - TIMING DIAGRAM (SERIAL DATA IN)

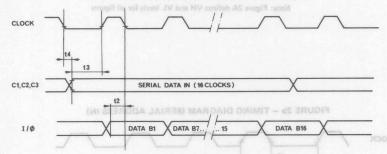
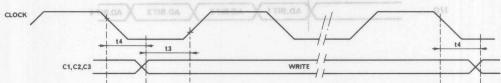


FIGURE 2e - TIMING DIAGRAM (WRITE)





MC144104

Product Preview

OWLEDWER COME EMENTARY MOS

INFRARED REMOTE

HIGH PERFORMANCE INFRARED REMOTE CONTROL TRANSMITTER

- Delta Modulated FSK Coding
- Error Protected Codes
- 12-Bit Data Word plus Parity Bit
- 1024 Commands (64 × 16)
- Option Pin for Expansion to 4096 Commands (64 × 64)
- Simple Infrared LED Driving Circuit
- Local Data out Pin
- Very Low Duty Cycle (typ 0.33%)
- 4-10 V Supply
- Ideal Transmitter for MC144124 Receiver
- Protected against Multiple Key Operation Malfunction

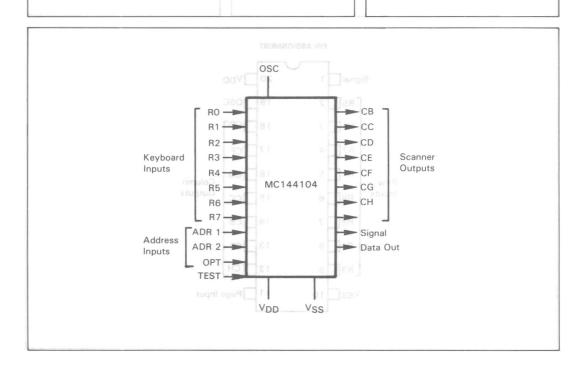
CMOS

(LOW-POWER COMPLEMENTARY MOS)

HIGH PERFORMANCE REMOTE CONTROL TRANSMITTER

Brown American Berne and attar Each Standard Control of the Contro

P SUFFIX
PLASTIC PACKAGE
CASE 709



MOTOROL

Product Pr

Product Preview

INFRARED REMOTE CONTROL TRANSMITTER

- Biphase AM Coding
- 9-Bit Data Word
- 8 Pages of 64 Commands
- EOT Word Sent before and after Each Command
- Protected against Multiple Key Operation Malfunction
- · LC or Ceramic Oscillator
- Low Standby Current
- Low Duty Cycle
- 4-10 V Supply
- Ideal Transmitter for MC144122 Receiver
- Simple Infrared LED Driving CKT

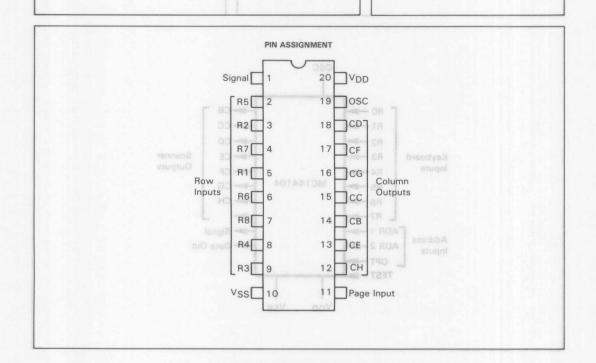
CMOS

(LOW-POWER COMPLEMENTARY MOS)

INFRARED REMOTE CONTROL TRANSMITTER

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P SUFFIX
PLASTIC PACKAGE
CASE 738





 $\text{(5)}^{\circ} \text{ as } = \text{(5)}^{\circ} \text{ (144110/1} \text{ (15)}^{\circ} \text{ (25)}^{\circ} \text{ (25)}^$

QUAD & HEX D/A CONVERTERS

The MC 144110 and MC 144111 are hex and quad static, D/A converters realised in CMOS technology. Each converter, featuring 6-bit resolution, consists of a 6-bit shift register, 6-bit latch and a static D/A converter.

- 4/6 direct R-2R network outputs
- 4/6 emitter follower outputs
- MPU compatible input levels
- Serial data input
- Data cascade output
- Wide operating voltage range of 4.5 to 15 Vdc

CMOS

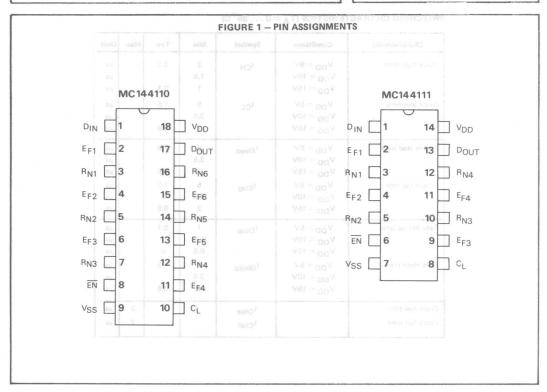
QUAD & HEX D/A CONVERTERS



MC144110 P SUFFIX PLASTIC PACKAGE **CASE 707**



P SUFFIX PLASTIC PACKAGE CASE 646



Issue 4 July 1981

The MC 144110 and MC 144111 are hex and quad static, D/A



MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	+ 18 to — 0.5	Vdc
Input Voltage, All Inputs	Vin	- 0.5 to V _{DD} + 0.5	Vdc
Input Current, All Inputs	lin	10	mAdc
Operating Temperature Range	TA	0 to +85	°c
Storage Temperature Range	T _{stq}	- 65 to + 150	°c

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any mode. And places voltage higher than maximum rated voltages to this high impedance circuit. For proper operation

it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. · 4/6 emitter follower outputs

SWITCHING CHARACTERISTICS (TA = 0 . . . 85 °C)

Characteristics	Conditions	Symbol	Min	Тур	Max	Unit
Clock high time	V _{DD} = 5V	^t CH	2	0.2		μs
	$V_{DD} = 10V$		1.5			μs
WC144141	$V_{DD} = 15V$		1	0.1	NC 14	μs
Clock low time	$V_{DD} = 5V$	tCL	5	1.5		μs
	$V_{DD} = 10V$		3.5		1	μs
PIN T 14	$V_{DD} = 15V$		-02V	0.5		μs
Enable lead time	V _{DD} = 5V	[†] Elead	50	1.5	1	μs
	$V_{DD} = 10V$		3.5	1		μs
12 12 12	$V_{DD} = 15V$		2	0.5	1 4	μs
Enable lag time	$V_{DD} = 5V$	t _{Elag}	5	1.5		μs
F2 4 11	V _{DD} = 10V	Liag	3.5	15	3	μs
05 2	$V_{DD} = 15V$		2	0.5	1	μs
Data Set-up time	V _{DD} = 5V	t _{Dsup}	1	0.1		μs
e a 7	$V_{DD} = 10V$		0.75	Ter	1	μs
	$V_{DD} = 15V$		0.5	0		μs
Data Hold time	$V_{DD} = 5V$	^t Dhold	5	1.5	1	μs
	$V_{DD} = 10V$	2,1010	3.5			μs
	$V_{DD} = 15V$		2	0.5	1 8	μs
Clock rise time		[†] Crise	Jo [10	2	μs
Clock fall time		^t Cfall		1	2	μs

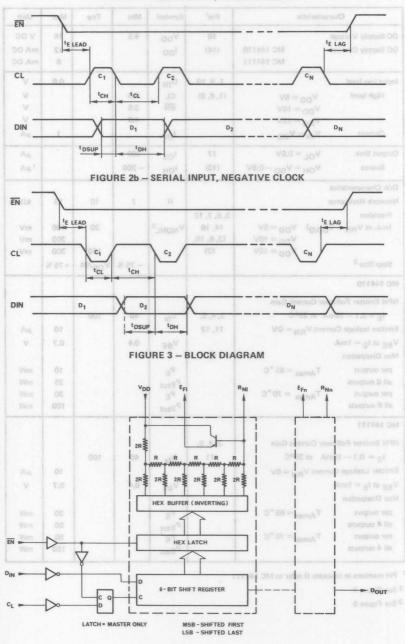
ELECTRICAL CHARACTERISTICS (T_A = 0 - 85 °C, V_{DD} = 4.5 - 15V)

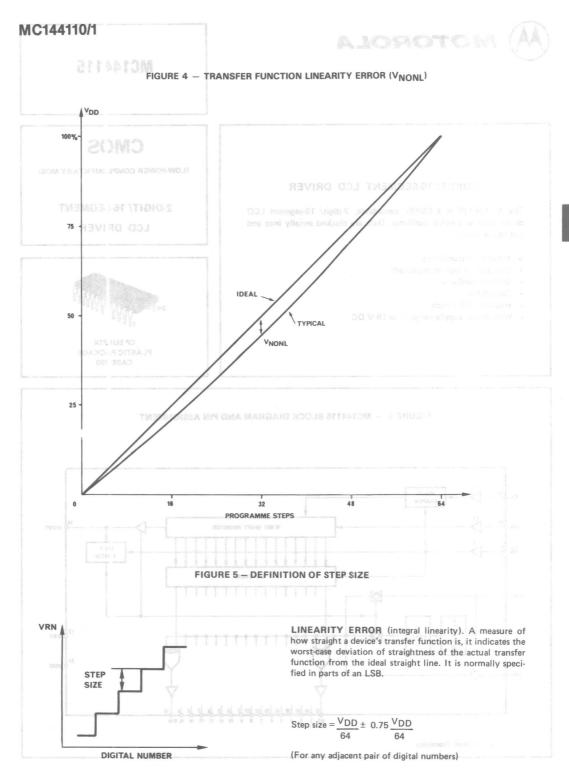
Characteristic		Pin ¹	Symbol	Min	Тур	Max	Unit
	144110 144111	18 (14)	V _{DD}	4.5	GA2.	15 12 8	V DC mA DC mA DC
Input low level		1, 8, 10	D _{IN}	/	01	0.8	_ v
High level $V_{DD} = 5V$ $V_{DD} = 10V$		(1, 6, 8)	CL EN	3.5	10,		V
$V_{DD} = 15V$ Current $V_{IN} = V_{DD}$			IN	4.0	_X	11	μΑ
Output Sink $V_{OL} = 0.5V$ Source $V_{OH} = V_{DD}$	- 0.5V	17 (13)	I _{OL}	200 200	1000		μA ³ μA
D/A Characteristics	SVIII	21.0421	78114-52		11213		
Network Resistance Precision		3, 5, 7, 12	R	7	10	15	kΩ
(w.c. at $V_{RN} = V_{DD/2}$) $V_{DD} = V_{DD} = V_{DD}$	5V	14, 16 (3, 5, 10,	V _{NONL} 2		20	100 200	mV mV
Step Size ³	15V	12)	4	- 75 %	120 V _{DD} /64	300 +75 %	mV
MC 144110							
NPN Emitter Follower Current Gain	+			V	147		1515
I _E = 0.1 - 10mA at 25°C		2, 4, 6,	h _{fe}	40	100		
Emitter leakage Current $V_{RN} = OV$		11, 13	HQ1	shad,		10	μA
V_{BE} at $I_{E} = 1mA$ Max Dissipation	MARON	IG 1500.II	V _{BE} - € ∃RI	0.4 FIGU		0.7	V
per output T _{Amax} = 85 °	c		PE			10	mW
all 6 outputs	31.0		PEtot	no V		25	mW
per output $T_{Amax} = 70$ all 6 outputs	°C		P _E P _{Etot}	4/4		30 100	mW mW
MC 144111	4			-6			
NPN Emitter Follower Current Gain	1 ++	2, 4, 9,		E115			
I _E = 0.1 - 10mA at 25°C		s11 s	h _{fe}	40	100		
Emitter Leakage Current $V_{RN} = 0V$ V_{BE} at $I_E = 1mA$	100	Ent Ent	V _{BE}	0.4		10 0.7	μA V
Max Dissipation			reveius x				
per output T _{Amax} = 85 °	c		PE			20	mW
all 4 outputs			PEtot			50	mW
per output $T_{Amax} = 70^{\circ}$ all 4 outputs	,c		P _E		1	50 150	mW mW

¹ Pin numbers in brackets () refer to MC 144111

² See Figure 4

³ See Figure 5





MC144115

IC144110/1

2

2-DIGIT/ 16-SEGMENT LCD DRIVER

RE 4 - TRANSFER PUNCTION LINEARITY ERROR (VNONL)

The MC144115 is a CMOS, cascadable, 2-digit/ 16-segment LCD driver with an on-chip oscillator. Data are clocked serially into and out of the circuit.

- Input level translators
- · Direct drive (not multiplexed)
- On-chip oscillator
- Cascadable
- Internal 16-bit latch
- Wide power supply range, 3 to 18 V DC

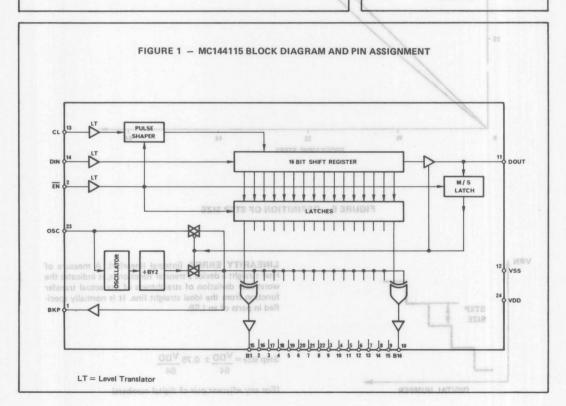
CMOS

(LOW-POWER COMPLEMENTARY MOS)

2-DIGIT/ 16-SEGMENT LCD DRIVER



CP SUFFIX
PLASTIC PACKAGE
CASE 709



MC144115

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	18 to -0.5	Vdc
Input Voltage, All Inputs	Vin	V _{DD} + 0.5 to V _{SS} -0.5	Vdc
Input Current, All Pins - 8	431in	V8 = 00V	mAdo
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	IOT _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended, that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$.

-out $\sim vDD$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either Vss or VDD).

ELECTRICAL CHARACTERISTICS

-	4%			VDD	vor-40	o°c	25	°C	85 °C		Unit
G	naracteristic	00	Symbol	Vdc	Min	Max	Min	Max	Min	Max	Unit
Segment Outpu (pins 3, 410,	t Drive Current 15, 16, 22)	90		16191	A01 = 0	gV gv			m7 063 9	GEA 1	
Source	VOH = 4.6Vdc		IoH	5	220	gV_	160	_	120	_	μAdc
	VOH = 9.5Vdc			10	525	gV _	370	- 88	280	8760	,
	VOH = 13.5Vdc			15	1900	ciV-	1300	_	1000	_	
Sink	VOL = 0.4Vdc		loL	5	330	av_	240		190		
SINK	VOL = 0.4Vdc VOL = 0.5Vdc		IOL	10	880	6V =	600		470	_	
	VOL = 1.5Vdc			15	3100	0V -	2100	-	1600	STREET	
Source Current	pin 1 an -	00			V81 = E	σV					
	VOH = 4.6 Vdc		loH	5	690	_ 109	500	- 1	390	Doct.	μAdo
	VOH = 9.5Vdc			10	1620		1140	_	870	(cop)	
	VOH = 1.3Vdc			15	5880	a -	4000	- J J- ,emi	3100	nilė	
Source Current	pin 11	No.									
Chip Enabled	VOH = 4.6Vdc		loH	barlatel e	29	of to sure	21	erasm orbi	16	1001	μAdc
(Slave chip	VOH = 9.5Vdc		IOH	10	70	_	40	_	30	_	μAuc
only)	VOH = 13.5Vdc		N/A	19 15 0	250	- S 38	175	_	135		
311147	VOH = 13.5Vdc			15	250	3100	-		-	1670	
			IoH	5	aithea Cla	3100	4.5	2160			
Chip disabled	VOH = 0Vdc		IOH		6			-	3.8	-	μAdd
				10	28	-	20	-	16	- 13	
	-	A-11-12-16-7		15	58		40		31	-	
Sink Current fo	or pins							GA:			
1 and 11	VOL = 0.4V		loL	5	590	_	430		340	-	μAdo
	VOL = 0.5V		1	10	1570	/=\	1100	W 10	840	- 37	
	VOL = 1.5V	ИЭ	-	15	5550	13	3850	13	2900	-	
Pin 23 Input Co	ırrent					-	H07	1011			
(Master chip on			lin	- 5	3.4	15	2.6	-11	2.1	9	μAdd
Sink (Vin = VI	DD) or	X		10	22	70	15	50	12	40	
Source (Vin =	VSS)			15	50	150	35	110	25	85	
nput Voltage			VIL	5 to 15	-	0.8	-	0.8	_	0.8	Vdc
oins 2, 13, 14			VIH	5 x100	3 3	(cl) -	3	-	3	-	
				10	3.5	-	3.5	_	3.5	_	
				15	4.0	_	4.0	_	4.0	-41	
Quiscent currer	nt parsi		Iss	5	_	150	_	20		150	μAdo
	100.32			10	-	300	-	40	_	300	
	-		,	15	_	600	_	80	-	600	
Tristate Output						1					
Leakage Currer pins 11, 23	t		İTL	15	-	± 1.6	701	± 1.6	_	± 12	μAdc
Input Current Except pins 11	and 23	p(0	lin	15	-	± 0.3	yd=)	± 0.3	a =	± 1.0	μAdo
Input Capacita			Cin	_		1103	muso 1	7.5		-	pF

Characteristic	Condition	Symbol	Min	Max	Unit
Clock High Time	VDD = 5V	tCh	5	-	μs
	VDD = 10V	AT I	4		μs
	VDD = 15V		2	-	μs
Clock Low Time	VDD = 5V	tCI	5	-	μs
-loon is ssy	VDD = 10V	-	4	-	μs
	VDD = 15V		201	rainas	μѕ
Enable Lead Time	VDD = 5V	tElead	2	-	μs
	VDD = 10V	ggv I	1	-	μs
Min Max Min Ma	VDD = 15V	abV Mo	500	-	ns
Enable Lag Time	VDD = 5V	tElag	500	-	ns
	VDD = 10V		300	- 80	ns
120 - 120	VDD = 15V	20 10	200	absi	ns
Data Set-up Time	VDD = 5V	tDsup	500	- bb\v	ns
	VDD = 10V	16	300	±V≥	ns
240 - 190 -	VDD = 15V	8 4	200	-sb\	ns
Data Hold Time	VDD = 5V	tDhold	2	7997	μs
	VDD = 10V	91	1	00%	μs
	VDD = 15V		500	-	ns
Clock Rise Time	10% to 90%	tCrise	51 -	200	μѕ
Clock Fall Time - CAPT	of VDD	tCfall	-	2	μs
Min. EN High Time, CL = 50pF*	5 to 15V	tEnh	50	_dbV	μs

* Min. time for the master/slave status of the chip to be latched in.



(a) Positive Clock EN TELEAD LELAG CL c, t CL t CH DIN D1 D2 t DSUP ^tDH (b) Negative Clock EN TELEAD ELAG C1 C2 CL t CL t CH DIN D1 D2 t DSUP 1DH

2

CIRCUIT OPERATION

The circuit operation can be followed by referring to the block diagram, Figure 1.

Data are entered serially into the circuit's 16-bit shift register via the DIN pin. The data transfer rate is controlled by the clock input, CL, either positive or negative clock pulses may be used, see Figure 2.

The CL input is enabled only when the \overline{EN} input is in the low state, logical '0'. On the positive going edge of \overline{EN} data in the shift register are latched and transferred to the display drivers.

If more than two digits are to be displayed two, or more, circuits can be simply cascaded, as shown in Figure

Level translators are provided on inputs CL, DIN and EN to allow the circuit to interface directly with a 5V powered controller, regardless of the circuit's own power supply voltage—which can lie anywhere in the range 3 V to 18 V.

LCD DRIVE

AC drive for the LCDs is provided by an on-chip, 50% duty cycle oscillator whose frequency is determined by a single external capacitor, see Figure 4.

A segment output is in phase with the backplane when the corresponding data bit in the shift register is low, logical '0'. The segment is in anti-phase when the corresponding data bit is high, logical '1'.

CASCADING

When MC144115s are cascaded, that which controls the backplane frequency, called the master, is the last circuit in the shift register chain, see Figure 3.

The master's BKP output is connected directly to the slaves' OSC inputs. The slaves' oscillator circuits are bypassed and their backplane frequency is controlled by the OSC input.

DOUT acts an input/output. When \overline{EN} is high it acts as an input and when \overline{EN} is low DOUT acts as an output. While the chip is disabled, \overline{EN} at logical '1', an internal resistive pull-up pulls the slaves' DOUT pin high, to logical '1'. A falling edge on \overline{EN} latches-in the logic state of DOUT which defines the master/slave status of each IC.

During the EN low time DOUT acts as an output; the internal pull-up is inactive and an output buffer is enabled (standard push-pull buffer in the slave mode, open drain N channel buffer in the master mode).

It is recommended that in a cascaded configuration the EN input is held high during power-up to avoid any chance of the circuit whose DOUT pin is grounded trying to act as a slave and drawing current through its P channel buffer transistor. This transistor is designed to limit the short circuit current to 3mA with a 15V supply.

INPUT/OUTPUT FUNCTIONS

CL - (pin 13) This is the clock input.

DIN - (pin 14) This is the serial data input pin.

EN — (pin 2) This is the chip enable pin and is active when low, logical '0'. On its positive going edge it causes the contents of the shift register to be loaded into the latches and transferred to the display drivers. When it is high it causes DOUT to act as an input and when low as an output.

BKP - (pin 1) This is the backplane driver output.

DOUT — (pin 11) This is the serial data output pin and is also used to determine the master/slave status of

the circuit.

In a master configuration the pin is tied to ground thus enabling the oscillator and disabling the push-pull data output buffer. In the slave configuration DOUT is tied to DIN of the following device, the oscillator is bypassed and the output buffer is enabled.

OSC — (pin 23) This pin, in the master role, needs an external frequency determining capacitor to ground, see Figure 3. In the slave role the oscillator circuitry is bypassed and the pin serves as the input for the backplane frequency.

B1 to B16 — (pins 3 to 10 and 15 to 22) These are the segment output drivers.

FIGURE 3 - Cascading MC144115s

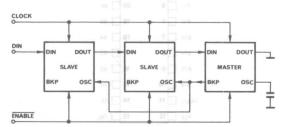
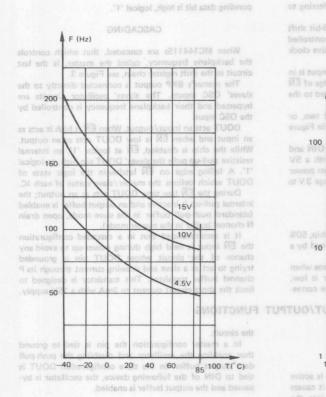
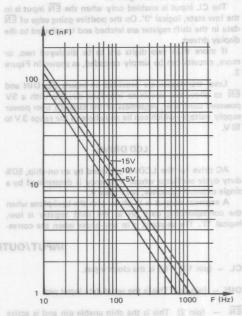


FIGURE 4 - BACKPLANE FREQUENCY



the block diagram, Figure 1.

Data are entered serially into the circuit's 16-bit shift register via the DIN pin. The data trensfer rate is controlled by the clock input, CL, either positive or negative clock puters may be used, see Figure 2.



when low, logical '0'. On its positive going edge it causes the contents of the shift register to be loaded into the latches and transferred to the display drivers. When it is

PIN ASSIGNMENT -yd al yellumia not, as a Function of Temperature | .C. e as a Function of Capacitor Value Tugillo na analysised and not sugar a (10nF capacitor), and bus beauti (18°C) DOUT - (pie 11) Tois is the serial data puzzo 25 2 A B16 - (pins 3 to 10 and 15 to 22) These are the B9 3 22 B8 B10 4 21 B7 B11 5 20 B6 19 B5 B12 6 B13 7 18 B4 814 8 17 B3 B15 9 16 B2 B16 10 15 B1 DOUT 11 14 CL

13 DIN

2

VSS 12



MC144117

ACTAGES!



CMOS LSI

(LOW POWER COMPLEMENTARY MOS).

4-DIGIT DUPLEX LCD DECODER/DRIVER

4 DIGIT DUPLEX LCD DECODER/DRIVER

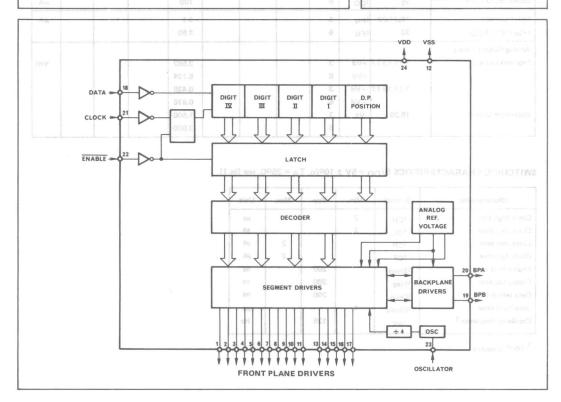
The MC144117 is a CMOS 4 digit duplex LCD decoder/driver with on-chip oscillator. Data is entered serially, latched and decoded for LCD front and back planes.

Min.

- On-chip oscillator
- · On-chip analog reference voltages
- . Compatible with MC 14499 LED driver
- Supply voltage range 3V to 6V DC
- MPU compatible



CP SUFFIX
PLASTIC PACKAGE
CASE 709





MAXIMUM RATINGS (Voltages referenced to VSS, pin 12)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	VDD	6 to - 0,5	Vdc
Input Voltage, all Inputs	Vin	V _{DD} + 0,5 to V _{SS} - 0,5	Vdc
DC Current Drain per Pin		10	mAdd
Operating Temperature Range	TA	-40 to+85	oC.
Storage Temperature Range	T _{stg}	-65 to+150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < (Vin or Vout) < VDD.

ELECTRICAL CHARACTERISTICS

		-3		TA = -	40°C	TA = 2	20C	planes.	TA = 85	OC OT	LOI
Characteristic	Pin	Symbol	V _{DD}	Min.	Max.	Min.	Тур	Max,	Min.	Max.	Unit
DC Supply Voltage	24	V _{DD}	-	3	6	3		6	103	6	Vdc
Input Voltages							tages		en galan		3 0
'O' Level	18,21	VIL	3		0.9	191	LED dri	0.9	d drive of	0.9	Vdc
	22		6		1.8		DO VI	1.8	ten egs/l	1.8	8 .
'I' Level XIRAUS 93		VIH	3	2.1		2.1			2.1	mop U9	M e
ASTIC PACKAGE			6	4.2		4.2			4.2		
Quiescent Current	24	IDD	6				100				μА
Input Current	18,21,22	IFN	6				±1				μА
(Vin = 0 to VDD)	23	IFN	6				±50				
Analog Output Levels	d day										
Segment Drivers	1-11,13-17	+Vd	3		-		2.562				Vdc
		+Vd	6				5.124				
	1-11,13-17	-Vd	3				0.438	-05/-	PAL ATA	d	
		-Vd	6	TIĐICI	TIDIO	DIGIT	0.876	-			
Backplane Drivers	19,20	Vc	3				1.500	-00	50-w X30	ua	
			6				3.000	- 4			

SWITCHING CHARACTERISTICS (VDD = 5V ± 10°/o, TA = 25°C, see fig.1)

Characteristic	Symbol	Min.	Тур	Max.	Unit	F
Clock high time	tCH	2	RE	20030	μs	1
Clock low time	tCL	2	-		μs	1
Clock rise time	tCR	-		2	μs	П
Clock fall time	tCF	11	14	2	μs	
Enable lead time	tElead	1-1	200	×	ns	F
Enable lag time	Liay	1.0	200	HI THEMOT	ns	
Data set-up time	tDsup		200	10/2002	ns	
Data hold time	tDhold	1	-	TITE	μѕ	1
Oscillator frequency 1	fosc		125		Hz	ı

^{1 10}nF capacitor

* * * * * * * * * * * * * * * * *

MOLTASIMA CIRCUIT OPERATION - 8 3RUSIS

The circuit accepts a 20-bit input, 16 bits for the 4-digit display plus 4 bits for the decimal point. These latter 4 bits are optional.

The input sequence is the decimal point followed by the 4 digits, as shown in figure 2. In order to enter the data the enable, $\overline{\text{EN}}$ must be low (=0). The sample and the shift are accomplished on the falling clock edge, see fig. 1. Data is loaded from the shift register to the latches when $\overline{\text{EN}}$ goes high (=1). While the shift register is being loaded, the previous data is stored in the latch. Figure 5 shows the decoding used by the device. If the decimal point is used, the system requires 20 clock pulses to load data, otherwise only 16 are required. Inputs CL, DIN and $\overline{\text{EN}}$ will allow the circuit to interface directly with a 5V powered controller, regardless of the circuits own power supply voltage which can lie anywhere in the range 3V to 6V.

The backplane drive signals from BPA and BPB are orthogonal 3-level amplitude signals, as shown in fig. 4. Only one backplane can be at $V_{\mbox{\scriptsize DD}}$ or $V_{\mbox{\scriptsize SS}}$ when the other backplane is at $V_{\mbox{\scriptsize DD}/2}$. In this way, a segment driver (front plane) which is connected to two segments — one on each backplane — can be arranged to select only one (or any combination) of the segments attached to the driver. Each segment driver has a square wave output centered about 0.5 $V_{\mbox{\scriptsize DD}}$. Since each driver has two segments associated with it (one for backplane A and one for backplane B), there are 4 possible operating conditions, as follows:

LCD DRIVE

The device pinout has been organised to ease the interconnection to the LCD display. The LCD digit organisation is given in fig. 3.

SEG. A	SEG. B
on	on
on	off
off	on
off	off

These conditions are obtained by changing the phase relationship between the segment driver and backplane drivers, as shown in the figures 6 to 9.

FIGURE 1 - TIMING DIAGRAM

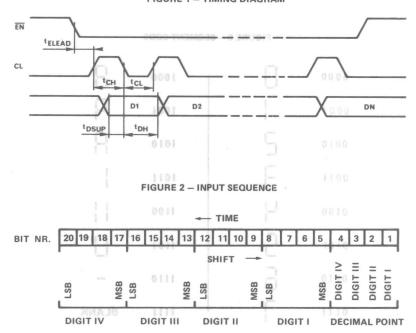
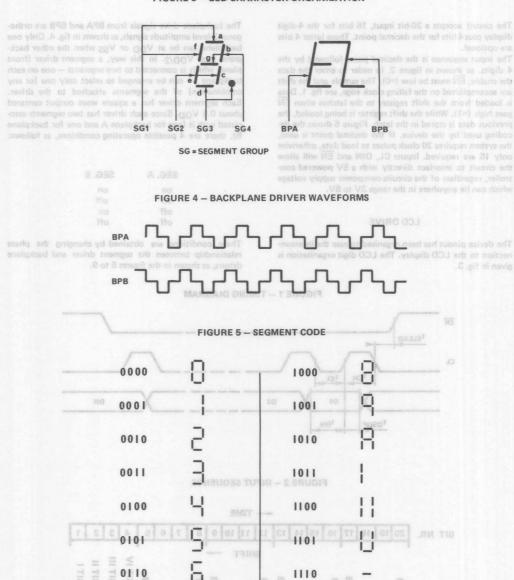


FIGURE 3 - LCD CHARACTER ORGANIZATION



DECIMAL POINT

Ш

FIGURE 6 - SEGMENT DRIVE VOLTAGE

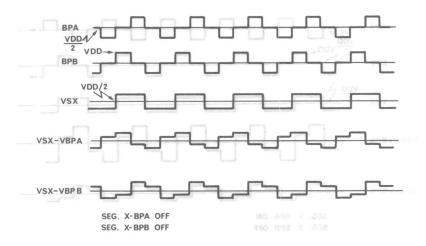
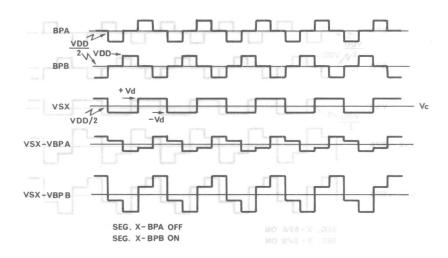


FIGURE 7 - SEGMENT DRIVE VOLTAGE



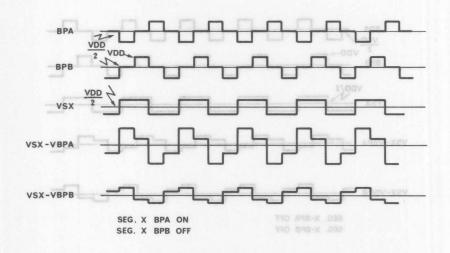
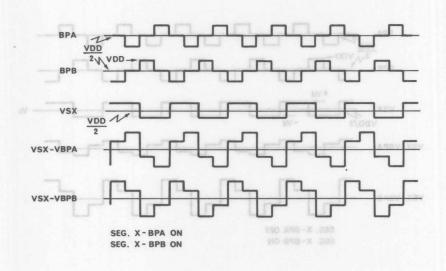


FIGURE 9 - SEGMENT DRIVE VOLTAGE



71144117 WC1441122

D1SG1

D1SG3

D1SG4

D2SG1

D2SG2

D2SG3 D2SG4

D3SG1 9

D3SG2 10

D3SG3

VSS

11

12

DISG2 2 PARTIAL

CONTRO



PIN DESCRIPTION

24 VDD

23 OSC

22 EN

21 CL

20 BPA

19 BPB

18 DIN

17 D4SG4

16 D4SG3

15 D4SG2

14 D4SG1

13 D3SG4

D1SG1 — D1SG4 (Pins 1 to 4) — Front Plane Drivers for Digit 1, Segment Groups 1 to 4

D2SG1 - D2SG4 (Pins 5 to 8) - Front Plane Drivers for Digit 2, Segment Groups 1 to 4

D3SG1 — D3SG4 (Pins 9-10, 13) — Front Plane Drivers for Digit 3, Segment Groups 1 to 4

D4SG1 — D4SG4 (Pins 14 to 17) — Front Plane Drivers for Digit 4, Segment Groups 1 to 4

VSS (Pin 12) - Most Negative Supply

DIN (Pin 18) - Serial Data Input

BPB (Pin 19) - Backplane B Driver Output

BPA (Pin 20) - Backplane A Driver Output

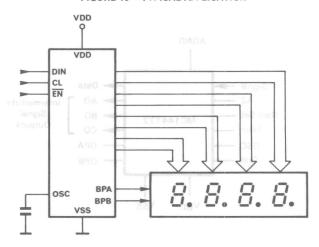
CL (Pin 21) - Clock Input, Active Negative going edge

EN (Pin 22) — Chip Enable Pin, when low, logical 'O' CL Input is active on the positive going edge.
The contents of the shift register are loaded into the latches and transferred to the display drivers.

OSC (Pin 23) — The oscillator pin requires an external frequency determining capacitor to VSS.

VDD (Pin 24) - Most Positive Supply

FIGURE 10 - TYPICAL APPLICATION



PIN DESCRIPTION

MC144122

NC144117

D1SG1 - D1SG4 (Pins 1 to 4) - Front Plane Drivers for Digit 1, Segment Groups 1 to 4

Product Preview

for Digit 3, Segment Groups 1 to 4 .

D4861 - D4864 (Pins 14 to 17) - Front Plane Drivers

INFRARED REMOTE CONTROL RECEIVER

- Preamp/Detector for AM Infrared Signals
- Digital Signal Output
- Coil-less Input Circuit for High Noise Immunity
- Programmable On-chip Bandpass Filtering
- Minimal External Components
- Single 10 V Supply

Input is active on the positive going edge.
The contents of the shift register are loaded into the latitudes and transferred to the display drivers.

CSC (Pin 23) - The oscillator pin requires an external frequency determining capacitor to VSS.

VDD (Pin 24) - Most Positive Supply

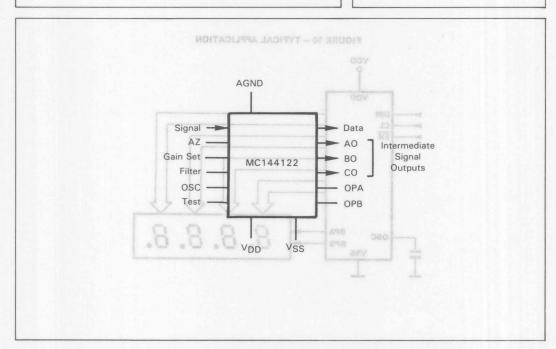
CMOS

(LOW-POWER COMPLEMENTARY MOS)

INFRARED REMOTE CONTROL RECEIVER

P SUFFIX

P SUFFIX
PLASTIC PACKAGE
CASE 648



2

MOTOROL



Product Preview

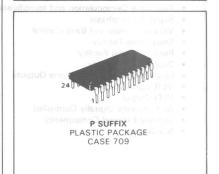
HIGH PERFORMANCE REMOTE CONTROL RECEIVER

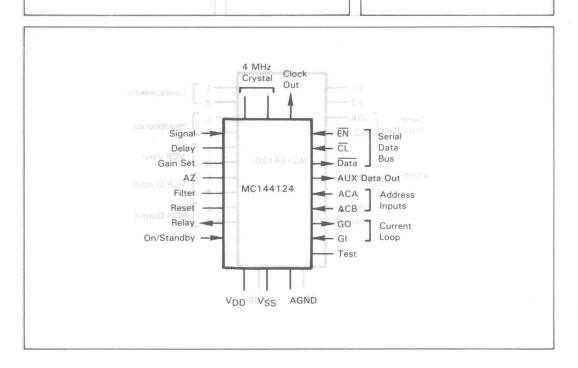
- Preamp/Detector for FSK Infrared Signals
- · Coil-less Input Circuit for High Noise Immunity
- · On-chip Bandpass Filtering
- F1/F2 Detection Using Pulse Counting Technique
- Data Validation and Address Recognition
- 2 Programmable Address Bits
- MPU Data Bus Interface
- Additional Serial Data Output
- Wake-up Logic
- Supply Relay Switch
- 5 mA Current Loop for Standby Indicator
- Uses 4 MHz Crystal
- Clock Output
- 10 V Supply
- Minimum External Components needed

CMOS

(LOW-POWER COMPLEMENTARY MOS)

HIGH PERFORMANCE REMOTE CONTROL RECEIVER





Product Preview

ONTROL RECEIVER REDODED DESTRUCTE VITE RECEIVER

- Decodes Baseband Dual Carrier Signals
- · Pilot Tone Demodulation and Identification
- Signal De-emphasis
- · Volume, Treble and Bass Control

(LOW-POWER COMPLEMENTARY MOS)

MC144124

- Stereobase Facility
- Pseudo Stereo Facility
- Dual Muting Facility
- Loudspeaker and Headphone Outputs
- VCR Input/Output
- · Hi-Fi Output
- All Functions Digitally Controlled
- Minimal External Components
- 5 V Supply DAY OFTEAST

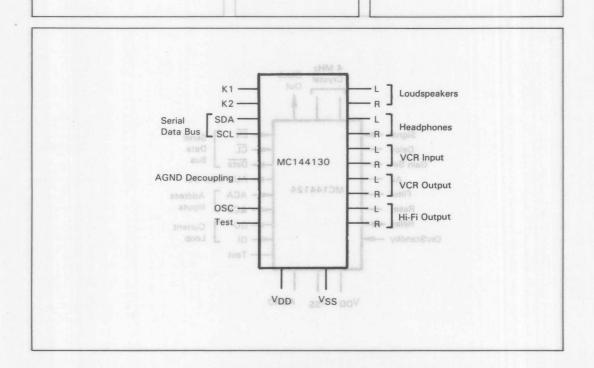
CMOS

(LOW-POWER COMPLEMENTARY MOS)

TV STEREO DECODER



P SUFFIX
PLASTIC PACKAGE
CASE 710



WOLV



MC145000 MC145001

MULTIPLEXED LCD DRIVERS MASTER AND SLAVE

The MC145000 (Master) LCD Driver and the MC145001 (Slave) LCD Driver are CMOS devices designed to drive liquid crystal displays in a multiplexed-by-four configuration. The Master unit generates both frontplane and backplane waveforms, and is capable of independent operation. The Slave unit generates only frontplane waveforms, and is synchronized with the backplanes from the Master unit. Several Slave units may be cascaded from the Master unit to increase the number of LCD segments driven in the system. The maximum number of frontplanes is dependent upon the capacitive loading on the backplane drivers and the drive frequency. The devices use data from a microprocessor or other serial data and clock source to drive one LCD segment per bit.

- Microprocessor Compatibility
- Serial Data, Externally Clocked
- Multiplexing-By-Four
- Net dc Drive Component Less Than 50 mV
- Master Drives 48 LCD Segments
- Slave Provides Frontplane Drive for 44 LCD Segments
- Drives Segments Up to one Square Centimeter (0.155 Square Inches)
- Display Operating Frequency = 250 Hz Maximum
- Supply Voltage Range = 3 V to 6 V
- Latch Storage of Input Data
- Low Power Dissipation
- Logic Input Voltage Can Exceed VDD
- Accomodates External Temperature Compensation
- 24-Pin DIP Configuration Master
- 18-Pin DIP Configuration Slave

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

MULTIPLEXED LCD DRIVERS
MASTER AND SLAVE

L SUFFIX P SUFFIX CERAMIC PACKAGE PLASTIC PACKAGE CASE 623 CASE 709 L SUFFIX P SUFFIX CERAMIC PACKAGE PLASTIC PACKAGE **CASE 726 CASE 707** ORDERING INFORMATION MC14XXXB Suffix Denotes Ceramic Package Plastic Package Limited Operating Temperature Range

PIN ASSIGNMENTS DVDD 18 VDD FP1 - 1 -FP1 1 FP2 osc_{out} FP2 Doscin FP3 oscin FP3 Frame-Sync. In Data Out
Data Clock FP4 Frame-Sync. Out FP4 MC145001 FP5 Data Out FP5 Slave MC145000 FP6 Data Clock FP6 □ Data In FP7 Data In FP7 FP11 FP8 □BP1 FP8 FP10 FP9 10 FP9 BP2 VSS Q 9 ВР3 FP10 C FP11 BP4 VSS 12 13 FP12

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the ranges $V_{SS}\!\leq\!V_{out}\!\leq\!V_{DD}$ and $V_{SS}\!\leq\!V_{in}\!\leq\!15$ V

Unused inputs must always be tied to an appropriate logic voltage level.

ADI-825

MASTER AND SLAVE

MAXIMUM RATINGS (Voltages referenced to VSS)

Characteristic	Symbol	Value	Unit	
DC Supply Voltage	V _{DD}	-0.5 to +6.5	٧	
Input Voltage, Data In and Data Clock,	Vin	-0.5 to 15	٧	
Input Voltage, Pin 22 of Master	V _{in osc}	-0.5 to VDD+0.5	٧	
DC Current Drain per Pin	1	10	mA	
Operating Temperature Range	TA	-40 to +85	°C	
Storage Temperature Range	T _{stq}	-65 to +150	°C	

ELECTRICAL CHARACTERISTICS

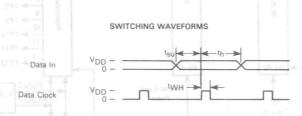
and the control of th		Symbol	VDD	-4	0°С		25°C		85	85°C	
MEVIAG COU Characteristic M		Symbol	V	Min	Max	Min	Тур	Max	Min	Max	Uni
RMS Voltage Across a Segment	"ON"	DJ fovali	3.0	B1 214	18533 10	10.101	1.73	POINT	ALLER	प्राप्त व	
(BPi-FPj)	Segment	VON	6.0	uo_pii	bil sv	ID_DI	3.46	NED	UM	51 <u>6</u> 1	V
	"OFF"	20 11229	3.0	State	-	2111	1.00	Hoplan	d bas	revenu	
	Segment	VOFF	6.0	ROSQE	0 8i bi	18, 80	2.00	RCKDIN	o ons	ensig	V
Average DC Offset Voltage	71	27.4	3.0	U TSA	30	F OTIO	10	30		30	
		Vdc	6.0	NU TRUE	50	0 10101	20	50	INV US	50	∘mV
Input Voltage	"0" Level	IO VILO 1	3.0	conser	0.90	4-	1.35	0.90	b <u>₹</u> 7∩8	0.90	av
		VIL	6.0	0. 7008	1.80	GOTTON.	2.70	1.80	geoni	1.80	melc
I HARINGA I AT THE LAND OF THE PARTY OF THE	"1" Level	V/	3.0	2.10	iveo	2.10	1.65	WITE	2.10	ms 81	ev.v
1985		VIH	6.0	4.20	iz Zon	4.20	3.30	edTo a	4.20	10/70	maior
Output Drive Current - Backplanes	14								atid to	d me	npe
High-Current State*							vtiliditsor	no On	000000	nomsi	W 0
VO = 2.85 V		IBH	3.0	150	-	75	190	-	35	O Toron	PμA
VO = 1.85 V		,BH	0.0	220	-	110	200	sn <u>a</u> ana	55	G lans	
$V_0 = 1.15 \text{ V}$				160	-	80	200	uo 2 y	40	ploith	M e
V _O = 0.15 V				400	VIII 6	200	300	ισπού	100	9D 19	V1 0
V _O = 5.85 V				500	-	250	300	48-LC	125	10786	VI e
$V_0 = 3.85 \text{ V}$		I _{BH}	6.0	1000	027	500	600	noTi a	250	9 evs	248
$V_0 = 2.15 \text{ V}$			155 S	800		400	500	Uam	200		0 0
$V_0 = 0.15 \text{ V}$		auent	0 001	500	BUTTUE	250	300	0_5111	125	tearto	ni ni
Low-Current State*					-	7 10 700					
V _O = 2.85 V				140	HOSEM	70	80	H Bud	35	yslas	0 0
VO-1.00 V		IBL	3.0	2.4	-	1.2	2.8	neff e	0.6	Yiggs	μΑ
VO = 1.15 V				2.2	-	1.1	2.5	ofto	0.5	Refr. S	11 0
$V_0 = 0.15 \text{ V}$				400	-	200	330		100	-9 w	.) 4
V _O = 5.85 V				190	-	95	105	oltage	45	nt gipi	. 1 0
V _O = 3.85 V		IBL	6.0	15	-	7.5	10		3.7		μΑ
V _O = 2.15 V _O = M = M = O = O		0.		13 850	inemic	6.5	9 570	netvill.	3.2	omeos	100
V _O = 0.15 V Output Drive Current — Frontplanes	-			800	-	425	Olyi - Albos	milita	100) m9-	9 24
High-Current State*		1 1 1				91	alicon - Star	eu gân	11P Cd	D di94	81 9
V _O =2.85 V				80	_	40	60	_	20		
V _O = 1.85 V		IFH	3.0	140		70	120		35		μΑ
V _O =1.15 V				180		60	100	_	30	_	
V _O =0.15 V				100	_	50	95	_	25	_	
V _O = 5.85 V				140	_	70	90	_	35	_	
V _O =3.85 V				360	273	180	250	_	90	_	3.00
V _O =2.15 V		IFH	6.0	400	_	200	240	_	100	_	μΔ
V _O =0.15 V	7			100		50	120	-	25		
Low-Current State*		nove	91	- 0	b119			lavel	28 /	0	bi
Vo = 2.85 V		108Cm		60	209	30	40	SOC	15	-	13
V _O = 1.85 V		IFL	3.0	2.8	300	1.4	2.8	Sec	0.7	-	μΑ
V _O = 1.15 V		O Date Or		2.2	319	1.1	2.5	3718	0.5	-	B
$V_0 = 0.15 \text{ V}$		Dama Cl	1000	100	339	50	100	MODE	25	-	5.0
V _O = 5.85 V		ni steGC	189	100	200	50	60	med	25	META	133
V _O =3.85 V		IFLE	6.0	16		8.0	10	10/7/	4.0	tald:	μΑ
V ₀ =2.15 V no not huoto sombed		01990	0.0	13	2759 289	6.5	9	980	3.2	-	μΑ
V _O = 0.15 V		W1 118		200	177	100	175	news and	50	-	hin.
nput Current	11	lin	6.0	_	±0.1	-	±0.00001	±0.1	-	± 1.0	μΑ
nput Capacitance (V _{in} = 0)		Cin	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		Inn	3.0	-	10	-	2.5	15	-	20	μА
proprieta logic voltaga level.		IDD	6.0	_	185	-	50	175	51	130	μΑ

^{*}For a time (t \cong 2.56/osc. freq.) after the backplane or frontplane waveform changes to a new voltage level, the circuit is maintained in the high-current state to allow the load capacitances to charge quickly. Then the circuit is returned to the low-current state until the next voltage level change occurs.

2

SWITCHING CHARACTERISTIC	$S (C_1 = 50 \text{ pF}, T_{\Delta} = 25 ^{\circ}C)$	
--------------------------	--	--

Characteristic	Symbol	V _{DD}	Min	Тур	Max	Unit	
Data Clock Frequency	fol	3.0 6.0	_	12.5 24	7.5 12.5	MHz	
Rise and Fall Times - Data clock	Bir 1	tr, tr	3.0 6.0	_	_	125 10	μS
Setup Time Data In to Data Clock		t _{su}	3.0 6.0	48 16	_	_	ns
Hold Time Data In to Data Clock	4	th	3.0 6.0	-5 0	_	_	ns
Pulse Width Data Clock	3 4	tWH	3.0 6.0	65 40	_	_	ns



DEVICE OPERATION

Figure 1 shows a block diagram of the Master unit. The unit is composed of two independent circuits: the data input circuit with its associated data clock, and the LCD drive circuit with its associated system clock.

Forty-eight bits of data are serially clocked into the shift register on the rising edges of the external data clock. Data in the shift register is latched into the 48-bit latch at the beginning of each frame period. (As shown in Figure 3, the frame period, tframe, is the time during which all the LCD segments are set to the desired "ON" or "OFF" states.)

The binary data present in the latch determines the appropriate waveform signal to be generated by the frontplane drive circuits, whereas the backplane waveforms are invariant. The frontplane and backplane waveforms, FPn and BPn, are generated using the system clock (which is the oscillator divided by 256) and voltages from the V/3 generator circuit (which divides VDD into one-third increments). As shown in Figure 3, the frontplane and backplane waveforms and the "ON" and "OFF" segment waveforms have periods equal to tframe and frequencies equal to the system clock divided by four.

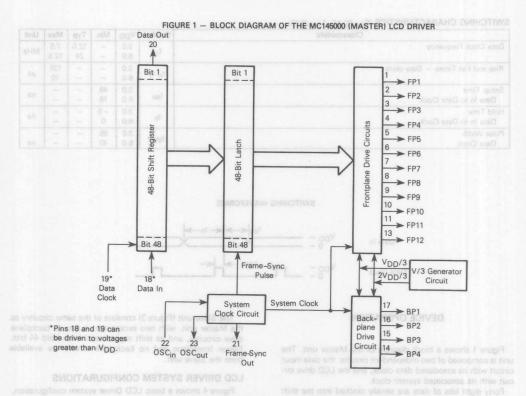
Twelve frontplane and four backplane drivers are available from the Master unit. The latching of the data at the beginning of each frame period and the carefully balanced voltage-generation circuitry minimize the generation of a net dc component across any LCD segment.

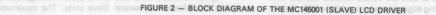
The Slave unit (Figure 2) consists of the same circuitry as the Master unit, with two exceptions: it has no backplane drive circuitry, and its shift register and latch hold 44 bits. Eleven frontplane and no backplane drivers are available from the Slave unit.

LCD DRIVER SYSTEM CONFIGURATIONS

Figure 4 shows a basic LCD Driver system configuration, with one Master and several Slave units. The maximum number of slave units in a system is dictated by the maximum backplane drive capability of the device and by the system data update rate. Data is serially shifted first into the Master unit and then into the following Slave units on the rising edge of the common data clock. The oscillator is common to the Master unit and each of the Slave units. At the beginning of each frame period, tframe, the Master unit generates a frame-sync pulse (Figure 3) which is received by the Slave units. The pulse is to ensure that all Slave unit frontplane drive circuits are synchronized to the Master unit's backplane drive circuits.

A single multiplexed-by-four, 7-segment (plus decimal point) LCD and possible frontplane and backplane connections are shown in Figure 5. When several such displays are used in a system, the four backplanes generated by the Master unit are common to all the LCD digits in the system. The twelve frontplanes of the Master unit are capable of controlling forty-eight LCD segments (6 LCD digits), and the eleven frontplanes of each Slave unit are capable of controlling forty-four LCD segments (6% LCD digits).





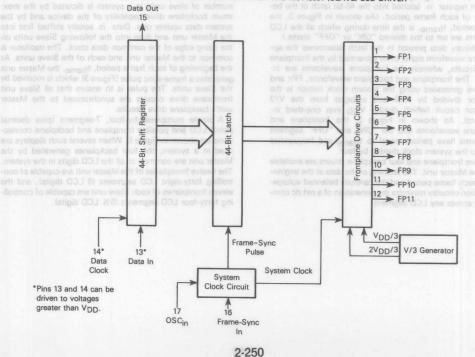


FIGURE 3 - VOLTAGE WAVEFORMS

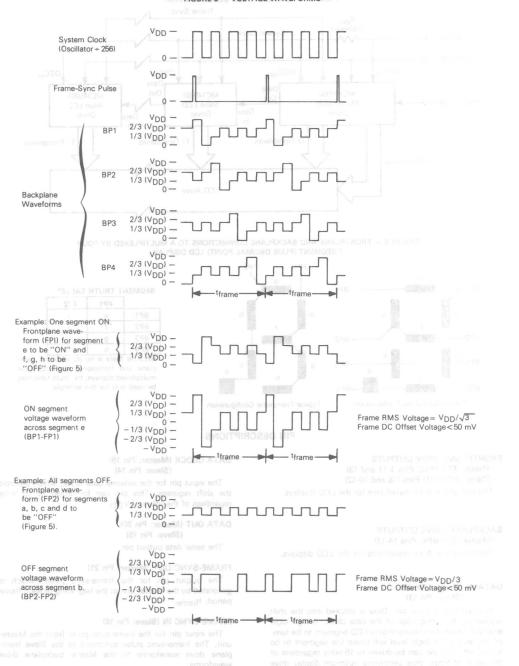


FIGURE 4 - BASIC SYSTEM CONFIGURATION

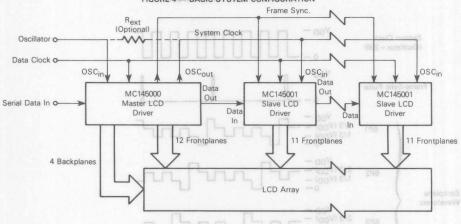
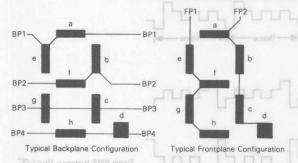


FIGURE 5 — FRONTPLANE AND BACKPLANE CONNECTIONS TO A MULTIPLEXED-BY-FOUR 7-SEGMENT (PLUS DECIMAL POINT) LCD DISPLAY



SEGMENT TRUTH TABLE*

	FP1	FP2	
BP1	е	а	
BP2	f	b	200
BP3	9 man	mas Col III	30
BP4	h	bred MO	100

*Because there is no standard for backplane and frontplane connections on multiplexed displays, this truth table may be used only for this example.

PIN DESCRIPTIONS

FRONTPLANE DRIVE OUTPUTS

(Master: FP1-FP12; Pins 1-11 and 13) (Slave: FP1-FP11; Pins 1-8 and 10-12)

The frontplane drive waveforms for the LCD displays.

BACKPLANE DRIVE OUTPUTS (Master: BP1-BP4; Pins 14-17)

The backplane drive waveforms for the LCD displays.

DATA IN (Master: Pin 18) (Slave: Pin 13)

The serial data input pin. Data is clocked into the shift register on the rising edge of the data clock. A high logic level will cause the corresponding LCD segment to be turned on, and a low logic level will cause the segment to be turned off. This pin can be driven to 15 volts regardless of the value of VDD, thus permitting optimum display drive voltage.

DATA CLOCK (Master: Pin 19) (Slave: Pin 14)

The input pin for the external data clock, which controls the shift registers. This pin can be driven to 15 volts regardless of the value of VDD.

DATA OUT (Master: Pin 20) (Slave: Pin 15)

The serial data output pin.

FRAME-SYNC OUT (Master: Pin 21)

The output pin for the frame-sync pulse, which is generated by the Master unit at the beginning of each frame period, tframe.

FRAME-SYNC IN (Slave: Pin 16)

The input pin for the frame-sync pulse from the Master unit. The frame-sync pulse synchronizes the Slave front-plane drive waveforms to the Master backplane drive waveforms.

OSC_{in} (Master: Pin 22) and affiline it ligible to differentiation (Slave: Pin 17) and good a strenges formed work

The input pin to the system clock circuit. The oscillator frequency is either obtained from an external oscillator or generated in the Master unit by connecting an external resistor between the OSC_{in} pin and the OSC_{out} pin (Pin 23). Figure 6 shows the relationship between resistor value and frequency.

OSCout (Master: Pin 23) a available lotted of beau ed year

The output pin of the system clock circuit. This pin is connected to the ${\sf OSC}_{\sf in}$ input (Pin 17) of each Slave unit.

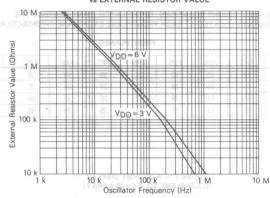
V_{DD} (Master: Pin 24) (Slave: Pin 18)

The positive supply voltage.

VSS (Master: Pin 12)

The negative supply (or ground) voltage and logic zero in-





APPLICATIONS

The following examples are presented to give the user further insight into the operation and organization of the Master and Slave LCD Drivers.

An LCD segment is turned either on or off depending upon the RMS value of the voltage across it. This voltage is equal to the backplane voltage waveform minus the frontplane voltage waveform. As previously stated, the backplane waveforms are invariant (see Figure 3). Figure 10 shows one period of every possible frontplane waveform.

For a detailed explanation of the operation of liquid crystal materials and multiplexed displays, refer to a brochure entitled "Multiplexed Liquid Crystal Displays," by Gregory A. Zaker, General Electric Company, Liquid XTAL Displays Operation, 24500 Highpoint Road, Cleveland, Ohio 44122.

Example 1: Many applications (e.g., meters, gasoline pumps, pinball machines, and automobile dashboard displays) require that, for each display update, an entirely new set of data must be shifted into the Master and cascaded Slave units. The correspondence between the frontplane-backplane intersections at the LCD segments and the data bit locations in the 48-bit latch of the Master (or 44-bit latch of the Slave) is necessary information to the system designer. In Figure 1, it is shown that data is serially shifted first into the 48th-bit location of the shift register of the Master. Thus, after 48 data bits have been shifted in, the

first bit to be entered has been shifted into bit-location one, the second bit into bit-location two, and so on. Table 1 shows the bit location in the latch that controls the corresponding frontplane-backplane intersection. For example, the information stored in the 26th-bit location of the latch controls the LCD segment at the intersection of FP7 and BP3. The voltage waveform across that segment is equal to (BP3 minus FP7). The same table, but with the column for FP12 deleted, describes the operation of the Slave unit.

In applications of this type, all the necessary data to completely update the display are serially shifted into the Master and succeeding Slave units within a frame period. Typically, a microprocessor is used to accomplish this.

Example 2: Many keyboard-entry applications, such as calculators, require that the most significant digit be entered and displayed first. Then as each succeeding digit is entered, the previously entered digits must shift to the left. It is, therefore, neither necessary nor desirable to enter a completely new set of data for each display change. Figure 7 shows a representation of a system consisting of one Master and three Slave units and displaying 20 LCD digits. If each digit has the frontplane-backplane configuration shown in Figure 5, the relationship between frontplanes, backplanes, and LCD segments in the display is shown in Table 2.

Digits (or alphanumeric characters) are entered, mostsignificant digit first, by using a keyboard and a decoder external to the MC145000. Data is entered into the Master and cascaded Slave units according to the following format:

1) Initially, all registers and latches must be cleared by entering 160 zero data bits. This turns off all 160 segments of the display.

2) Entering the most-significant digit from the keyboard causes the appropriate eight bits to be serially shifted into the Master unit. These eight bits control LCD segments a through h of digit 1, and cause the desired digit to be displayed in the least-significant digit location.

3) Entering the second-most-significant digit from the keyboard causes eight more bits to be serially shifted into the Master unit. These eight bits now control LCD segments a

through h of digit 1, and the previously entered eight bits now control segments a through h of digit 2. Thus the two digits are displayed in the proper locations.

4) Entering the remaining 18 digits from the keyboard fills the 20-digit display. Entering an extra digit will cause the first digit entered to be shifted off the display.

Example 3: In addition to controlling 7-segment (plus decimal point) digital displays, the MC145000 and MC145001 may be used to control displays using 5×7 dot matrices. A Master and three Slave units can drive 180 LCD segments, and therefore are capable of controlling five 5×7 dot matrices (175 segments). Two control schemes are presented in Figures 8 and 9; one using a single Master unit, and one using two Master units.

TABLE 1 - THE BIT LOCATIONS, IN THE LATCH, THAT CONTROL THE LCD SEGMENTS LOCATED AT EACH FRONTPLANE-BACKPLANE INTERSECTION

FRONTPLANES

	FP1	FP2	FP3	FP4	FP5	FP6	FP7	FP8	FP9	FP10	FP11	FP12
BP1	4	8	12	16	20	24	28	32	36	40	44	48
BP2	3	7	11	15	19	23	27	31	35	39	43	47
BP3	2	6	10	14	18	22	26	30	34	38	42	46
BP4	1	5	9	13	17	21	25	29	* 33	37	41	45

FIGURE 7 — A 20-DIGIT DISPLAY (EQUIVALENT TO A 4×40 ARRAY)

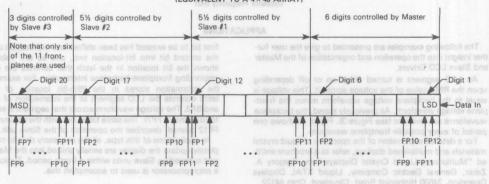


TABLE 2 — THE RELATIONSHIP BETWEEN FRONTPLANE-BACKPLANE INTERSECTIONS AND LCD SEGMENTS FOR THE SYSTEM CONFIGURATION OF FIGURE 7

	-	erio.		/aste	t yd a l	e noi	-	-	Slave #1				Slave #2						Slave #3				
e fi	FP12	FP11	FP10	FP9		FP2	FP1	FP11	FP10		FP1	FP11	FP10	FP9		FP2	FP1	FP11	FP10		FP7	FP6	
BP1	a1	e1	a2	e2	word	a6	e6	a7	e7	-5	a12	e12	a13	e13	ni n	a17	e17	a18	e18	mari 3	a20	e20	
BP2	b1	f1	b2	f2	beatle of	b6	f6	b7	f7	CON I	b12	f12	b13	f13	4 43 13	b17	f17	b18	f18	60X	b20	f20	
BP3	c1	g1	c2	g2	2000	c7	g6	c7	g7		c12	g12	c13	g13	Caba	c17	g17	c18	g18	do o	c20	g20	
BP4	d1	h1	d2	h2		d6	h6	d7	h7		d12	h12	d13	h13		d17	h17	d18	h18		d20	h20	
	dig	it 1	dig	it 2		dig	it 6	dig	it 7		dig	it 12	digi	t 13		digi	t 17	dig	it 18		digi	t 20	

FP5

FP6

FP9

FP7

FP6

FP8

FP4

FP10

FP2

FP3

FIGURE 8 — EXAMPLE OF A 5×7 DOT MATRIX DISPLAY SYSTEM CONTROLLED
BY ONE MASTER AND THREE SLAVE UNITS

Master

Slave #1

Slave #2

Slave #3

FP11 FP9

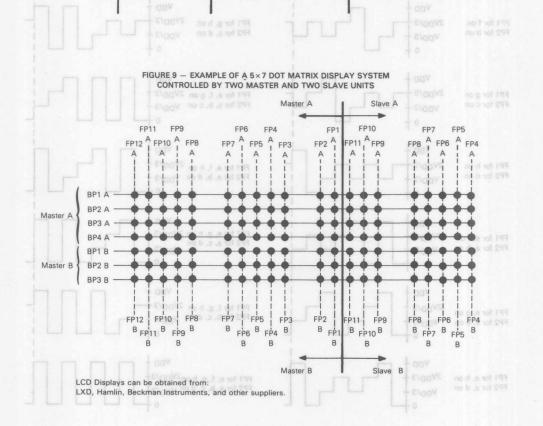
FP2 FP11 FP10 FP5 FP3 FP1 FP7 FP5 FP3 FP9 FP7 FP5

FP11

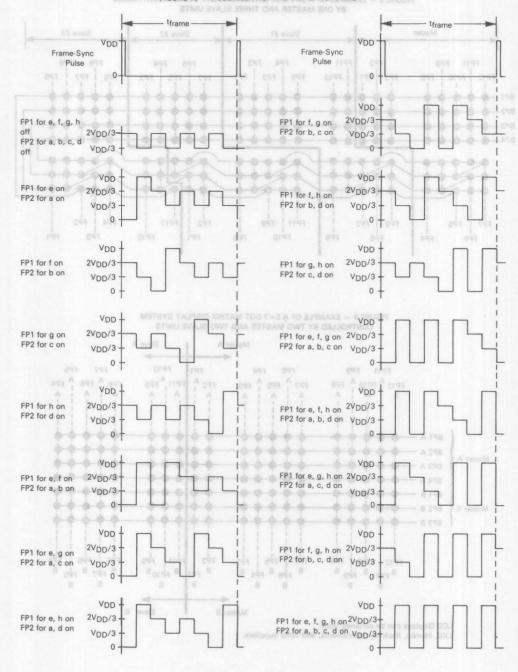
FP9

FP8

FP2









MC145026 MC145027 MC145028 MC145029

MC145026 ENCODER, MC145027/MC145028/MC145029 DECODERS

The MC145026 will encode nine bits of information and serially transmit this information upon receipt of a transmit enable, $\overline{\text{TE}}$, (active low) signal. Nine inputs may be encoded with trinary data (0,1, open) to allow 3^9 (19,683) different codes.

Three decoders are presently available and they use the same transmitter — the MC145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The MC145027 will interpret the first five transmitted bits as address and the last four bits as data. The MC145029 will interpret the first four transmitted bits as address and the last five bits as data. The MC145028 will treat all nine bits as address. If no errors are received, the MC145027 will output four data bits, and the MC145029 will output five data bits, when the transmitter sends address codes that match that of the receiver. A valid transmission output will go high on the decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

- May be Addressed in either Binary or Trinary
- Trinary Addressing Maximizes Number of Codes
- Interfaces with RF, Ultrasonic, or Infrared Transmission Medias
- 4.5 V to 18 V Operation
- On-Chip R/C Oscillator; No Crystal Required
- High External Component Tolerance; Can use 5% Components
- Standard B-Series Input and Output Characteristics

CMOS MSI

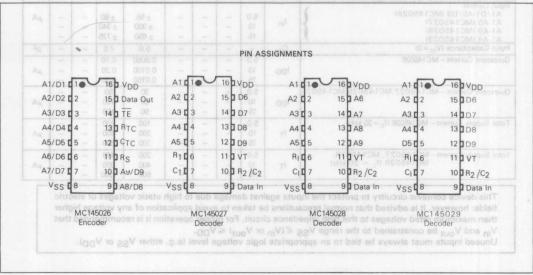
(LOW-POWER COMPLEMENTARY MOS)

REMOTE CONTROL ENCODER/DECODER PAIRS

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MC14XXXX Suffix Denotes
L Ceramic Package
P Plastic Package



ADI-855

MC145026 MC145027 MC145028 MC145029

MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +18	٧
Input Voltage, All Inputs	V _{in}	-0.5 to V _{DD} +0.5	٧
DC Current Drain Per Pin	1	10	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stq}	-65 to +150	°C

MOTOROLA

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	VDD	18/-4	0°C	end an	25°C	26 will	+ 85	5°C	Unit
Characteristic		Symbol	V	Min	Max	Min	Тур	Max	Min	Max	Oilli
Output Voltage	"0" Level	F,O) BIS	5.0	0.11 TABLE	0.05	DOUB SIL	0	0.05	-1891U	0.05	- SAII
V _{in} = V _{DD} or 0		VOL	10	-	0.05	po_Inet	0 50	0.05	E WOR	0.05	V
		emes en	15	year	0.05	delleve	App. O seud	0.05	etwood	0.05	
	"1" Level	nd-E aut	5.0	4.95	81 <u>a</u> D0	4.95	5.0	137 8	4.95	1	CHARAL
V _{in} = 0 or V _{DD}		VOH	10	9.95	blus a	9.95	1010	тещте	9.95	b <u>n</u> s	V
		ed bits as	15	14.95	12211	14.95	15 V	4502	14.95	T_st	
Input Voltage	"0" Level	Perioreim	HW U	0000	UNI E	FFL . SIR	D 36 STO 1	101 126	901 0	15,225	HUDS
$(V_0 = 4.5 \text{ or } 0.5 \text{ V})$		as data	5.0	1 125	1.5	dress a	2.25	1.5	right if	1.5	ert
(V _O =9.0 or 1.0 V)		VIL	10	2231	3.0	22rd e	4.50	3.0	15028	3.0	V
(V _O = 13.5 or 1.5 V)		end the	15	stab	4.0	rueluo	6.25	4.0	A with	4.0	
CASE 620	"1" Level	-DS VOOR	5 5591310	TEHEN	Brita in	MV LEN	Ilva data b	indino	mw e	COR	1 3119
(V _O = 0.5 or 4.5 V)	Level	tuo nois	5.0	3.5	VA.1	3.5	2.75	dalam	3.5	0208	eent
(V _O = 1.0 or 9.0 V)		VIH	10	7.0	n word	7.0	5.50	arlLno	7.0	op_lin	V
(V _O = 1.5 or 13.5 V)		beouber	15	11.0	rises s	11.0	8.25	nit bo n	11.0	Stem	teri
	Causas	0000000	10	11.0	11000	11.0	0.23	12261b	11.0	101110	Mily
Output Drive Current	Source		5.0	-2.5		-2.1	-4.2	-	-1.7		
$(V_{OH} = 2.5 \text{ V})$			5.0	-2.5 -0.52	_	-0.44	-4.2	_	-0.36	105-a/10	
$(V_{OH} = 4.6 \text{ V})$		ІОН	10					be-is	-0.36	10-18	m/
(V _{OH} = 9.5 V)			15	-1.3 -3.6	O to 1	-1.1 -3.0	-2.25 -8.8	Surss.	-0.9	V.	
$(V_{OH} = 13.5 \text{ V})$		Mediaa		III TOPE VIEW	(ben	111111111111111111111111111111111111111	F-11 (10 20 20 20 1) 1 2	1,341		etro!	
$(V_{OL} = 0.4 V)$	Sink		5.0	0.52	-	0.44	0.88	had o A	0.36	1748	9 4
$(V_{OL} = 0.5 V)$		IOL	10	1.3	in with	11111	2.25	Oscilla	0.9	ine in	mA
(V _{OL} = 1.5 V)		ponents	15	3.6	U ms3	3.0	8.8	Comp	2.4	9-10	1
Input Current - TE (MC145026, Pullup Device)			5.0	0.15-18	hattac	3.0	0 4.0 100	7.0	S-8 b	interis	5 8
		lin	10	-	-	16	20	26	-	-	μΑ
effection a strategy of			15	-	-	35	45	55	-	-	
Input Current											
R _S (MC145026)		lin	15	-	±0.3	-	± 0.00001	±0.3	-	± 1.0	μΑ
Data In (MC145027, MC145028, MC1450	029)										
Input Current	,										
A1/D1-A9/D9 (MC145026))		5.0	_	_	_	+ 55	+80	_	-	u.A
A1-A5 (MC145027)	>	lin	10	-	_	-	± 300	± 340	-	-	-
A1-A9 (MC145028) A1-A4 (MC145029))		15	-	-	-	± 650	± 725		-	
nput Capacitance (V _{in} =0)	,	Cin	- Tan	-	-	-	5.0	7.5	-	_	pF
Quiescent Current – MC145026	27	All I	5.0	-	_	-	0.0050	0.10	-	_	Pi
CONSTRUCTION OF THE PROPERTY O		Ipp	10				0.0000	0.10	_		μА
pros. pros. pr		100	15	-	5	Вта	0.0150	0.30	5	- TOIL	μ
Quiescent Current - MC145027, MC145028, N	AC1 45020	14	5.0	VIII	- 0	1	30	50	-	2107	-0-
Quiescent Current – MC (45027, MC (45028, MC)		CA	10	ı gar	_	T SA	60	100	- 5	1 SOV	A.
		IDD	15	1000	_	D-A	90	150			μA
TABAY KARA TABAY	M E	EA.	2000	1174				12.000		1 81	-
Total Supply Current – MC145026 (f _C = 20 kHz)		MA.	5.0	DETE	-	ATE	100	200	- 20	YOAR	WA.
		IT	10	12/10	-	-	200	400	-	-	μΑ
10A8 05 45 12 05 8		GA.	15		-	J-BA	300 01	600	- 8	1,301	LA.
Total Supply Current - MC145027, MC14502		IR .	5.0	THE	-	12TR	200	400	- 9	1001)A
MC145029 ($f_C = 20 \text{ k}$	(Hz)	IT.	10	100	-	150	400	800	-	Tan	μΔ
		100	15	1 1421	-	TATA	600	1200	- 1	1 77	100

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}.$ Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or $V_{DD}).$

2

MC145026 MC145027 MC145028 MC145029 CORANG M STCORANG M SECORANG M

SWITCHING	CHARACTERISTICS	1C1 - 50 nF	TA - 25001

Characteristic		Symbol	VDD	Min	Тур	Max	Unit
Output Rise and Fall Time 1935 8 2019 1991 1991 1991 1991 1991 1991 1991	ded and the	tTLH tTHL	5.0 10 15	igai s ns-ort	100 50 40	200 100 80	PA- ns
Data In Rise and Fall Time (MC145027, MC145028, MC145029)	cond).	LITTH	5.0 10 15	ilve si pins avie	sg a n sea7T	15 15 15	μs
Encoder Clock Frequency	ected to the		5.0 10 15	0 0	OSCIE OSCIE	2 5 10	MHz
Maximum Decoder Frequency (Referenced to Encoder Clock) (See Figure 9)	allup device	fcl	5.0 10 15	wol b wollor	force	240 410 450	kHz
TE Pulse Width Velid Trenemission, VT — This output will go high what the following conditions are satisfied.	Sing and Juni	twL	5.0 10 15	65 30 20	bebo riseq	fly end	ns T = gg
System Propagation Delay (TE to Valid Transmission)	DERS S) Al-Ad	COARDS	38 (88 (88	BN , IVA	182	MGT C1A5	Clock Cycles
Tolerance on Timing Components $ (\Delta R_{TC} + \Delta C_{TC} + \Delta R_1 + \Delta C_1) $ $ (\Delta R_2 + \Delta C_2) $	that must der for the					± 25 ± 25	%

OPERATING CHARACTERISTICS

MC145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0, 1, open) allowing $3^9=19,683$ possible codes. The transmit sequence will be initiated by a low level of the \overline{TE} input pin. Each time the \overline{TE} input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the \overline{TE} input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each \overline{TE} pulse).

Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to VpD. If only a low state is obtained, the input is assumed to be hard wired to Vss. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The transmit sequence is enabled by a logic zero on the TE input. This input has an internal pullup device so that a simple switch may be used to force the input low. While TE is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When TE is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

MC145027/MC145029

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The MC145027 assumes the first five bits are address and the MC145029

assumes the first four bits are address. These address bits must be encoded to match the address inputs at the receiver. If the address bits match, the next (data) bits are stored and compared to the last valid data stored. If this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

MC145028

This receiver operates in the same manner as the MC145027/MC145029 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.

Although address information normally is encoded in trinary, the designer should be aware that, for the MC145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only $2\times38=13,122$ different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the transmitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 \times C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words for error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figures 8 and 9.

SWITCHING CHARACTERISTICS ICL = 50 PR. TA = INDITRINS ONIH

MC145026 Encoder

A1/D1-A9/D9 — These inputs will be encoded and the data serially output from the encoder.

Vss - The most negative supply (usually ground).

RS, CTC, RTC — These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

TE — This Transmit-Enable (active low) input will initiate transmission when forced low. An internal pullup device will keep this input high normally.

Data Out — This is the output of the encoder that will present the serially encoded signals.

VDD - The most positive supply.

MC145027, MC145028, MC145029 DECODERS

A1-A5 (MC145027), A1-A9 (MC145028), A1-A4 (MC145029) — These are the address inputs that must match the corresponding encoder inputs in order for the decoder to output data.

D6-D9 (MC145027), D5-D9 (MC145029) — These outputs will give the information that is presented to the corresponding encoder inputs. Note: only binary data will be acknowledged; a trinary open will be decoded as a logic one.

 R_1 , C_1 — These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant $R_1 \times C_1$ should be set to 1.72 transmit clock periods. $R_1C_1 = 3.95$ RTCCTC.

 R_2/C_2 — This pin accepts a resistor to VSS and a capacitor to VSS that are used to detect both the end of an encoded word and the end of transmission. The time constant $R_2 \times C_2$ should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R_2C_2) to detect the dead time between transmitted words. $R_2C_2 = 77\ R_{TC}C_{TC}$.

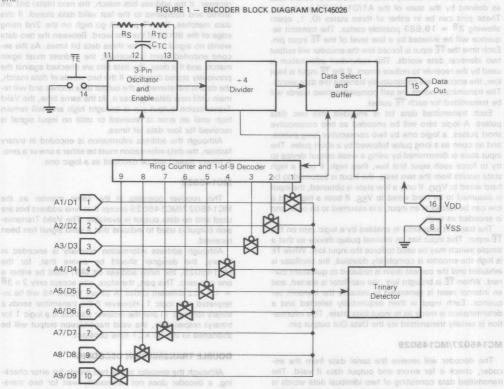
Valid Transmission, VT — This output will go high when the following conditions are satisfied:

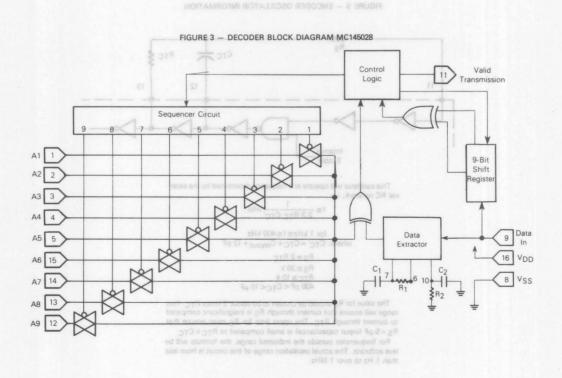
- the transmitted address matches the receiver address, and
- 2. the transmitted data matches the last valid data received.

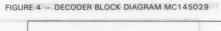
VT will remain high until either a mismatch is received, or no input signal is received for four data bit times.

VDD - The most positive supply.

Vss - The most negative supply (usually ground).







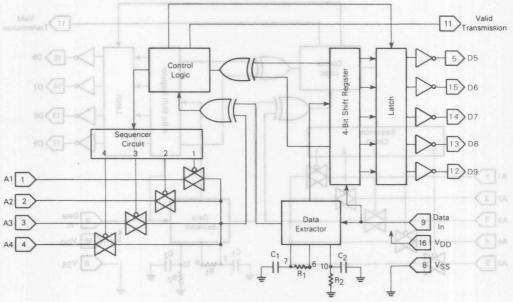
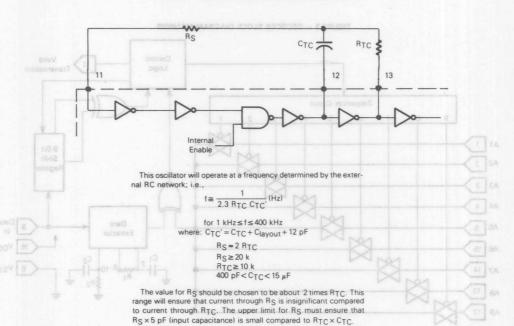


FIGURE 5 - ENCODER OSCILLATOR INFORMATION



For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1 Hz to over 1 MHz.

MC145026 MC145027 MC145028 MC145029 CORN OF CO

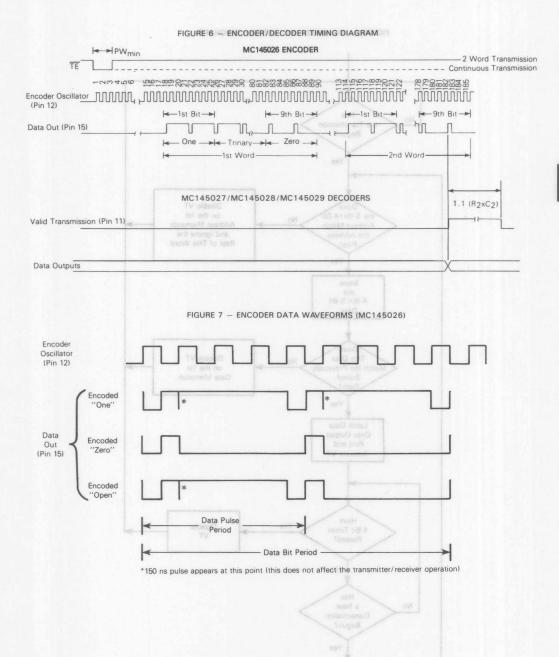
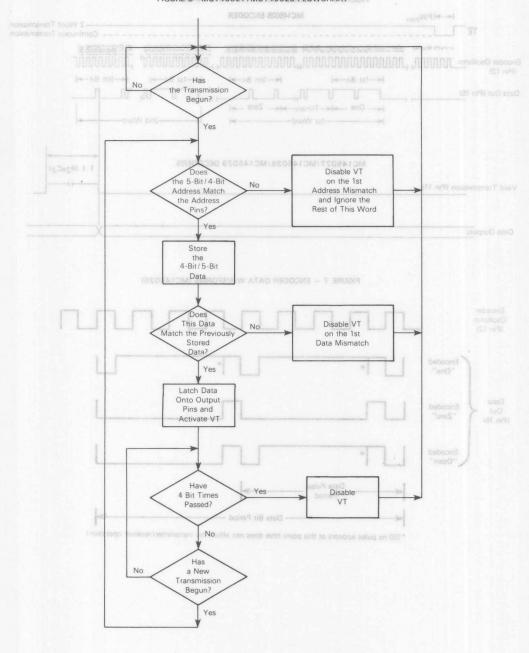
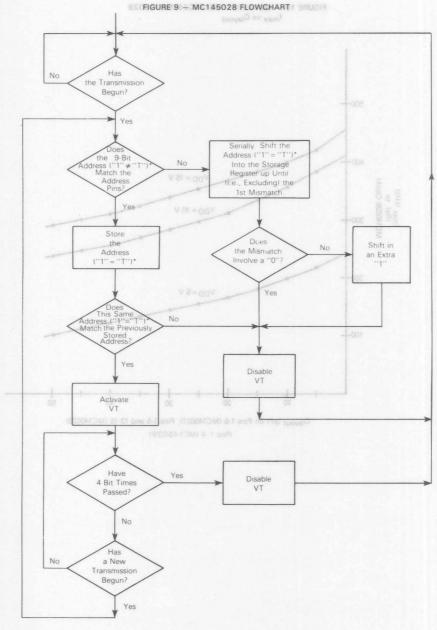
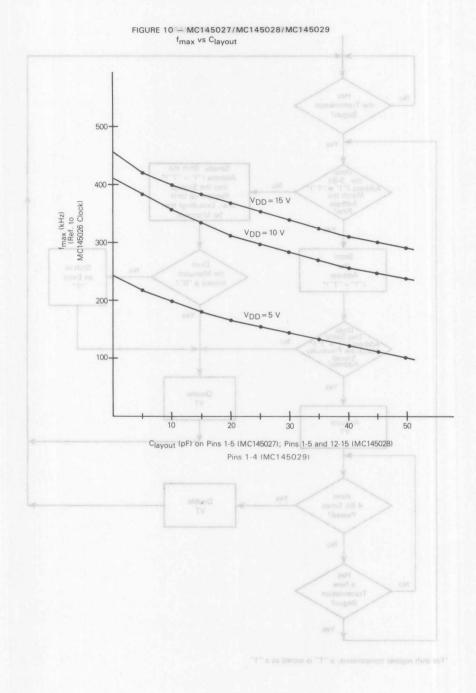


FIGURE 8 - MC145027/MC145029 FLOWCHART





*For shift register comparisons, a "T" is stored as a "1"



 $f_{\rm osc} = \frac{1}{2.3 \; R_{\rm TC} C_{\rm TC'}}$

 $R_1C_1 = 3.95 R_{TC}C_{TC}$ $R_2C_2 = 77 R_{TC}C_{TC}$

Example R/C Values (All Resistors and Capacitors are $\pm 5\%$)

FIGURE 11 - TYPICAL APPLICATION

R₂≥ 100 k C₂≥ 700 pF

 $C_{TC'} = C_{TC} + C_{layout} + 12 pF$ $100 pF \le C_{TC} \le 15 \mu F$ $R_{TC} \ge 10 k$; $R_S \approx 2 R_{TC}$ $R_1 \ge 10 k$ $C_1 \ge 400 pF$

0.1 µF

 $(C_{TC'} = C_{TC} + 20 pF)$

2-267

VDD

A1

fosc (kHz)	RTC	CTC'	RS	R ₁	C ₁	R ₂	C ₂
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 μF
8.53	10 k	5100 pF	20 k	10 k	0.02 μF	200 k	0.02 μF
1.71	50 k	5100 pF	100 k	50 k	0.02 uF	200 k	0.01 µF

TE

MC145026 MC145027 MC145028 MC145029

Trinary

Addresses

-

Repeat of Above

Repeat of Above VDD

A2

MC145026 MC145027 MC145028 MC145029

Product Preview

SERIAL A/D CONVERTER (SAD)

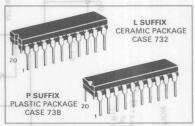
The MC145040 and MC145041 are 8-bit A/D converters with built-in serial I/O ports. The A/D section is composed of an all capacitor, charge redistribution D/A converter, a chopper stabilised comparator, and a successive approximation register. It performs a single conversion in 32 µsec (50 µsec including the serial data transfer of the result) and includes an on-chip 11 channel analog multiplexer. The conversion is ratiometric with respect to an externally supplied reference voltage. Analog input range extends from VSS to VDD. All digital interfacing — chip select, serial data clock, serial data input and serial data output — is handled via a 4-wire serial I/O port.

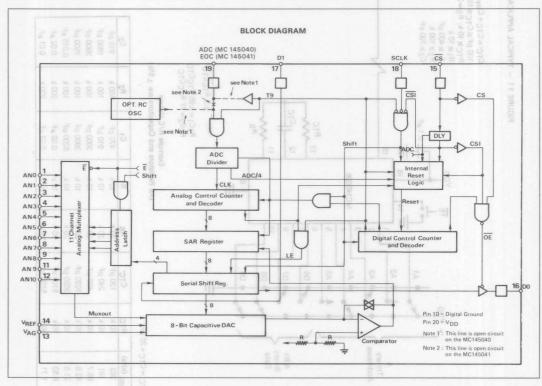
The MC145040 uses pin 19 as a clock input for the A/D conversion timing.

The MC145041 uses pin 19 as an end of conversion output status pin.

CMOS (LOW-POWER COMPLEMENTARY MOS)

SERIAL A/D CONVERTER (SAD)





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PLL FREQUENCY SYNTHESIZERS

The MC145104, MC145106, MC145107, MC145109, and MC145112 are phase locked loop (PLL) frequency synthesizer parts constructed with CMOS devices on a single monolithic structure. These synthesizers find applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 210 or 211 divider chain for that oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145104/ 5106/5112 have circuitry for a 10.24 MHz oscillator or may operate with an external signal. The MC145107/5109 require the external reference signal. Several of the circuits provide a 5.12 MHz output signal, which can be used for frequency tripling. A 29 (MC145106/ 5109/5112) or 28 (MC145104/5107) programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

The MC145106 is the full pinout version of this family of parts and has the capability of all parts in the family. The MC145104/ 5107/5109/5112 are limited pinout versions. See block diagrams for details.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 Vdc
- 16 or 18 Pin Plastic Packages
- 10.24 MHz Oscillator on Chip
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 29
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 210 or 211
- Three-State Phase Detector

CMOS MSI

MC145104

MC145107

MC145106 MUMIXAM

(LOW-POWER COMPLEMENTARY MOS)

PLL FREQUENCY SYNTHESIZERS

PSUFFIX PLASTIC PACKAGE CASE 648 P SUFFIX PLASTIC PACKAGE **CASE 707**

Pin-for- Pin Replacements for: MC145104 for SM5104, MM55104, MM55114 MC145106 for MM55106, MM55116 MC145107 for SM5107 (Sby 8.0 = gV) MC145109 for SM5109 MC145112 for SM5106

PIN ASSIGNMENTS 1 - VDD VSS - 18 10 VDD VSS == 16 17 □16 10 1 VDD VSS = 18 VDD VSS VSS 16 VDD Po 15 Po = 15 2 = P₀ 17 P₁ 16 PO 2 = fin 2 = **17** 2 = fin 2 = Fin Po 15 3 Osc in P1 14 3 = Oscin 3 C Osc in P1 14 3 C Osc in 3 🖂 Osc in 14 P₂ 15 P₃ 14 P₄ 13 4 COscout 4 Coscout Osc out P2 15 13 4 P2 ____ 13 4 = ÷2 out 4 FS P2 13 5 2Out P3 12 5 FS FS □ 14 FS 5 DET Out P3 12 5 P3 12 5 = 6 🛏 6 Det out FS P4 13 φ DET Out 6 🗆 P4 _____11 6 DETOUT P4 11 6 🖂 P4 11 7 P PETOU P5 12 LD P5 12 P6 11 7 LD P₅ 10 P₅ = 10 7 - LD P5 10 LD 7 8 = LD P6 - 11 NC 8 = P6 9 P6 9 P7 10 8 P7 9 = 9 P8 P7 10 MC145104 MC145106 MC145107 MC145109 MC145112

MC145104 MC145106 MC145107 MC145109 MC145112



MAXIMUM RATINGS (Voltages referenced to VSS)

MC145104

CMOS MSI

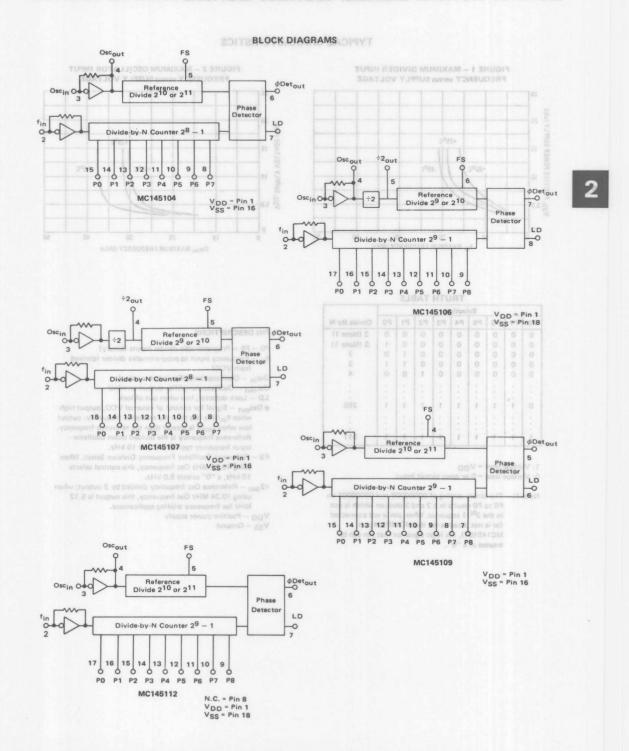
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to + 12	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	Vdc
DC Current Drain per Pin		10	mAdd
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in})$ or $V_{in} = V_{in}$. V_{out} ≤ V_{DD}.

The MC145104, MC145106, MC145102, MC145109, and

1.10			ne/joieth	VDD	185003	All Types	IVers, I	102/15/0
Characteristic			Symbol	Vdc	Min	Тур	Max	Unit
Supply Current		The MICT45 (U4)	ID	5.0	bns lei	6	10	mAdc
			e oscillate	10	i a wit y	20	35	6106/5
			5109 rec	1012	The Mil	28	50	s drive
Input Voltage	"O" Level	.12 MHz output	VIL	5.0	ed-to	15 mm = 2	1.5	Vdc
			A policin	10	m) 107 b	sev Ed ne	3.0	Isropie
			v 'Smedis	12	NACTOR O	SOU DU TH	3.6	A TON THE PARTY
	"1" Level		VIH	5.0	3.5	- July	D (21)	Vdc
		he inputs to the	lection.	10	7.0	nsup <u>a</u> ti it	ingiz_7ud	m ent
			d-to-supp	10012 bi	8.4	a tabiyib	oldenin	8160.td
nput Current (FS)	"0" Level	these inputs to	tes liniam	5.0	-5.0	-20	-50	μAdc
(Pull-up Resistor)			ed of ste	10	-15	-60	-150	onuore
P SUFFIX				12	-20	-80	-200	a medi
(PO to P8) MOAS DITEALS			. han 00	5.0	_	-	-0.3	odT
CASE 648			y bas Of	10	nay_com	1 1023otel	-0.3	
			level wo	6 12 .V	of st Abu	eup <u>er</u> l tu	-0.3	signal v
(FS)	"1" Level		provided	5.0	t of lock	gh, An ou	0.3	μAdc
			of lock or	10	tot lavel	"0" = dbi	0.3	lock di
			ris to not	12	io Ituli s	dt al-801	0.3	The
(P0 to P8)			vilms) s	5.0	7.5	30	75	and bine
(Pull-down Resistor)			ions. Se	10	22.5	90	225	5107/5
		block diagrams	BG .SHOR	12	30	120	300	NITO I C
(Oscin, fin)	"0" Level			5.0	-2.0	-6.0	-15	μAdc
PLASTIC PACKAGE				10	-6.0	-25	-62	
CASE 707				12	-9.0	-37	-92	uis e
(Oscin, fin)	"1" Level			5.0	2.0	6.0	15	biW e
				10	6.0	25	62	
				12	9.0	37	92	0 16 0
Output Drive Current			ІОН		on Chip)scillator	14 MHz	mAdc
$(V_O = 4.5 \text{ Vdc})$	Source			5.0	-0.7	-1.4	·	
(V _O = 9.5 Vdc) attempted and and and and				10	-1.1	-2.2	D 3 HM 9	0 5,11
(V _O = 11.5 Vdc) . MOTEME THE AOTEM OM			Coul aftest	12	-1.5	-3.0	Ismmau	eng en
(VO = 0.5 Vdc)	Sink	livider Inputs	IOL	5.0	0.9	1.8	lu9 girl3	mAdc
(V _O = 0.5 Vdc) totales tot total tom			DIESTITE	10	1.4	2.8	The Party	THE P
(V _O = 0.5 Vdc)			1	12	2.0	4.0	ctable P	e Sale
Input Amplitude			-		uninote	Phase P	se-Stati	Vp-p
(fin @ 4.0 MHz)				-	1.0	0.2	-	Sine
(Osc _{in} @ 10.24 MHz)					1.5	0.3		
Input Resistance			Rin			The second		MΩ
(Oscin, fin)	-			5.0	-	1.0	-	
			9	10	-	0.5	-	
		and the same of the same of		12	-	-	-	
Input Capacitance	-	Vop Vss 2216	Cin	V EL BEV	sav l	ES Y SI	SE SEV	pF
(Oscin, fin)			200	1 0 - 07	_65	6.0	- 00	100
Three State Leakage Current	1 122	01C 19 6130	ITL	4	8,00	14	71 [22]	μAdc
(φ Det _{out})		42 out 12 cm 12	133 h	5.0	NOMO !	13 - 21	1.0	100 mg
PERSON AND ADDRESS OF THE PERSON ADDRESS OF THE PERSON AND ADDRESS OF THE PERSON AND ADDRESS OF			20	10	20ut	- SE	1.0	81 =
	100		D 3	12	07:00	- 17	1.0	TROO
Input Frequency	1 == 1	0100 54 05	fin	4.5	4.0	12 3 _ UI	72	MHz
(-40°C to +85°C)	1 38		=38"	12	4.0	20- 6		11 12
Oscillator Frequency			Oscin	4.5	-	_	10.24	MHz

MC145104 MC145106 MC145107 MC145109 MC145112 MOTE ATOM (ADDIES ATOM)



TYPICAL CHARACTERISTICS

FIGURE 1 – MAXIMUM DIVIDER INPUT FREQUENCY versus SUPPLY VOLTAGE

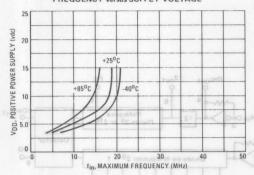
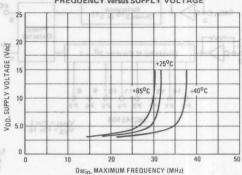


FIGURE 2 – MAXIMUM OSCILLATOR INPUT FREQUENCY versus SUPPLY VOLTAGE



TRUTH TABLE

			MC 14	n	lectio	Se	-32		F14
Divide By N	PO	P1	P2	Р3	P4	P5	P6	P7	P8
2 (Note 1)	0	0	0	0	0	0	0	0	0
3 (Note 1)	1	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0	0
3	1	1	0	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0	0
255	1	1	1	1	1	1	1	1	0
			0.						
								.	
								.	
511	1	1	1	1	1	1	1	1	1

1: Voltage level = V_{DD}

0: Voltage level = 0 or open circuit input

Note 1: The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2N-1 sequence. When pin is not connected (or is not listed as for the MC145104 and MC145107), the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

PO - P8 - Programmable divider inputs (binary)

f_{in} – Frequency input to programmable divider (derived from VCO)

Oscin - Oscillator/amplifier input terminal

Osc_{out} - Oscillator/amplifier output terminal

LD - Lock detector, low when out of lock

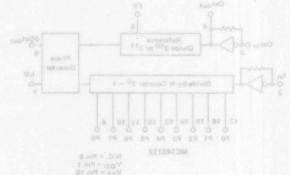
Φ Det_{out} – Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator input frequency typically 5.0 or 10 kHz.

FS - Reference Oscillator Frequency Division Select. When using 10.24 MHz Osc frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.

÷2_{out} — Reference Osc frequency divided by 2 output; when using 10.24 MHz Osc frequency, this output is 5.12 MHz for frequency tripling applications.

V_{DD} - Positive power supply

Vss - Ground



MC145104 MC145106 MC145107 MC145109 MC145112 agraxio M AGRANOM

PLL SYNTHESIZER APPLICATIONS

The MC145104, MC145106, MC145107, MC145109, MC145112 ICs are well suited for Applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer using a single crystal reference is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

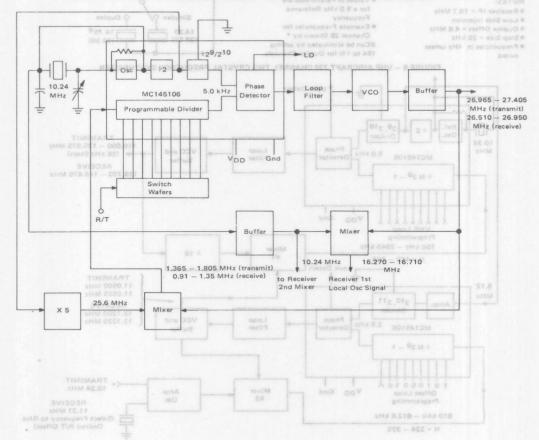
In addition to applications in CB radios, the MC145104-12 ICs can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling and loop programming techniques. In general, 300-400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

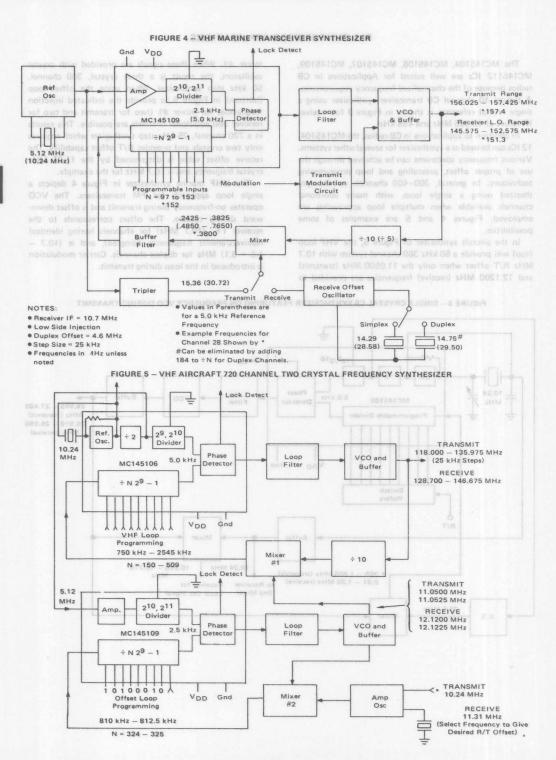
In the aircraft syntheizer of Figure 5, the VHF loop (top) will provide a 50 kHz 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to

mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal, 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels, are possible. This results in a 720 channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

single loop approach for FM transceivers. The VCO operates on-frequency during transmit and is offset downward during receive. The offset corresponds to the receiver I F (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

FIGURE 3 -- SINGLE CRYSTAL CB SYNTHESIZER FEATURING ON-FREQUENCY VCO DURING TRANSMIT







MC145143

CAIGAIUI

Advance Information

PLL FREQUENCY SYNTHESIZER

The MC145143 is a phase locked loop building block variation of the MC145106/MC145112 family. The device contains the oscillator circuitry required to operate with fundamental mode crystals to 10.24 MHz. The oscillator circuitry is connected to the phase detector through a divide-by-16 and a 29-1 divide-by-N counter. The reference oscillator can be divided in steps of 16 between 32 and 8176 before interfacing with the phase detector. The external input to the phase detector requires a Vss to VpD signal and forces the phase-detector output high if higher in frequency than the output of the divide-by-N counter. An out-of-lock signal is provided from the on-chip lock detector with a "0" level for an out-of-lock condition.

- Operation to 25 MHz
- 4.5 V to 12 V Operation
- Programmable Reference Divisions from 32 to 8176 (16X2 to 16X511)
- Three-State Phase Detection
- On-Chip Lock Detection

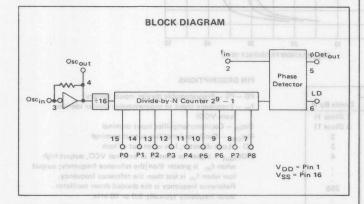
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

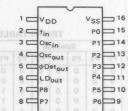
PLL FREQUENCY SYNTHESIZERS



P SUFFIX PLASTIC PACKAGE CASE 648



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to VSS)

	00		
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to + 12	V
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} + 0.5	V
DC Current Drain per Pin	1	10	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in})$ or $V_{out} \leq V_{OD}$.

ADI-808

Coperation to 25 MHz

Characteristics		Symbol	Min	Тур	Max	Units
Supply Current (Oscin = 12 MHZ)		ID	-	3.5	12	mA
Input Voltage	"0" Level	VIL	_	_	1.5	V
Input Voltage	"1" Level	VIH	3.5	-		V
Input Current (Excluding Pin 3)	RECEED	lin	PARL	±0.00001	±0.1	μΑ
Output Voltage (IO = 0.8 mA)		VOL	-	-	0.5	V
Output Voltage (IO = -0.6 mA)	or to	VOH	4.5	1311/5303	1.50	V
Oscillator Frequency	majerimo da abi	Oscin	25.0	ensida a al	DAFBAF	MHz
Oscillator Input Resistance	te contains the	Rin	1.2 Tamil	MC145	145106	ΜΩ
Oscillator Input Capacitance	famental mode	Cin/ el	saece o	ben 8 pen	circ ui try	топерязов
Three-State Leakage (connected to the	SI VITEIONIO	oillator	±0.005	±100	nA
Phase Detector Input Pulse Width — Positive O	φDetin	0.15	o n ubno	(I) 101091	μs	

TYPICAL MAXIMUM OSCILLATOR INPUT TO THE PROPERTY OF THE PROPER FREQUENCY versus SUPPLY VOLTAGE, about on to Juquo on the property of the prop VOLTAGE (Vdc) @ 4.5 V to 12 V Operation @ Programmable Reference +25°C @ Three-State Phase Dete +85°C -40°C @ On-Chip Look Detection 0 5.0 20 Oscin, MAXIMUM FREQUENCY (MHz)

TR	UT	H	TA	BL	E

			-1.0	n	lectio	Se	17.4	- Lance	
Divide By N	PO	P1	P2	P3	P4	P5	P6	P7	P8
2 (Note 1)	0	0	0	0	0	0	0	0	0
3 (Note 1)	1	0	0	0	0	0	0	0	0
2	0	1	0	80	0	0	0	0	0
3	1	1	0	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0	0
. 51									
15				.					
	1						.		
255	1	1	1	1	1	1	1	1	0
				.					
process and the same									
	. 1								
511	1	1	1	1	1	1	1	1	1

The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2^N-1 sequence.

	59+ nr 04-	

recommended that V_{In} and V_{OLD} be constrained to the range VSS ≤ (Via or

voltages or electric fields; however, it is

PO - P8 - Programmable divider inputs (binary) fin - Frequency input to programmable divider (derived from VCO)

Oscin - Oscillator/amplifier input terminal Oscout - Oscillator/amplifier output terminal LD - Lock detector, low when out of lock

φ Det_{out} - Signal for control of external VCO, output high when fin is greater than the reference frequency; output low when f_{in} is less than the reference frequency. Reference frequency is the divided down oscillator input frequency typically 5.0 or 10 kHz.

V_{DD} - Positive power supply

PIN DESCRIPTIONS

Vss - Ground



MC145144

PATCATON

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145144 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

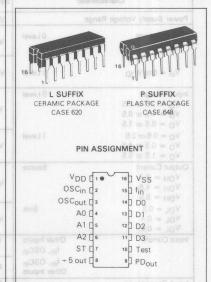
The MC145144 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, programmable reference divider, digital-phase detector, programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145144 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145144.

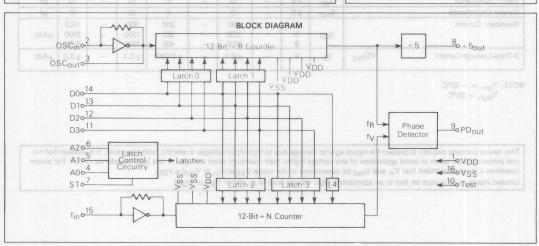
- Tailored for TV Tuning Applications
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3584 and 3839
- On- or Off-Chip Reference Oscillator Operation
- Single Modulus 4-Bit Data Bus Programming
- + N Range = 4 to 4092 in Steps of Eight
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Pin-for-Pin Compatible with the MN6044

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER





ADI-831

MC145144

MOTOROLA

MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +10	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain Per Pin		10	mA
DC Current Drain VDD or VSS Pins	1	30	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

Characteristic	Symbol	VDD	TL	ow	qrii ina-	25°C	mango	TH	igh	Units
Characteristic	Oymbor	*00	Min	Max	Min	Тур	Max	Min	Max	Ormo
Power Supply Voltage Range	VDD	CONT. 1545	3	9	3	Antibudges (9	3	9	Vdc
Output Voltage 0 Level Vin = VDD or 0	VOL	3 5 9	PLLTire	0.05 0.05 0.05	oolts r	0 0 0	0.05 0.05 0.05	taWi i provid crettoo	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$ 1 Level	Vон	3 5 9	2.95 4.95 8.95	ide prese	2.95 4.95 8.95	3 5 9	nwob i Mcbns	2.95 4.95 8.95	ncytope weeth ti	reque
Input Voltage 0 Level V _O = 2.5 or 0.5 V _O = 4.5 or 0.5 V _O = 8.5 or 1.5	VIL	3 5 9	-	0.9 1.5 2.7	-	1.35 2.75 4.05	0.9 1.5 2.7	DIEIN OGEN	0.9 1.5 2.7	Vdc
$V_{O} = 0.5 \text{ or } 2.5$ 1 Level $V_{O} = 0.5 \text{ or } 4.5$ $V_{O} = 1.5 \text{ or } 8.5$	VIH	3 5 9	2.10 3.5 6.3	- let <u>w</u> een	2.10 3.5 6.3	1.65 2.75 4.95	0 /=qri - eg/jeri	2.10 3.5 6.3	sl -B VI 0 em <u>o</u> nong	e < e
Output Current Source VOH = 2.7 VOH = 4.6 VOH = 8.5	ЮН	3 5 9	-0.44 -0.64 -1.3	- no	- 0.35 - 0.51 - 1.0	-0.66 -0.88 -1.3	farence it Catal recount	-0.22 -0.36 -0.7	or Off-	mAdo
V _{OL} = 0.3 V _{OL} = 0.4 V _{OL} = 0.5	IOL	3 5 9	0.44 0.64 1.3	itanet a	0.35 0.51 1.0	0.66 0.88 1.3	- 19 	0.22 0.36 0.7	boshso tins	alil" 4
Input Current Other Inputs fin, OSCin	IIL	9	-	± 0.3 ± 15	-1000	± 0.00001 ± 5	± 0.1 ± 10	Compat	±1.0 ±8	μAdo
Other Inputs	IIH	9	-	± 15 ± 0.3	-	±5 ±0.00001	±10 ±0.1	_	±8 ±1.0	
Input Capacitance	Cin	3-9	-	10	_	6	10	_	10	pF
Output Capacitance	Cout	3-9	-	10	-	6	10	-	10	pF
Quiescent Current	IDD	3 5 9	IAI O XS	800 1200 1600	-	200 300 400	800 1200 1600	13	1600 2400 3200	μAdc
3-State Leakage Current PD _{out}	IIL	9	T - 1	±0.1	7 /	±0.0001	±0.1	-	±3.0	μAdo

NOTE: $T_{low} = -40$ °C $T_{high} = 85$ °C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

SWITCHING CHARACTERISTICS (TA = 25°C, CI = 50 pF)

Characteristic Characteristic	Symbol	VDD	Min	Тур	Max	Units
latch that intormation. When high, any changes in the da	orm an or	3	31 - 10	100	200	n ulnen
Output Rise Time and official benefit and ad fliw notismoth	TLH	5	connecte	50	100	ns
	Primas A	9	crystal	40	80	NA REPUBLICA
+ 5 (First) - That + 5 output is one liftly the reference th	This is the same	3	to group	100	200	to at 172
Output Fall Time of problems of state of the support of the suppor	[†] THL	9	у-допшор-у	50 40	100 80	ns more
Setup Times and to Judicia sistement = (8 nls) and G	in, out the	3	deligned CMC		runia epri	ns
use as loop error signal. Note that output TS of stad of	tsu	9	the <u>a</u> xten	ul <u>p</u> asn	ad gale y	ns m gallque
		3	10000	3 01 0211	Other St. 18	D COURSELLE
Frequency Ty > It or Ty Leading. Positive Standard Requency Ty < It or Ty Leagung Negative Negative Standard Research	t _{su}	5 9	B, 6) A	(Pi <u>ns</u> 4,	вти <u>я</u> итя	ns
Hold Time	th	3	st edit of i	Hor sage	ostriumiw eshbe, arti	senil lugi
Data, Address to ST	th	9	_	_	aro is LS	I ns
Input Rise And Fall Times bell to nego Hel ad bluede bits	177.11	3	-	-	5	
OSC _{in} , fin	TLH	5 9	notion	d _ b	4 2	A PA SA
Input Pulse Width (AL, EL, EL, AL, AL, AL, AL, AL, AL, AL, AL, AL, A	6 5	3	40	30	risi <u>e</u> .i	0 0
OSC _{in} , f _{in} , Strobe	tW	5	35	20	rioteJ	ns 0
TS input it in the blak state, the IS (CS) is even distributed.	B B	9	25	15	riate.	0 1 0

FREQUENCY CHARACTERISTICS

	Vss (Pin 16) - Circuit Groun	C	.,	TI	ow		25°C		Th	igh	
	Characteristic	Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Units
Operating Frequency		900	3	07.99	17	-	27	14	-	12	
OSCin	Input = SQ Wave VDD - VSS	fmax	5	-	33	-	55	27	-	21	MHz
		00V6-	9	-	35	V	65	35	-	33	
	Input = Sin Wave Will mVn-n		3		11	-	21	10	-	9	
	*	fmax	5	-	20	-	34	17	-	15	MHz
			9	-	17		34	17	-	15	
Operating Frequency	4ω ∂.0 = 1		3	-	9		15	8	-	7	
fin	Input = SQ Wave VDD - VSS	fmax	5	-	19	-	30	15	-	15	MHz
			9	-	31	-	52	26	-	22	
	Input = Sin Wave 500 mVp-p		3	-	10	-	15	7	-	6	
		fmax	5	-	18	-	31	15	-	15	MHz
		000/6	9		21	A-	31	15	-	15	

 $T_{low} = -40$ °C $T_{high} = 85$ °C

for a typical design $\omega_{N} = (2\pi/10) \, t_{\rm f}$ (at phase detector input)

1 = 1

 $\begin{array}{ll} \text{DEFINITIONS: N} &= \text{Total Division Ratio in leadback Joop} \\ K_{\varphi} &= V_{DD}/k_{x} \text{ for PD}_{out} \\ \text{Kyco} &= \frac{2\kappa \delta f V_{CO}}{\Delta V_{VCO}} \end{array}$

VDD (Pin 1) - Positive power supply.

OSC_{in}, OSC_{out} (Pins 2 and 3) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 4, 5, 6) — AO, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches: (NOTE: Bit Zero is LSB)

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	Reference-Bits	0	1	2	3
0	0	1	Latch 1	Reference-Bits	4	5	6	7
0	1	0	Latch 2	÷ N Bits	3	4	5	6
0	1	1	Latch 3	÷ N Bits	7	8	9	10
1	0	0	Latch 4	+ N Bit	11	-	_	-
1	0	1						
1	1	0						
1	1	1						

ST (Pin 7) — When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low, will latch that information. When high, any changes in the data information will be transferred into the latches.

 \pm 5 (Pin 8) — The \pm 5 output is one fifth the reference frequency, f_R, that is derived by dividing the OSC_{in} signal by the reference divider.

PD_{out} (Pin 9) — Three-state output of phase detector for use as loop error signal. Note that output is of opposite polarity of the other PLL synthesizers in this family.

Frequency fy>fR or fy Leading: Positive Pulses.
Frequency fy<fR or fy Lagging: Negative Pulses.
Frequency fy=fR and Phase Coincidence: HighImpedance State.

TEST (Pin 10) — This input is used during manufacturing and should be left open or tied to VSS during normal operation.

DATA INPUTS (Pins 11, 12, 13, 14) — Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 11 (D3) is most significant.

 $f_{\mbox{\scriptsize in}}$ (Pin 15) — Input to +N portion of synthesizer. $f_{\mbox{\scriptsize in}}$ typically derived from loop VCO and is AC coupled into Pin 15. For larger amplitude signals (standard CMOS-logic levels) DC coupling may be used.

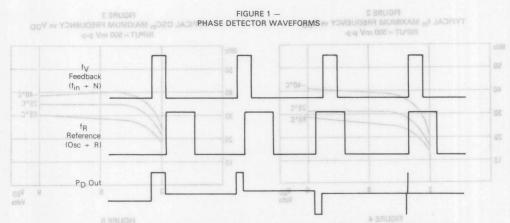
 $\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NC(R1 + R2)}}$

 $\zeta = 0.5 \omega_N (R2C + N/K_{\phi}K_{VCO})$

 $F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$

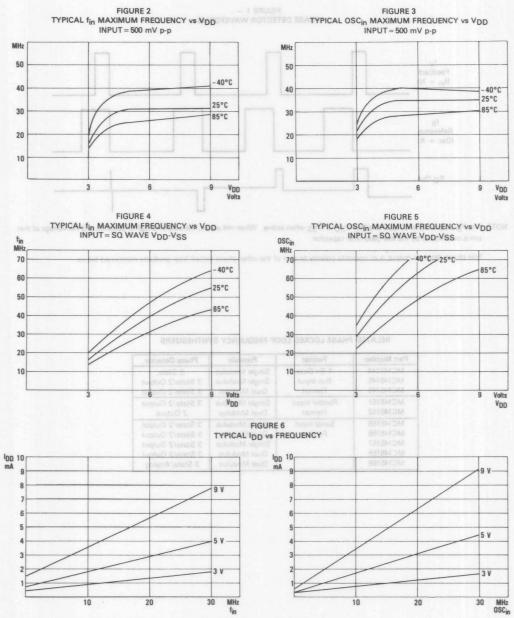
DEFINITIONS: N = Total Division Ratio in feedback loop
$$\begin{split} K_{\phi} &= V_{DD}/4\pi \text{ for PD}_{Out} \\ K_{VCO} &= \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}} \end{split}$$

for a typical design $\omega_{N}\cong (2\pi/10)~\mathrm{f_{f}}$ (at phase detector input) $_{\zeta}\cong 1$

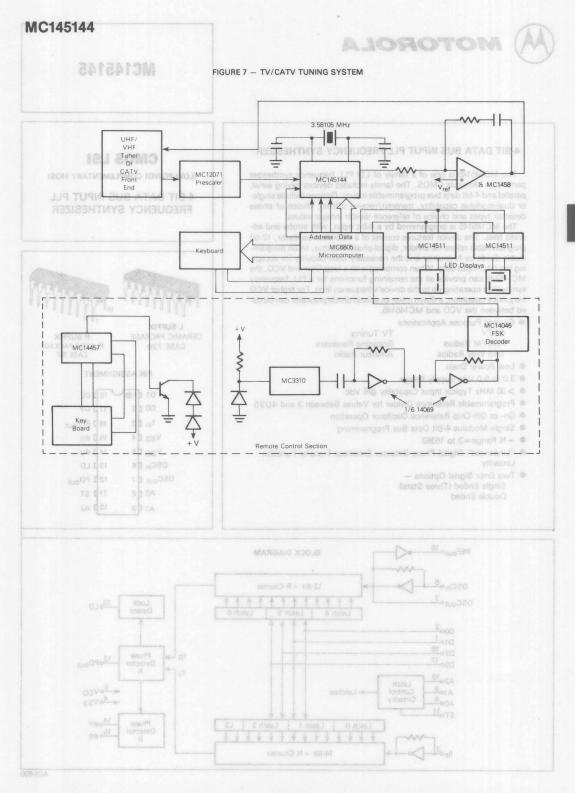


NOTE: The Pp_output state is equal to either Vpp or Vss when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

pin is determined by the low pass filter capacitor. This phase detector output is of opposite polarity to that of the other phase locked loop products mentioned below. RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS Part Number Format Prescale Phase Detector MC145144 Single Modulus 4-Bit Data 3 State MC145145 Bus Input Single Modulus 3 State/2 Output MC145146 Format Dual Modulus 3 State/2 Output MC145151 Parallel Input Single Modulus 3 State/2 Output MC145152 Format Dual Modulus 2 Output MC145155 Serial Input Single Modulus MC145156 Format Dual Modulus 3 State/2 Output MC145157 Single Modulus 3 State/2 Output MC145158 Dual Modulus 3 State/2 Output MC145159 **Dual Modulus** 3 State/Analog



NOTE: To compute total IDD add component due to fin with that due to OSCin.



MC145145

PPICALON

The MC145145 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145145 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145145 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145145.

General Purpose Applications

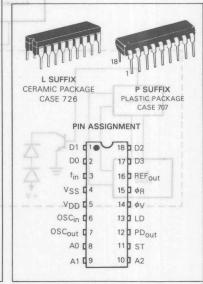
CATV AM/FM Radios Two Way Radios TV Tuning Scanning Receivers Amateur Radio

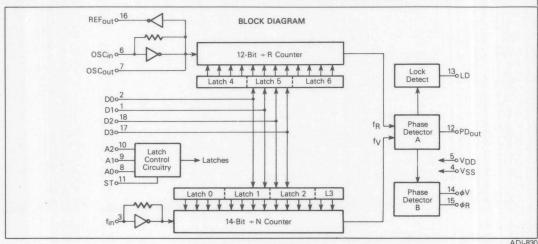
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Single Modulus 4-Bit Data Bus Programming
- + N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function-Linearity
- Two Error Signal Options Single Ended (Three State)
 Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER





MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +10	Vdc
Input Voltage, All Inputs	Vin	-0.5 to VDD +0.5	Vdc
DC Current Drain Per Pin		10	mA
DC Current Drain VDD or VSS Pins	1	30	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	1/	TIC	w		25°C		Th	Units	
Characteristic	Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Voltage Range	VDD	-	3	9	3	-	9	3	9	Vdc
Output Voltage 05 0 Level Vin = VDD or 0 00 00 00 00 00 00 00 00 00 00 00 00	VOL	3 5 9	-	0.05 0.05 0.05	-	0 0 0	0.05 0.05 0.05	Title Title	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD} 1 Level	Vон	3 5 9	2.95 4.95 8.95	-	2.95 4.95 8.95	3 5 9	1 1 1	2.95 4.95 8.95	ise and l	Put P
Input Voltage 0 Level V _O = 2.5 or 0.5 V _O = 4.5 or 0.5 V _O = 8.5 or 1.5	VIL	3 5 9	-	0.9 1.5 2.7	-	1.35 2.75 4.05	0.9 1.5 2.7	th be_	0.9 1.5 2.7	Vdc SO _{IO} S
V _O = 0.5 or 2.5 V _O = 0.5 or 4.5 V _O = 1.5 or 8.5	VIH	3 5 9	2.10 3.5 6.3	-	2.10 3.5 6.3	1.65 2.75 4.95	CTERIS	2.10 3.5 6.3) YOM	EQU
Output Current Source V _{OH} = 2.7 V _{OH} = 4.6 V _{OH} = 8.5	IOH	3 5 9	-0.44 -0.64 -1.3	- <u>_</u>	-0.35 -0.51 -1.0	-0.66 -0.88 -1.3	Chara	-0.22 -0.36 -0.7	ng Frequ	mAc
V _{OL} = 0.3 V _{OL} = 0.4 V _{OL} = 0.5	lor _s	3 5 9	0.44 0.64 1.3	Vm 008	0.35 0.51 1.0	0.66 0.88 1.3	-	0.22 0.36 0.7	- - -	
Input Current Other Inputs	- IIL E	9	-	±0.3 ±15		±0.00001 ±5	±0.1 ±10	gnsy	±1.0 ±8	μAd
f _{in} , OSC _{in} Other Inputs	IH e	9 9	-	± 15 ± 0.3	-	±5 ±0.00001	±10 ±0.1	_	±8 ±1.0	
Input Capacitance	Cin	3-9	1-	10	-	6	10	-	10	pF
Output Capacitance	Cout	3-9	-	10	-	6	10	-	10	pF
Quiescent Current	IDD	3 5 9	-	800 1200 1600	-	200 300 400	800 1200 1600	-	1600 2400 3200	μΑσ
3-State Leakage Current PD _{out}	IIL	9	-	±0.1	-	±0.0001	±0.1	-	±3.0	μAd

NOTE: $T_{low} = -40$ °C $T_{high} = 85$ °C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

NOTE: Tlow = -40°C Trigh = 85°C

SWITCHING CHARACTERISTICS (TA = 25 °C, CL = 50 pF)

THE BUILD STATES	Teau	Charac	teristic	-			 Symbol	VDD	Min	Тур	Max	Units
00 V 01 0.0 -		UY 1						3	-	100	200	200
Output Rise Time							TLH	5	- 1	50	100	ns
							7	9	- n	40	80	0.00
Am 0E								3	82¥ 10	100	200	0.00
Output Fall Time							tTHL	5	привя	50	100	ns
76 021 - 61 88 -								9	=	40	80	100
Setup Times	1.6						-	3	-	-	-	
Data to ST							t _{su}	5	-	-	-	ns
Data to 51								9	-	-	-	
								3	-	-	-	
Address to ST							t _{su}	500	BIRST:	ARAH	RICAL	ns
Tool Tool		2000		971	T.			9	-	-	-	-
Hold Time						.agv		3	climet:	Chara	-	
Data, Address to ST							th	5 9	apos	Voltage F	Supply	ns
Output Pulse Width	80.0	0		80.0	-	8	love J 0	3	70	120	170	Outpo
φ _R , φ _V with f _R in							tWH(φ)	5	50	100	150	ns
Phase With fy							(ννηιφ)	9	30	80	130	113
Input Rise and Fall Times	-	8	2.95		2.90	8	1.	3	-	-	5	1
000 6	- 1						TLH	5	-	_ 0	4	μS
OSCin, fin							THL	9	-	-	2	
Input Pulse Width							level t	3	40	30	epsilo)	
	8.0			e.o.			tw	5	35	20	=2.5_or 9	
OSC _{in} , f _{in} , Strobe							1	9	25	15	10_d.k=	- DV
35V 1 77 1 -	X X 1	9.00	1 -	1.7.7		100					1 10 0 0	101

REQUE	NCY (CHARA	CTERI	STICS	2.10	- 7.7	2.10	8 8	HI)		leved (0.5 or 0.5 or 0.5 or	
		6,3		9:55	6.3		6.8	6		T	ow		25°C		Th	igh	OV.
			Chara	cteristic				Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Units
Operatin	g Frequ	uency		88.0-	GC 01-		9900	1 5	3	-	17	-	27	14	-	12	O.V
OSCin	-			Input =	SQ Wave	VDD -	Vss	fmax	540		33	-	55	27	-	21	MHZ
ODAN				6.1-			757		9		35	-	65	35	-	33	100
				Input =	Sin Wave	500 m	/p-p	0	3		11	-	21	10	-	9	120
				88.0			10.0	fmax	5	-	20	-	34	17	-	15	MH
								max	9		17		34	17	-	15	14
Operatin	g Frequ	uency	1:03	100000.0	21 -	5.04	1 -	0	3	-	9	SHIP	15	8	-	7	- mode
fin	84		01主	Input = S	SQ Wave \	/DD -	Vss	fmax	5	-	19	State,	30	15	-	15	MH
				6主		西生	1	1	9	-	31	mil	52	26	-	22	
				Input =	Sin Wave	500 m\	/ p-p	-	3		10	COLUMN TO	- 15	7	-	6	
			10	1 8				fmax	5		18		31	15	eons	15	MHZ
								11192	900	0 1	21	-	31	15	100.670	15	Padang.

 $T_{low} = -40$ °C $T_{high} = 85$ °C

MC145145

DATA INPUTS (Pins 2, 1, 18, 17) — Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 17 (D3) is most significant.

 f_{in} (Pin 3) — Input to $\pm N$ portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels) DC coupling may be used.

VSS (Pin 4) - Circuit Ground.

V_{DD} (Pin 5) - Positive power supply.

OSC_{in}, OSC_{out} (Pins 6 and 7) — These pins form an onchip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 8, 9, 10) — A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

					200	-	9	
A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	+ N Bits	0	1	2	3
0	0	1	Latch 1	+ N Bits	4	5	6	7
0	1	0	Latch 2	+ N Bits	8	9	10	11
0	1	1	Latch 3	+ N Bits	12	13	_	_
1	0	0	Latch 4	Reference Bits	0	1	2	3
1	0	1	Latch 5	Reference Bits	4	5	6	7
1	1	0	Latch 6	Reference Bits	8	9	10	11
1	1	1		_NCR1	Ne	_	_	_

ST (Pin 11) — When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low, will latch that information. When high, any changes in the data information will be transferred into the latches.

 ${\sf PD_{out}}$ (Pin 12) — Three-state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses. Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses. Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

LD (Pin 13) — Lock detector signal. High level when loop is locked (f_R , f_V of same phase and frequency). Pulses low when loop is out of lock.

 ϕ_V , ϕ_R (Pins 14 and 15) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PDout).

If frequency fy is greater than fg or if the phase of fy is leading, then error information is provided by ϕ_V pulsing low. ϕ_B remains essentially high.

If the frquency fy is less than f $_R$ or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing low. ϕ_Y remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

REF_{out} (Pin 16) — Buffered output of on-chip reference oscillator or externally provided reference-input signal.

2

DATA INPUTS (Pins 2, 1, 18, 17) - INDICAD RETAIN 28A9 WOL - 9001 DEATH IN PINS INDICADE THE DESIGN - (17, 18, 17) - (18, 18) - (18,

televel and $\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NR1C}}$ and a solution and the second of δ and δ and δ and δ and δ and δ are solutions as δ and δ and δ are solutions as δ and δ and δ are solutions as δ and δ are solutions as δ and δ are solutions.

 $F(s) = \frac{\text{Yeague 1 woq evitico}}{\text{R1CS} + 1} - (8 \text{ n/q}) \text{ agV}$

LD (Pln 13) - Lock detector signal. High level when loop is locked (LR, LV of same phase and frequency). Pulses low when toop is out of lock.

 $\omega_{N} = \sqrt{\frac{K_{\phi}K_{V}CO}{NC(R1 + R2)}}$ $\xi = 0.5 \,\omega_{N} \,(R2C + N/K_{\phi}K_{V}CO)$

 $F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$ $\frac{R}{S(R1C + R2C) + 1}$ $\frac{R}{$

 $\zeta = \frac{\omega_{\text{NR2C}}}{2}$

Assuming gain A is very large, then:

 $F(s) = \frac{R2CS + 1}{R1CS}$

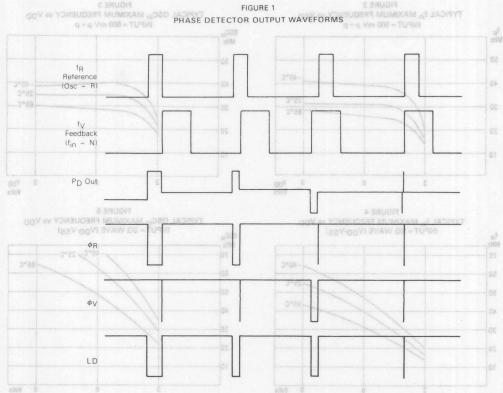
REF_{OUT} (Pin 18) — Buffered output of on-chip reference scribstor or externally provided reference-input signal.

NOTE: Sometimes R1 is split into two series resistors each R1 + 2. A capacitor C_C is then placed from the midpoint to ground to further filter $\phi \gamma$ and ϕR . The value for C_C should be such that the corner frequency of this network does not significantly affect ωN .

DEFINITIONS: N = Total Division Ratio in feedback loop $\begin{array}{ll} K_{\varphi} &= V_{DD}/4\pi \ \text{for PD}_{out} \\ K_{\varphi} &= V_{DD}/2\pi \ \text{for } \phi_{V} \ \text{and } \phi_{R} \end{array}$

 $K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

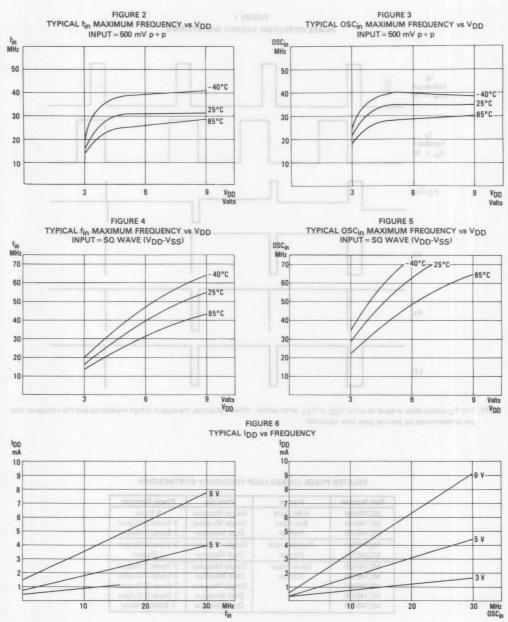
for a typical design $\omega_{\rm N} \cong (2\pi/10)~{\rm f_f}$ (at phase detector input) $\xi \cong 1$



NOTE: The PD output state is equal to either VDD or VSS when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

	RELATED I	PHASE LOCKED LO	OP FREQUENCY SY	NTHESIZERS	
	Part Number	Format	Prescale	Phase Detector]
	MC145144	4-Bit Data	Single Modulus	3 State	
	MC145145	Bus Input	Single Modulus	3 State/2 Output	
7.8	MC145146	Format	Dual Modulus	3 State/2 Output	
0	MC145151	Parallel Input	Single Modulus	3 State/2 Output	
	MC145152	Format	Dual Modulus	2 Output	
	MC145155	Serial Input	Single Modulus	3 State/2 Output	
8	MC145156	Format	Dual Modulus	3 State/2 Output	
	MC145157		Single Modulus	3 State/2 Output	
	MC145158		Dual Modulus	3 State/2 Output	
	MC145159		Dual Modulus	3 State/Analog	0.0

NOTE: To compute total IOD add component due to $f_{\rm iff}$ with that due to ${\rm OSC}_{\rm inf}$



NOTE: To compute total I_{DD} add component due to f_{in} with that due to OSC_{in} .

2

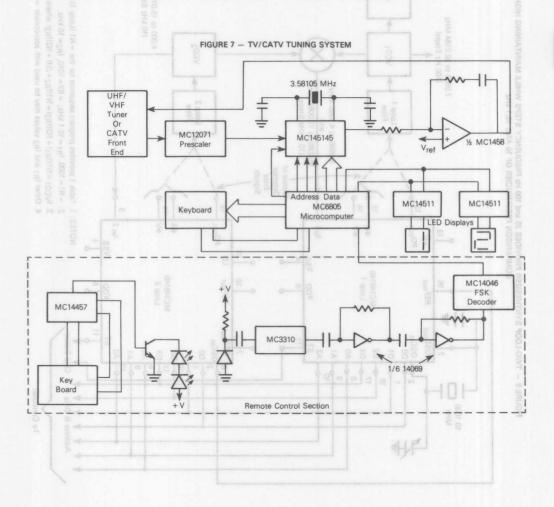
APPLICATIONS

The features of the MC145145 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

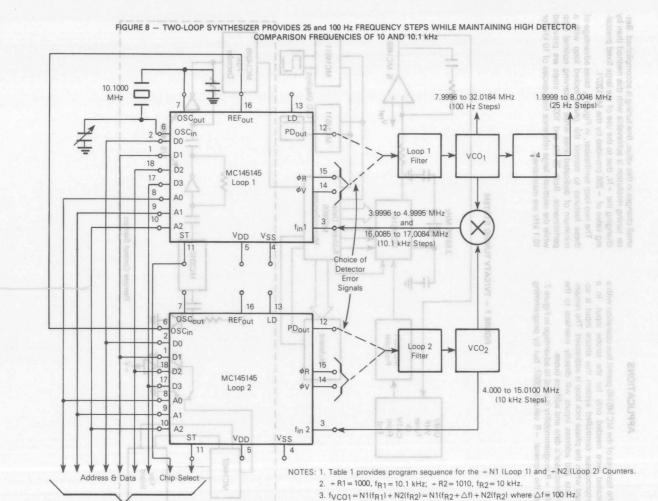
The + R programmability is used to advantage in Figure 7. Here, the nominal + R value is 3667; but by programming

small changes in this value, fine tuning is accomplished. Better tuning resolution is achievable with this method than by changing the +N, due to the use of the large fixed prescaling value of +256 provided by the MC12071.

The two loop synthesizer, in Figure 8, takes advantage of these features to control the phase locked loop with a minimum of dedicated lines while preserving optimal loop performance. Both 25 Hz and 100 Hz steps are provided while the relatively large reference frequencies of 10 kHz or 10.1 kHz are maintained.



4. Other f_{R1} and f_{R2} values may be used with appropriate + N1 and + N2 changes.

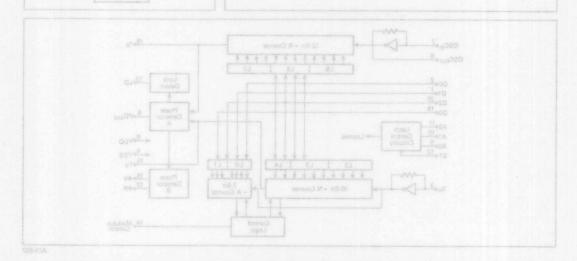


To Controller



TABLE 1 — PROGRAMMING SEQUENCE FOR TWO-LOOP SYNTHESIZER OF FIGURE 8

	÷ N1	fin1 (MHz)	+ N2	fvCO2 (MHz)	fvco1 (MHz)	
	396 "A" 397	3.9996 "B" 4.0097	400 399	4.0000 3.9900	7.9996 7.9997	
	495	4.9995	301	3.0100	8.0095	
LISI	, A.	.″B″	401	4.0100 4.0000	8.0096 8.0097	ATAC TIS-
	HALLON MODILATION THAT	1	19 kiss my 302 mau	3.0200 V		The MC14514
	4	1	402	4.0200	8.0196	ns from More
	B AA"AG TIB	"B"	"C" 401	"D" 4.0100	0.0137	rallel and 4-bit dual-modulus
		1	303	3.0300	8.0295	
			th strobe and ad-	w , jugai rid it s yi		The MC14514
			e oscillator 12-bit	nsist of a relerence		
			1500	15.0000	19.9995	grammabla n ble divide by-
	A	1	1600	16.0000	19.9996	th circuitry for
	"A"	"B"	1599	15.9900	19.9997	p filter and V
	200		1501	15.0100	20.0095	ns for a PLL fancy limit. For
	1585	16.0085	e VCO and the	used between the	20.0085	aulubom is
	"E" 1586	"F" 16.0186			20.0086	
00	″E″ 1586	17.0084			1	General Purpi
P SUPRIX PLASTIC PACKAGE CASE 738	1684			TV Tuning Scarning Rec Amateur Radii	20.0184	
P SUFFIX PLASTIC PACKAGE CASE 738	1684 "E"	17.0084			20.0184 20.0185 20.0186	General Purpi CATV AM/FM Re Two Way F
P SUFFIX PLASTIC PACKAGE CASE 738 UMENT	1684 "E"	17.0084		Amareur Radii	20.0184 20.0185 20.0186 20.0284 Increasing	General Purpo CATV AM/FM Ra Two Way I Low Power D 3.0 to 8.0 Vds
P SUFFIX PLASTIC PACKAGE CASE 738 MAENT 20 102	1684 "E" 3840	17.0084	"ç"	Ama eur Radii "O"	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps	General Purpo CATV AM/FM Ra Two Way I Low Power D 3.0 to 8.0 Vdd > 30 MHz Ty
P SUFFIX PLASTIC PACKAGE CASE 738 MENT 20102	1684 "E" 384	17.0084	"ç"	Amajour Radii "O" Ilty @5 \ do ir for Values Betw	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084	General Purpo CATV AM/FM Rd Two Way I Low Power D 3.0 to 8.0 Vdd > 30 MHz Ty Programmabli
P SUFFIX PLASTIC PACKAGE CASE 738 WHENT 20102 19003	1684	17.0084	"ç"	Ama eur Radii "O"	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085	General Purp CATV AM/FM Ra Two Way I 3.0 to 9.0 Vds > 30 MHz Ty Programmabli On- or Off-Cr
P SUFFIX PLASTIC PACKAGE CASE 738 MENT 20102 19103 18016	1684 "E"	17.0084	"ç"	Amaleur Radii "O" "O" for Velus Between for Velus Between for Velus Between for Velus Between for Cogramm for Cogr	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085 32.0086	General Purp CATV AM/FM Re Two Way I 3.0 to 9.0 Vdi >30 MHz Ty Programmabli On- or Off-Cr Dual Modulus
P SUFFIX CASE 738 WEENT 20102 19003	1684	17.0084	"ç"	Ama Bur Radia "O" Ity @6 \ do It for Values Betw Ilator Operation	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085 32.0086	General Purp CATY AM/FM Two Way I 30 to 9.0 Vdi 230 to 9.0 Vdi Programmabl On- or Off-CI - W Range= + N Range=
P SUFFIX PLASTIC PACKAGE CASE 738 MENT 20102 19103 18016	1684 "E"	17.0084	"ç"	Amaleur Radii "O" "O" Ility @5 \ do In for Velusa Betwa Ilator Operation rogramming	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085 32.0086	General Purpl CATY AM/FIN AM/FIN Two Way I 3.0 to 9.0 Vol Low Power E > 30 MHz Tyl On- or Off-CI Puglal Modulus + N Range= "Linearized" "Linearized"
P SUFFIX CASE 738 CASE 738 CASE 738 19 D02 19 D03 17 D48 16 J 17	1684 "E" 287 38 30 30 40 40 40 40 40 40 40 40 40 40 40 40 40	17.0084	"ç"	Amaleur Radii "O" "O" Ility @5 \ do In for Velusa Betwa Ilator Operation rogramming	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085 32.0086 32.0184	General Purp CATV AM/FR Two Way I Two Way I 3.0 to 8.0 Vol Low Power I > 30 MHz Ty - 30 MHz Ty Programmabl On- or Off-Ci Dual Modulus + N Range=: "Linearized"
P SUFFIX CASE 738 CASE 738 CASE 738 19 D02 19 D03 10 D4 16 D4 16 D4 16 D4 16 D4	1684 "E" DAY DIMA "E" DAY DAY DAY DIMA "E" DAY	17.0084	"ç"	Amaleur Radii "O" "O" Ility @5 \ do In for Velusa Betwa Ilator Operation rogramming	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085 32.0086 32.0184	General Purp CATV AM/FM Re AM/FM Re 3.0 to 9.0 Vd. Low Power D Programmabl On- or Off-CF Dual Modulus "Linearize" "Linearize" Two Error Sig Two Error Sig
P SUFFIX PLASTIC PACKAGE CASE 738 QMENT 20 102 19 102 17 19 64 16 19 99 16 19 99 16 19 19 16 19 16 19 17 19 60 16 19 17 19 60 16 19 17 19 60 18 19 18	1684 "E" DAY DIMA "E" DAY	17.0084	"ç"	Amaleur Radii "O" "O" Ility @5 \ do In for Velusa Betwa Ilator Operation rogramming	20.0184 20.0185 20.0186 20.0284 Increasing In 100 Hz Steps 32.0084 32.0085 32.0086 32.0184	General Purp CATV AM/FM Re AM/FM Re 3.0 to 9.0 Vd. Low Power D Programmabl On- or Off-CF Dual Modulus "Linearize" "Linearize" Two Error Sig Two Error Sig



CALCALUA

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

The MC145146 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

The MC145146 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit divide-by-A counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145146 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and the MC145146

General Purpose Applications

CATV AM/FM Radios Two Way Radios TV Tuning Scanning Receivers Amateur Radio

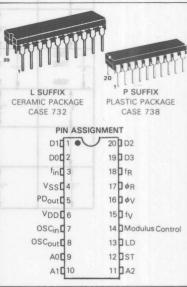
Low Power Drain

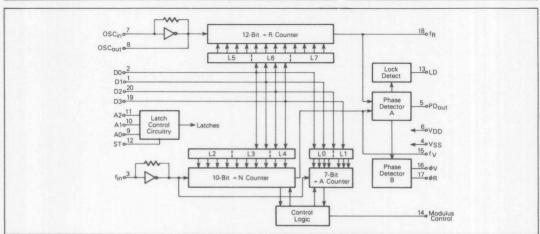
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @5 Vdc
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Dual Modulus 4-Bit Data Bus Programming
- + N Range = 3 to 1023, + A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options Single Ended (Three State) Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER





ADI-837

MAXIMUM RATINGS (Voltages Referenced to VSS)

estinul xell gyT mild ggV led Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to + 10	Vdc
Input Voltage, All Inputs	V _{in}	-0.5 to VDD+0.5	Vdc
DC Current Drain Per Pin		10	mA
DC Current Drain VDD or VSS Pins	1	30	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

		Charac	toriotio				Symbol	V	Tlo	w		25°C		Thi	igh	Units
		Charac	teristic				Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Units
Power Supply Volt	age F	Range	1 6				V _{DD}	-	3	9	3	_	9	3	9	Vdc
Output Voltage	0	91	8			01 1		3	_	0.05	-	0	0.05	_	0.05	Setup
V _{in} = V _{DD} or 0		0.5				0 Level	VOL	5	-	0.05	-	0	0.05	-	0.05	Date
viu = ADD or o								9	-	0.05	-	0	0.05	-	0.05	
								3	2.95	-	2.95	3	_	2.95	-	Vdc
Vin = or VDD						1 Level	Vон	5	4.95	-	4.95	5	-	4.95	01 8800	bbA.
								9	8.95	-	8.95	9	_	8.95	-	
Input Voltage	61	0.6	1 6			0 Level									8/110	L ploit
$V_0 = 2.5 \text{ or } 0.5$							VIL	3	-	0.9	-	1.35	0.9	or-see	0.9	Date
$V_0 = 4.5 \text{ or } 0.5$							VIL.	5	-	1.5		2.75	1.5	-	1.5	
$V_0 = 8.5 \text{ or } 1.5$								9	-	2.7	_	4.05	2.7	rithiW.	2.7	Vdc
$V_0 = 0.5 \text{ or } 2.5$						1 Level		3	2.10	-	2.10	1.65	-	2.10	NV_V4	. 用象
$V_0 = 0.5 \text{ or } 4.5$							VIH	5	3.5	-	3.5	2.75	-	3.5	fliw e	Pha
$V_0 = 1.5 \text{ or } 8.5$	-		1 6	1 40	ert.			9	6.3	-	6.3	4.95	agmi	6.3	no Ball	Tugn!
Output Current						Source									nit in	080
$V_{OH} = 2.7$								3	-0.44	-	-0.35	-0.66	-	-0.22	-	
V _{OH} = 4.6							ЮН	5 9	-0.64	-	-0.51	-0.88	-	-0.36	/ eglu!	t summal
V _{OH} =8.5			8						-1.3	-	-1.0	-1.3	-	-0.7	=	mAdc
V _{OL} = 0.3				1		Sink	-	3	0.44	-	0.35	0.66	-	0.22	- 100	
$V_{OL} = 0.4$							IOL	5	0.65	-	0.51	0.88	-	0.36	-	
$V_{OL} = 0.5$								9	1.3	-	1.0	1.3	nān.	0.7	- Tan	lanna
Output Current Mo	dulus	Control				Source	-	-		-	-	NY T SOURTER S	Sections	NI NO. 1	OFILE	PARMET
V _{OH} = 2.7							ЮН	3	0.15	-	0.25	0.5	-	0.08	-	mAdc
V _{OH} = 4.6							-On	5	0.45	-	0.75	1.5	-	0.23	-	MAGC
V _{OH} =8.5						1 3		9	0.75	-	1.25	2.5	-	0.38	u. PSu	resease
V _{OL} = 0.3						Sink	xem,	3	0.48	ENA D	0.8	1.6	-	0.24	- 0	mA
V _{OL} = 0.4							IOL	5	0.90	-	1.5	3	-	0.45	-	
V _{OL} = 0.5	0			H		8		9	2.10	sv¥ n	3.5	7	-	1.05	-	
Input Current						er Inputs	IIL	9	-	±0.3	-	±00001	±0.1	-	±1.0	
					fin	, OSCin	111	9	-	± 15	-	±5	±10	-	±8	uAdc
		15 8				, OSCin	ЛН	9	-	± 15	-	±5	±10	coulents	±8	-
	1 9	1 00		101	Othe	er Inputs	X IH	9	BOA BY	±0.3	= 100	±0.00001	±0.1	-	± 1.0	rti(
Input Capacitance		30		10			Cin	3-9	-	10	-	6	10	-	10	pF
Output Capacitano	е	01		101		2	Cout	3-9	-	10	-100	6	10	-	10	pF
1 81 -	1 8	18		21		0	AMIL .	3	-	800	-	200	800	-	1600	
Quiescent Current							IDD	5	-	1200	-	300	1200	-	2400	μAdc
						9	-	1600	-	400	1600	-	3200	- =wc		
3-State Leakage Cu	rrent		7			PDout	IIL	9	-	±0.1	-	± 0.00001	±0.1	-	±3.0	μAdc

NOTE: T_{low}= -40°C T_{high}=85°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Thigh=85°C

MAXIMUM RATINGS (Voltages Referenced to VSS)

SWITCHING CHARACTERISTICS (TA = 25 °C, CL = 50 pF)

Output Rise Time	-	100	200	das or
Output Fall Time		50		
Output Fall Time	-		100	ns
Output Fall Time tTHL 5 9 Propagation Delay Time tPLH 5 9 Clock to Modulus Control 3 3 TPHL 5 9 Setup Times Data to ST 5 5 9 9 9 15 15 15 15 15 15 15 15 15 15 15 15 15		40	80	muD DC
Propagation Delay Time Clock to Modulus Control 2 3 3 TPHL 5 9 Setup Times Data to ST	Vas Pins	100	200	muD DO
Propagation Delay Time Clock to Modulus Control 2 2 wolf 3 TPHL 5 9 Setup Times Data to ST 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		50	100	ns
Propagation Delay Time Clock to Modulus Control 2 2 3 TPHL 5 Setup Times Data to ST 3 3 Tsu 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	-	40	60	-
Propagation Delay Time Clock to Modulus Control 2 2 3 TPHL 5 Setup Times Data to ST 3 3 Itsu 5 3		80	160	
Temporary Temp		50 30	100	ns
TPHL 5 1 1 1 1 1 1 1 1 1	traingroppiers	80	160	
Setup Times	ALEGNA ACTION A	50	100	ns
Setup Times	Tepi	30	60	Jawes St
Data to ST = 80.0 0 = 80.0 = 8 10V tsu 5	10	0	-	
		0	eparlo	ns
	10	0	010-00	A E WA
3 296 - 296 3 - 296 - Volc		60	-	
Address to ST a aga _ aga a HoV lave_11 tsu 5		30	adv s	ns
30.0 0 30.0 30.0 9		18	-	
Hold Time 1 1 1 2 3		15	TO(a)	loV rug
Data, Address to ST 0 122 1 1 1 1 5		10	80 0 8.	ns
31 31 31 31 31 31 31 31	-	10	80108	-
Output Pulse Width 7.5 80 4 - 7.5 - 9		120	170	100
φR, φV with fR in aa r or s = or s s lovad t tWH(φ) 5		100	150	ns
Phase with fy g		80	130	0=0V
Input Rise and Fall Times CEA C.B 5 5 5 5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		-	5 5	-
OSCia fia		-	1/4/10	Pool
- 122.0-1 - 100.0-100.0-1 - 100.0-1 - 100.0-1	_	+-	2 5	-
Input Pulse Width		30	20.7	1
OSCin, fin, Strobe		20 15	3.8	ns
- 860 - 880 160 - 600 8 101	25			

FREQUENCY CHARACTERISTICS

		80.0		Characteri	etic	1 _ 1	0.15	0	Symbol	VDD	TI	ow		25°C		Th	igh	Units
mAdc				Characteri	200				Symbol	ADD	Min	Max	Min	Тур	Max	Min	Max	Ollic
Opera	ting Fre	quency	/	2.5	1.25	1-1	0.75	6		3	-	17	-	27	14	-	12	HOY
OSC	Cin _	0.24		a.r T	nput=	SQ Way	e VDD	-Vss	fmax	5	-	33	-	55	27	-	21	MH
									101	9	-	35	-	65	35	-	33	Insv
				7 1	nput=	Sin Wav		mV ptp	1	3	-	11	-	21	10	-	9	IOV
			± 0.1						fmax	5	нето	20	-	34	17	-	15	МН
									JII I	9	-	17	-	34	17	-	15	
Opera	ting Fre	quency	1	2.1		20		0		3	-	9	-	15	8	-	7	
fin				romm o 1	nput=	SQ Way	e VDI	-Vss	fmax	5	100	19	-	30	15	-	15	MH
								0.0		9	-	31	-	52	26	-	22	1
				- 1	nput=	Sin Way	e 500	mV ptp	The T	3	-	10	-	15	7	-	6	
								8.6	fmax	5		18		31	15	Dance	15	МН
									IIIUA	9	-	21	-	31	15	-	15	
ow= -	-40°C	-	1600	006	1	1800		8	00							ZITOT	April 1110	Justin
high=																		

This device contains choultry to pretect the inputs against damage due to high static voltages or alsoring fromewar, it is advised that normal precausers be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{\rm in}$ and $V_{\rm out}$ be constrained to the range VSS $\leq V_{\rm in}$ or $V_{\rm out} \simeq V_{\rm DO}$.

Unused mouts always be tied to an appropriate logic voltage level (e.g., either VSS or $V_{\rm OO}$).

DATA INPUTS (Pins 2, 1, 20, 19) — Information at these wou — inputs is transferred to the internal latches when the ST input is in the high state. Pin 19 (D3) is most significant.

 f_{in} (Pin 3) — Input to +N portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels), DC coupling may be used.

Vss (Pin 4) - Circuit Ground.

PD_{out} (Pin 5) — Three-state output of phase detector for use as loop error signal.

Frequency fy > fR or fy Leading: Negative Pulses. Frequency fy < fR or fy Lagging: Positive Pulses. Frequency fy = fR and Phase Coincidence: High-Impedance State.

VDD (Pin 6) - Positive power supply.

OSC_{in}, OSC_{out} (Pins 7 and 8) — These pins form an onchip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 9, 10, 11) — A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	+ A Bits	0	1	2	3
0	0	1	Latch 1	+ A Bits	4	5	6	
0	1	0	Latch 2	+ N Bits	0	1	2	3
0	1	1	Latch 3	+ N Bits	4	5	6	7
1	0	0	Latch 4	+ N Bits	8	9	_	-
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST (Pin 12) — When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low,

will latch that information. When high, any changes in the data information will be transferred into the latches.

LD (Pin 13) — Lock detector signal. High level when loop is locked (fg, fv of same phase and frequency). Pulses low when loop is out of lock.

MODULUS CONTROL (Pin 14) - Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the + A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N-A additional counts since both + N and + A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (NT) = N P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the + A counter.

 $f_V\,(Pin\,15)$ — This is the output of the $+\,N$ counter that is internally connected to the phase detector input. With this output available, the $+\,N$ counter can be used independently.

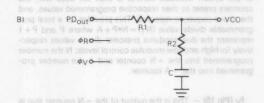
 $\phi_V,\,\phi_R$ (Pins 16 and 17) - These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_out).

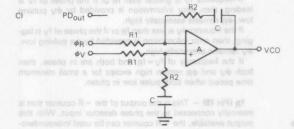
If frequency fy is greater than fR or if the phase of fy is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frquency fy is less than fR or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

 f_R (Pin 18) — This is the output of the +R counter that is internally connected to the phase detector input. With this output available, the $\mp R$ counter can be used independently.





$$\omega_N = \sqrt{\frac{\kappa_\phi \kappa_{VCO}}{\kappa_{R1C}}}$$

F(s) =
$$\frac{1}{RICS + 1}$$
 January one set $\frac{1}{RICS + 1}$ January one good as extraction of the second of the seco

$$\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NC(R1 + R2)}}$$

$$\zeta = 0.5 \,\omega_{\text{N}} \,(\text{R2C} + \text{N/K}_{\phi}\text{K}_{\text{VCO}})$$

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

KøKVCO wN =

$$\zeta = \frac{\omega_{NR20}}{2}$$

Assuming gain A is very large, then:

NCR1

NOTE: Sometimes R1 is split into two series resistors each R1+2. A capacitor CC is then placed from the midpoint to ground to further filter ϕ_V and ΦR. The value for Co should be such that the corner frequency of this network does not significantly affect ωN.

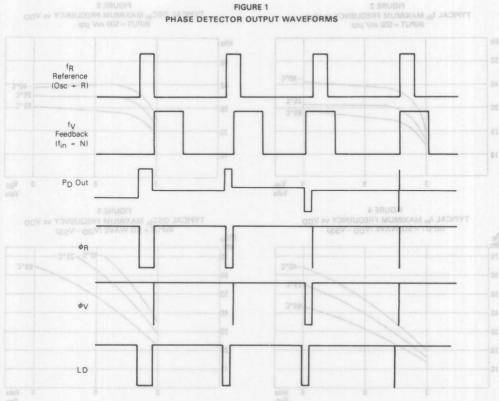
DEFINITIONS: N = Total Division Ratio in feedback loop

 $K_{\phi} = V_{DD}/4\pi$ for PD_{out} $K_{\phi} = V_{DD}/2\pi$ for ϕ_{V} and ϕ_{R}

 $K_{VCO} = \frac{2\pi\Delta f_{VCO}}{2\pi\Delta f_{VCO}}$ ΔVVCO

for a typical design $\omega_N \cong (2\pi/10) f_\Gamma$ (at phase detector input) \$ ≅ 1

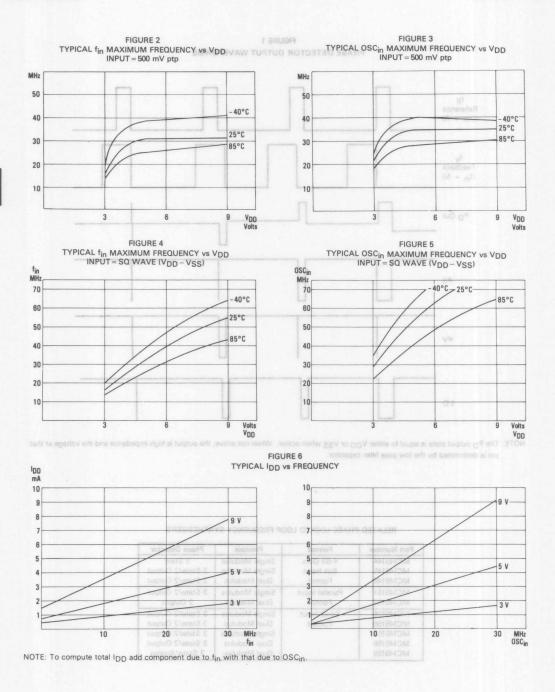




NOTE: The PD output state is equal to either VDD or VSS when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

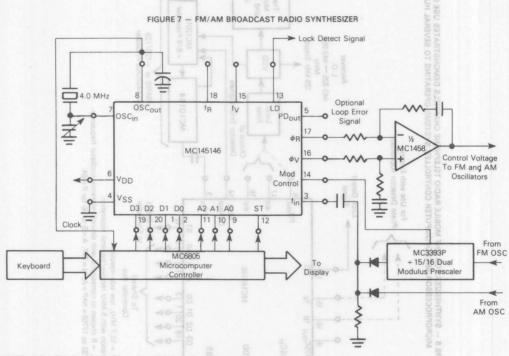
Part Number	Format	Prescale	Phase Detector
MC145144	4-Bit Data	Single Modulus	3 State
MC145145	Bus Input	Single Modulus	3 State/2 Output
MC145146	Format	Dual Modulus	3 State/2 Output
MC145151	Parallel Input	Single Modulus	3 State/2 Output
MC145152	Format	Dual Modulus	2 Output
MC145155	Serial Input	Single Modulus	3 State/2 Output
MC145156	Format	Dual Modulus	3 State/2 Output
MC145157		Single Modulus	3 State/2 Output
MC145158		Dual Modulus	3 State/2 Output
MC145159		Dual Modulus	3 State/Analog



APPLICATIONS

The features of the MC145146 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The device architecture allows the user to establish any integer reference divide value between 3 and 4096. The wide selection of ÷ R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a microprocessor system clock. Typical applications that takes advantage of these MC145146 features including the dual modulus capability are shown in Figures 7, 8 and 9.

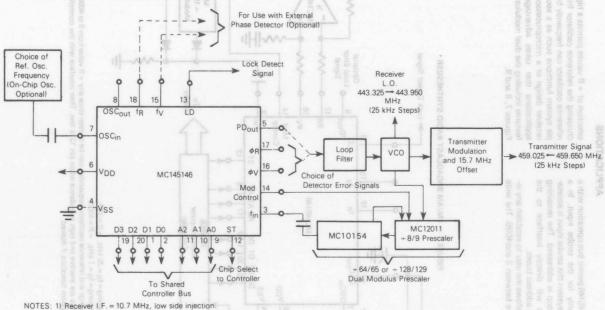


NOTES: 1) For FM: Channel spacing = $f_R = 25 \text{ kHz}$, + R = 160.

For AM: Channel spacing = f_R = 1 kHz, + R = 4000.

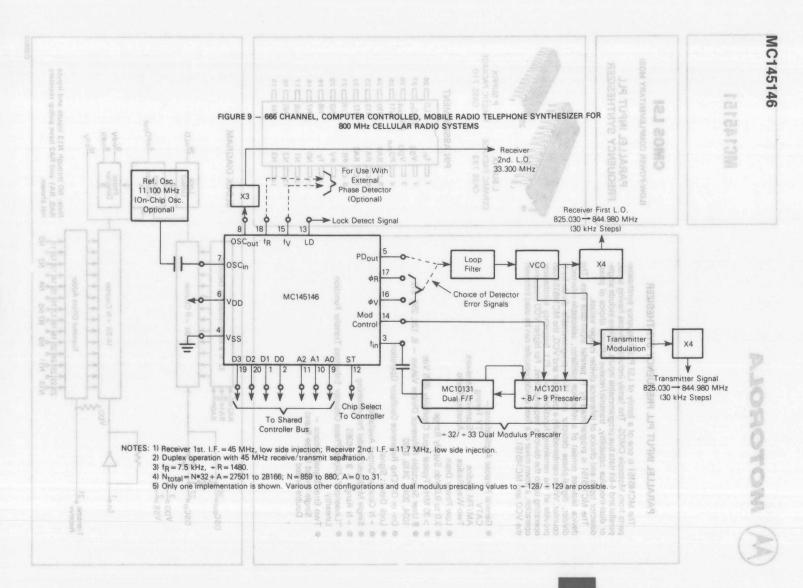
2) Various channel spacings and reference oscillator frequencies can be chosen since any + R value from 3 to 4096 can be established. 3) Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.





- 2) Duplex operation with 5 MHz receive/transmit separation.
- 3) f_R = 25 kHz, + R chosen to correspond with desired reference oscillator frequency.
- 4) N_{total} = 17733 to 17758 = N•P + A; N = 277, A = 5 to 30 for P = 64.





MC145151

2

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

The MC145151 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

The MC145151 is programmed by 14 parallel input-data lines. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector and 14-bit programmable divide-by-N counter. When combined with a loop filter and VCO, the MC145151 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145151.

- General Purpose Applications —
 CATV TV Tuning
 AM/FM Radios Scanning Receivers
 Two-Way Radios Amateur Radio

 Amateur Radio
 Two-Way Radios Amateur Radio

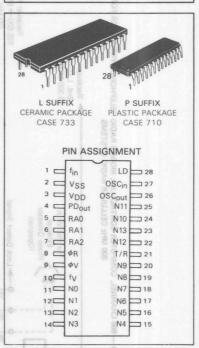
 Output

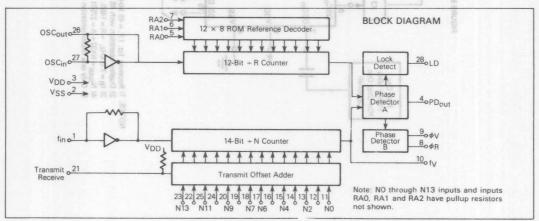
 Description:
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values 8, 128, 256, 512 1024, 2048, 2410, 8192
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- + N Counter Output Available
- Single Modulus/Parallel Programming
- + N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options Single Ended (Three-State) Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER





MAXIMUM RATINGS (Voltages Referenced to Vss)

etial xeM Rating aiM go	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to +10	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain Per Pin	1	10	mA
DC Current Drain VDD or VSS Pins	India.	30	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{sta}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	VDD	TL	.ow	-	25°C		TH	Units	
Characteristic	Symbol	ADD	Min	Max	Min	Тур	Max	Min	Max	Units
Power Supply Voltage Range	VDD	-	3	9	3	-	9	3	9	Vdc
Output Voltage 0 Lev	el	3	_	0.05	_	0	0.05	MAIN	0.05	DEPART.
Vin = VDD or 0 well	VOL	5 9	=	0.05 0.05	-	0 0	0.05 0.05	_	0.05	Vdc
	3 1	3	2.95	-	2.95	3	-	2.95	pen T gni	Vac
V _{in} = 0 or V _{DD}	el VOH	9	4.95 8.95	GGA an	4.95 8.95	9	_	4.95 8.95		oso
Input Voltage 0 Lev	el		qtq Vr	1 000 evi	Win2	tugnl				
Vo = 25 or 05	VIL	3	-	0.9	-	1.35	0.9	-	0.9	
V _O = 4.5 or 0.5		5	-	1.5	-	2.75	1.5		1.5	
VO = 8.5 or 1.5	- 18	9	-	2.7	-	4.05	2.7	<u>vo</u> neu	2.7	Vdc
V _O = 0.5 or 2.5	el	3	2.10	DGA SA	2.10	1.65	-	2.10	_	ni
V _O = 0.5 or 4.5	VIH	5	3.5	o 000 ev	3.5	2.75	-	3.5	-	
VO = 1.5 or 8.5	0	9	6.3	000 000	6.3	4.95	-	6.3	-	
Output Current Source	e	Xetty								
V _{OH} = 2.7 V _{OH} = 4.6	Іон	3 5	-0.44 -0.64	_	-0.35 -0.51	-0.66 -0.88	-	-0.22 -0.36	-40°C	= wol
$V_{OH} = 8.5$		9	-1.3	-	-1.0	-1.3	-	-0.7		mAd
$V_{OL} = 0.3$ Sir		3 5	0.44	-	0.35	0.66	-	0.22	-	
$V_{OL} = 0.4$ $V_{OL} = 0.5$	IOL	9	1.3	_	1.0	1.3	_	0.36	_	
Input Current Other Inpu	ie i	9	-	- 60	1.0	- 25	-50	-	- 35	
f _{in} , OSC		9	_	± 15	-	±5	± 10	- 1	±8	μAde
f _{in} , OSC Other Inpu	n lu	9	-	± 15 ± 0.3		±5 ±0.00001	±10 ±0.1	-	±8 ±1.0	
Input Capacitance	Cin	3-9	-	10	-	6	10	-	10	pF
Output Capacitance	Cout	3-9	-	10	-	6	10	-	10	pF
Quiescent Current	Out	3	-	800	7	200	800	-	1600	
	IDD	5	-	1200	-	300	1200	- 1	2400	μAd
		9	-	1600	-	400	1600	-	3200	
Three-State Leakage Current PD _{OI}	it IL	9	-	±0.1	-	±0.0001	±0.1	-	±3.0	μAdo

NOTE: T_{low} = -40°C T_{high} = 85°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

SWITCHING CHARACTERISTICS (TA = 25 °C, C1 = 50 pF)

	Characteristic	find.	SulteV	Symbol	VDD	Min	Тур	Max	Units
		Vdc	01 + or d.0 -	Monte	3	-	100	200	12.00
Output Rise Time				TLH	5	-	50	100	ns
		304	ana GGA of on-	- 181×	9	- 1	40	80	Judiu
		Am	01		3	_ 0	100	200	BD DG
Output Fall Time				THL	5	as¥ 16	50	100	ns
				Ta I	9	ecosil	40	80	Гезезо
Output Pulse Width		59	- 65 to + 160	1 7	3	70	120	170	Storad
φ _R , φ _V with f _R in				tWH(ø)	5	50	100	150	ns
Phase with fy					9	30	80	130	
In the Property of the Propert				1	3	-	-	5	
Input Rise and Fall Times				tTLH	5	-	-	4	μS
OSC _{in} , f _{in}				tTHL	9	-	-	2	
In a Date of Michigan					3	40	30	D.JADI	1700.
Input Pulse Width				tw	5	35	20	-	ns
OSC _{in} , f _{in}					9	25	15	-	

The second second second second			
FREQUENCY	CHADACT	TOIGT	100
FREQUENCT	LHARALI	EDIST	163

			80 Cha	racteristic			Symbol	V	Tic	w		25°C		Th	igh	Units
80.0		1 - 1	ao Chai	aracteristic		Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Office	
Operati	ng Fred	quency	-	8 8	- 2.9	2.95	8	3	-	17	-	27	14	-	12	
OSC	in _			Input = S	Q Wave VDD	y-Vss	fmax	5 9	ievis)	33 35	-	55 65	27 35	odij n	33	MHz
				Input = Si	in Wave 500	mV ptp		3	ITV0.	11	-	21	10	- 0	9	fuisió)
							fmax	5	-	20 17	_	34 34	17 17	8.070	15 15	MH
Operati	ng Fred	quency	2.7	4,05	27		.0	3	-	9	-	15	8	0.170	7_	by.
fin				Input = S	Q Wave VDD)-VSS	fmax	5	leve.	19	_	30 52	15 26	0.2.5	15	MHz
				Input = Si	in Wave 500	mV ptp	,0	3	-	10	-	15	7 15	3.8 1g	6	МН
							¹ max	5 9	60100	18 21	_	31	15	100	15	QUO.

							9	- 21 -	31 15 - 15
T _{low} = Thigh =	– 40°C 85°C	-0.28 -0.38 -0.7	-0.88 -0.88 -1.3	-0.51 -1.0	-0.64	8	HOL		VOH = AB VOH = B.5
									Quiescent Current

his device contains circuity to protect the rights against dringer due to tipe state vortages or excuts tress, in success or example of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it second rate V_{int} and V_{int} be constrained to the range V_{int} or V_{int} is V_{int} and V_{int} be that V_{int} be constrained to an appropriate logic voltage level (a., either VSS or VDD).

PIN DESCRIPTIONS

f_{in} (Pin 1) − Input to +N portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 9. For larger amplitude signals (standard CMOS Logic levels) DC coupling may be used.

Vss (Pin 2) - Circuit Ground.

Vnn (Pin 3) - Positive power supply.

PD_{out} (Pin 4) — Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency fy > fR or fy Leading: Negative Pulses Frequency fy < fR or fy Lagging: Positive Pulses
Frequency fy < fR and Phase Coincidence: High-Impedance State.

RAO, RA1, RA2 (Pins 5, 6, and 7) - These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Refe	rence Ad Code	dress	Total Divide
RA2	RA1	RA0	Value
0	0	0	8
0	0	1	128
0	.1	0	256
0	1	1 1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

ΦR, ΦV (Pins 8 and 9) - These phase detector outputs

φ_R, φ_V (Pins 8 and 9) — These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{Out}). If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by φ_V pulsing low. or remains essentially high.

If the frequency fy is less than fR or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing

low, ϕ_V remains essentially high. If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

fy (Pin 10) - This is the output of the + N counter that is internally connected to the phase detector input. With this output available, the + N counter can be used independent-

N Inputs (Pins 11 to 20 and 22 to 25) - These inputs provide the data that is preset into the +N counter when it reaches the count of zero. NO is least significant and N13 is most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

Transmit/Receive (Pin 21) - This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pullup resistor ensures that no connection will appear as a logic one causing no offset addition.

OSCout, OSCin (Pins 26 and 27) - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSCin to ground and OSCout to ground. OSCin may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode. no connection is required to OSCout.

LD (Pin 28) - Lock detector signal. High level when loop is locked (fg, fy of same phase and frequency). Pulses low when loop is out of lock.

If the frequency by is less than fix or if the phase of by is lagging, then error information is provided by en puising low, ey remains assentially high.

If the frequency of type and both areas phase, then A) PD_{out} time period where the purple of the end of t fy (Pin 10) — Inja is the output of the ~ N counter that is internelly connected to the phase demonstrating. With this dutout available, the + N counter can be used independent-

violation entre de la contraction de la contract

to the IF frequency of the transcaiver. We affect is fixed at \$55 when 1/R T and gives no offset when 1/R is high. A pullup resistor Turns that no connection will appear as a logic one causing no offset addition.

fin (Pin 1) — Input to +N portion of synthesizer, fin is rypically derived from loop VCO and is AC coupled into Pin 8. For larger amplitude signals (standard CMOS Logic levels) DC coupling may be used.

$$\omega_{\text{N}} = \sqrt{\frac{K_{\phi} K_{\text{VCO}}}{\text{NR1C}}}$$
 so so year grillions 3

\$ = 0.5 ωN (N/KoKVCO)

$$\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NC(R1 + R2)}}$$

$$S = 0.5 \omega_{N} (R2C + N/K_{\phi}K_{VCO})$$

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

This signal will typically be AC coupled to OSC_{Int} but for larger amplited signals (standard CMOS-logic levels) DC C) PDout O PDout O ired to OSCout-R1 gool nerfly level of R O In Man O VCO Vo vo cy) Pulses low ₹R2

$$\omega_{N} = \sqrt{\frac{K_{\phi} K_{VCO}}{NCR1}}$$

$$\xi = \frac{\omega_{N}R2C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R2CS + 1}{R1CS}$$

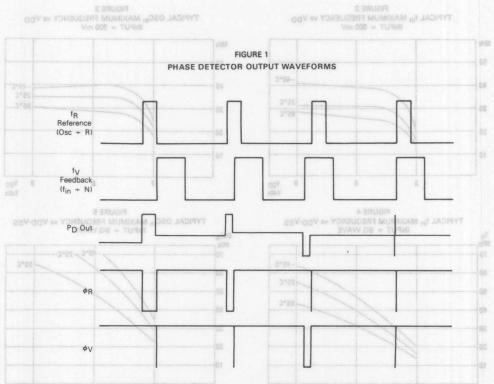
NOTE: Sometimes R1 is split into two series resistors each R1+2. A capacitor CC is then placed from the midpoint to ground to further filter ϕ_V and ΦR. The value for C_C should be such that the corner frequency of this network does not significantly affect ωN.

> DEFINITIONS: N = Total Division Ratio in feedback loop $K_{\phi} = V_{DD}/4\pi$ for PD_{out} $K_{\phi} = V_{DD}/2\pi$ for ϕ_V and ϕ_R

 $K_{VCO} = \frac{2\pi\Delta f_{VCO}}{2\pi\Delta f_{VCO}}$

Δ٧٧٢Ο

for a typical design $\omega_N \cong (2\pi/10) f_r$ (at phase detector input) 5 = 1

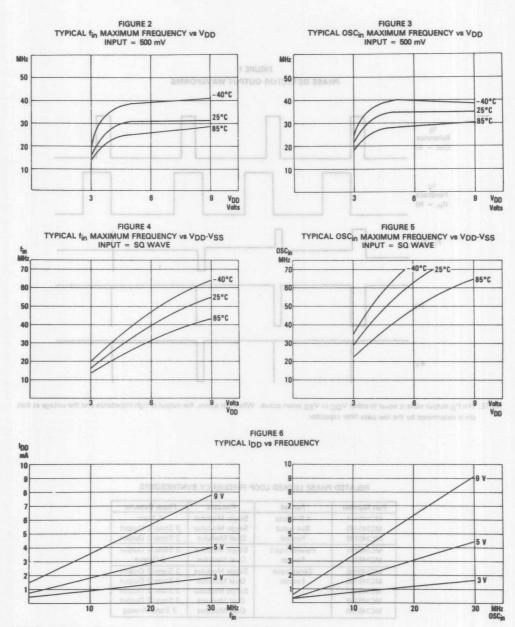


NOTE: The PD output state is equal to either VDD or VSS when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

TYPICAL IDD VS PREQUENCY

RELATED	THASE LUCKED LU	OP FREQUENCY SY	NIFESIZENS	
Part Number	Format	Prescale	Phase Detector	
MC145144 MC145145	4-Bit Data Bus Input	Single Modulus Single Modulus	3 State 3 State/2 Output	
MC145146	Format	Dual Modulus	3 State/2 Output	
MC145151 MC145152	Parallel Input Format	Single Modulus Dual Modulus	3 State/2 Output 2 Output	
MC145155	Serial Input	Single Modulus	3 State/2 Output	

NOTE: To compute total 100 add component due to fit with that due to OSCin.



NOTE: To compute total I_{DD} add component due to f_{in} with that due to OSC_{in} .

MOTOROLA

FIGURE 7 - 5 MHz TO 5.5 MHz LOCAL OSCILLATOR CHANNEL SPACING = 1 kHz

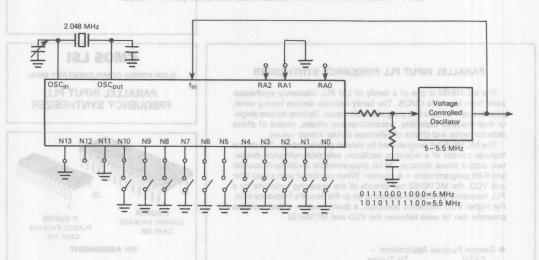
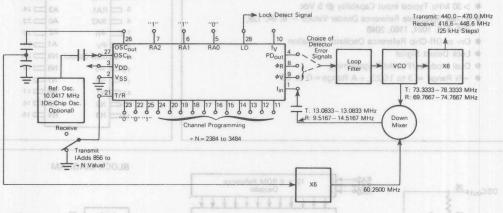


FIGURE 8 - SYNTHESIZER FOR LAND MOBILE RADIO UHF BANDS A VIOLET SHOW OF OF OR O



- IOTES:

 1) fig = 4.1667 kHz, + R = 2410, 21.4 MHz low side injection during receive

 2) MC145151 current drain ≅ 5 mA for Vpp = 5 Vdc

 3) Frequency values shown are for the 440 470 MHz band. Similar implementation applies to the 406 441 MHz band. For 470 512 MHz, consider refer ence oscillator frequency X9 for mixer injection signal (90.3750 MHz)



MC145152

ICTA5151

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER

The MC145152 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, perallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

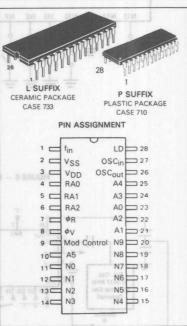
The MC145152 is programmed by sixteen parallel inputs. The device features consist of a reference oscillator, selectable-reference divider, two output phase detector, 10-bit programmable divide-by-N counter and 6-bit programmable + A counter. When combined with a loop filter and VCO, the MC145152 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145152.

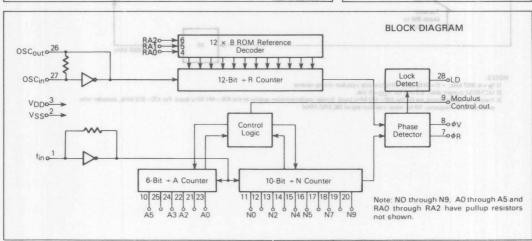
- General Purpose Applications —
 CATV TV Tuning
 AM/FM Radios Scanning Receivers
 Two-Way Radios Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values 8, 64, 128, 256, 512, 1024, 1160, 2048
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- + N Range = 3 to 1023, + A Range = 0 to 63

CMOS LSI

(LOW POWER COMPLEMENTARY MOS)

PARALLEL INPUT PLL FREQUENCY SYNTHESIZER





DS9811

Output Rise Time

SWITCHING CHARACTERISTICS ITA = 25°C. CL = 5

MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +10	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain Per Pin	1.6	10	mA
DC Current Drain VDD or VSS Pins	1 8	30	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{sto}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Cho	racteristic			Symbol	VDD	TLO	w		25°C	10111	ТН	igh	Units
en oor Cha	racteristi			Symbol	ADD	Min	Max	Min	Тур	Max	Min	Max	Offics
Power Supply Voltage	Range	70	0	VDD	-	3	9	3	-	9	3	9 0	Vdc
Output Voltage Vin = VDD or 0	100	90	0 Level	V _{OL}	3 5 9	-	0.05 0.05 0.05	=	0 0 0	0.05 0.05 0.05	75 g)	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD}			1 Level	Voн	3 5 9	2.95 4.95 8.95	-	2.95 4.95 8.95	3 5 9	- 8	2.95 4.95 8.95	ise And na An	080
Input Voltage V _O = 2.5 or 0.5 V _O = 4.5 or 0.5 V _O = 8.5 or 1.5	20	35	0 Level	VIL	3 5 9	-	0.9 1.5 2.7		1.35 2.25 4.05	0.9 1.5 2.7		0.9 1.5 2.7	Vdc
V _O = 0.5 or 2.5 V _O = 0.5 or 4.5 V _O = 1.5 or 8.5	02		1 Level	VIH	3 5 9	2.10 3.5 6.3		2.10 3.5 6.3	1.65 2.75 4.95	RSTO - Ones	2.10 3.5 6.3	- -	UDBR
Output Current VOH = 2.7 VOH = 4.6 VOH = 8.5	7 14 5 27 6 35	- 2	Source	loh 8	3 5 9	-0.44 -0.64 -1.3	v –aa	-0.35 -0.51 -1.0	-0.66 -0.88 -1.3	111	-0.22 -0.36 -0.7	per <u>3</u> gr	mAd
V _{OL} = 0.3 V _{OL} = 0.4 V _{OL} = 0.5	1 10 4 17 8 17	E -	Sink	- IOL 8	3 5 9	0.44 0.64 1.3	q \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	0.35 0.51 1.0	0.66 0.88 1.3	-	0.22 0.36 0.7	-	
V _{OH} = 2.7 V _{OH} = 4.6 V _{OH} = 8.5	odulus Co	E	Source	- IOH	3 5 9	0.15 0.45 0.75	v =00	0.25 0.75 1.25	0.5 1.5 2.5		0.08 0.23 0.38	ng Freq	mAd
Input Current	1 15	fi	er Inputs n, OSCin	- 111 3	9	(n)	-60 ±15	_	- 25 ± 5	-50 ±10	_	-35 ±8	μAdd
			n, OSC _{in} er Inputs	IH	9	_	±15 ±0.3	_	±5 ±0.00001	±10 ±0.1	_	±8 ±1.0	= 1910
Input Capacitance				Cin	3-9	-	10	-	6	10	-	10	pF
Output Capacitance				Cout	3-9	-	10	-	6	10	_	10	pF
Quiescent Current				IDD	3 5 9	-	800 1200 1600		200 300 400	800 1200 1600		1600 2400 3200	μAde
3-State Leakage Curre	ent		PDout	IL.	9	-	±0.1	_	±0.0001	±0.1	-	±3.0	μAdd

NOTE: T_{low} = -40°C T_{high} = 85°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range VSS ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

SWITCHING CHARACTERISTICS (TA = 25°C, CL = 50 pF)

	C	haracterist	ic				Symbol	VDD	Min	Тур	Max	Units
					ShV	01+	OF OUR	3	_	100	200	indas:
Output Rise Time							TLH	5 niV	-	50	100	ns
					Am.		01	9	-	40	80	semuji (
							30	3	P09	100	200	minu3
Output Fall Time							THL	5	-	50	100	ns
								9	-	40	80	
				- Lo	X.	1001	07.60-	3		80	160	1. 0/2011
							tPLH	5	-	50	100	ns
Propagation Delay Time	3							9	SENITS.	30	60	DIST
Clock to Modulus Co	ntrol							3	-	80	160	
							tPHL	5	- 1	50	100	ns
Karvi I IIII						101		9	-	30	60	
Output Pulse Width					13		GGY	3	70	120	170	DG 104
ΦR, ΦV with fR in							tWH(ø)	- 5	50	100	150	ns
Phase with fy							100	9	30	80	130	-
Input Rise And Fall Tim	00.0				-	- 1-3		- 3	-	-	5	
	ies						tTLH	5	-	-	4	μS
OSC _{in} , fin	-	- 0	4.85		36	P 0	THL	9	-	-	2	D = U
Innua Dulan Müdah	-		00.0		200	0 5		3	40	30		
Input Pulse Width							tw	5	35	20	_ 00	ns
OSC _{in} , fin							Merch	9	25	15	0.0.10 8	0 0

FREQUENCY CHARACTERISTICS

			Cham	acteristic		Combal	V	T	ow		25°C		Th	igh	Ov
			Chare	acteristic		Symbol	ADD	Min	Max	Min	Тур	Max	Min	Max	Units
Operation	ng Freq	uency		88.6 -	86.0 86	3 -	3	-	17	-	27	14	-	12	inV.
OSCin				Input = S	Q Wave VDD - VSS	fmax	5	DI -	33	-	55	27	- 4	21	MHz
						- 6	9	-	35	-	65	35	-	33	ioV.
				Input = Sir	Wave 500 mV p-p	3 0	3	-	st 11	-	21	10	-	9	You
						fmax	5	1 - 10	20	_	34	17	_	15	MHz
						1 0	9	-	17	-	34	17	-	15	loV.
Operation	ng Freq	uency					3	-	9	- 1	15	8	- 1	7	DODGE.
fin	-			Input = S	Q Wave VDD - VSS	fmax	5	_	19	-	30	15	_	15	MHz
		0.23		8.1	87.0 - 81	B 11 0	9	0 - 1	31	-	52	26	- 1	22	10V
				Input = Sin	Wave 500 mV p - p	9 9	3		10	_	15	7	_	6	10×
				92	- 00-	fmax	5	1 _	18	undtO.	31	15	_	15	MHz
pAde						IIIdx	9		21	In	31	15	_	15	101112

his device contains circulary to protect the inputs against damage due to high static voltages or electric helds; however, it is advised linst norms recentions to taken to avoid application of any voltage higher than maximum rated voltages to this high impredance circuit. For proper operation is recommended that V_{IN} and V_{OR} be constrained to the range VSS $\leq (V_{\rm IN}$ or V_{OR}) $\leq V_{\rm IN}$.

PIN DESCRIPTIONS

fin (Pin 1) - Input to the positive edge triggered + N and + A counters. fin is typically derived from a dual modulus prescaler and is AC coupled into Pin 1. For larger amplitude signals (standard CMOS logic levels) DC coupling may be

Vss (Pin 2) - Circuit Ground.

VDD (Pin 3) - Positive power supply.

RAO, RA1, RA2 (Pins 4, 5, and 6) - These three inputs establish a code defining one of eight possible divide values "for the total reference divider. The total reference divide values, including the +2 block, are as follows:"

Refe	rence Ad Code	dress	Total Divide Value
RA2	RA1	RA0	Divide value
0	0	0	8
0	0	1 1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

φR, φV (Pins 7 and 8) - These phase detector outputs can be combined externally for a loop error signal.

If frequency fy is greater than fR or if the phase of fy is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency of fy is less than fR or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of fy = fR and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MODULUS CONTROL (Pin 9) - Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the + A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the + N counter has counted the rest of the way down from its programmed value (N-A additional counts since both + N and + A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (NT) = NOP + A where P and P+1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the + N counter and A the number programmed into the + A counter.

N INPUTS (Pins 11 through 20) - The N inputs provide the data that is preset into the + N counter when it reaches the count of zero. NO is the least significant digit and N9 is the most significant. Pullup resistors ensure that inputs left open remain at a logic one and require only a SPST switch to alter data to the zero state.

A INPUTS (Pins 23, 21, 22, 24, 25, 10) - The A inputs define the number of clock cycles of fin that require a logic zero on the modulus control output. See page 8 for explaination of dual modulus prescaling. The A inputs all have internal pullup resistors that ensure that inputs left open will remain at a logic one.

OSCout, OSCin (Pins 26 and 27) - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSCin to ground and OSCout to ground. OSCin may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSCin, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSCout.

LD (Pin 28) - Lock detector signal. High level when loop is locked (fR, fy of same phase and frequency). Pulses low when loop is out of lock.

PHASE LOCKED LOOP - LOW PASS FILTER DESIGN

$$\phi_{R} \circ \phi_{V} \circ \phi_{V$$

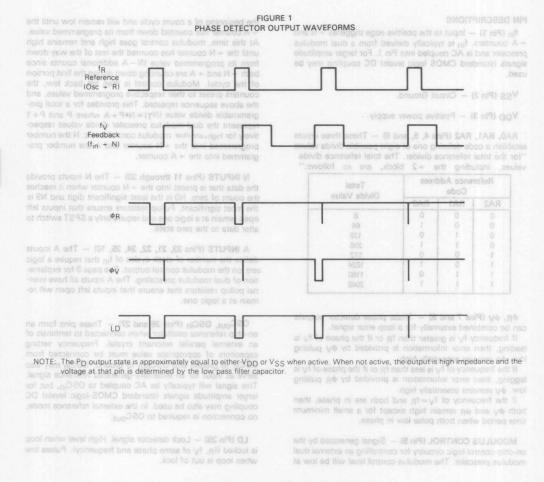
NOTE. Sometimes R1 is split into two series resistors each R1 + 2 A capacitor CC is then placed from the midpoint to ground to further filter by and bR. The value for CC should be such that the corner frequency of this network does not significantly affect ωN.

DEFINITIONS: N = Total Division Ratio in feedback loop

 $K_{\phi} = V_{DD}/2\pi$ $K_{VCO} = \frac{2\pi\Delta f_{VCO}}{2\pi}$

Δ٧٧CO

for a typical design $\omega_N \cong (2\pi/10)$ fr (at phase detector input)



PHASE LOCKED LOOP - LOW PASS FILTER DESIGN

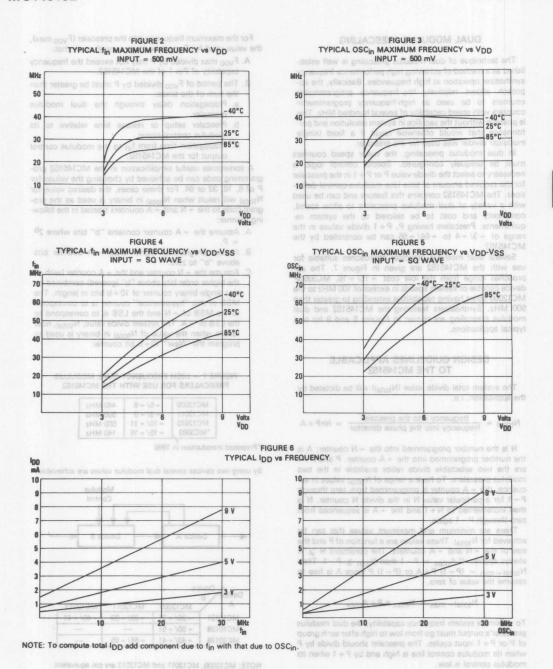
RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

Part Number	Format	Prescale	Phase Detector
MC145144	4-Bit Data	Single Modulus	3 State
MC145145	Bus Input	Single Modulus	3 State/2 Outpu
MC145146	Format	Dual Modulus	3 State/2 Outpu
MC145151	Parallel Input	Single Modulus	3 State/2 Output
MC145152	Format	Dual Modulus	2 Output
MC145155	Serial Input	Single Modulus	3 State/2 Outpu
MC145156	Format	Dual Modulus	3 State/2 Outpu
MC145157		Single Modulus	3 State/2 Output
MC145158		Dual Modulus	3 State/2 Output
MC145159		Dual Modulus	3 State/Analog

NOTE. Sometimes R1 is split into two sales registers each R1 + 2 A capacitor QC is then placed from the midpoint to ground to further filter by and BR. The value for CC should be such that the comet frequency of this network does not significantly affect cay.

OEFINITIONS: N = Total Division Ratio in feedback loop $K_{\beta} = V p p/2\pi$ Kyco. = $2\pi h t V CD$

or a typical design $\omega_{\rm N} \approx (2\pi/10) \, t_{\rm f}$ (at phase detector input)



DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145152 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of +3/+4 to +64/+65 can be controlled by the MC145152.

Several dual modulus prescaler approaches suitable for use with the MC145152 are given in Figure 7. The approaches range from the low cost +15/+16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145152 and dual modulus prescaling are shown in Figures 8 and 9 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145152

The system total divide value ($N_{\mbox{total}}$) will be dictated by the application. i.e.

$$N_{total} = \frac{frequency into the prescaler}{frequency into the phase detector} = N \cdot P + A$$

N is the number programmed into the +N counter; A is the number programmed into the +A counter. P and P+1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the +A counter is programmed from zero through P-1 for a particular value N in the divide N counter. N is then incremented to N+1 and the +A is sequenced from zero through P-1 again.

There are minimum and maximum values that can be achieved for N_{total}. These values are a function of P and the size of the +N and +A counters. The constraint N \geqslant A always applies. If A_{max} = P-1 then N_{min} \geqslant P-1. Then N_{total-min} = (P-1) P+A or (P-1) P since A is free to assume the value of zero.

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler (F_{VCO} max), the value used for P must be large enough such that:

- A. F_{VCO} max divided by P may not exceed the frequency capability of Pin 1 of the MC145152.
- B. The period of F_{VCO} divided by P must be greater than the sum of the times:
 - a. Propagation delay through the dual modulus prescaler.
 - b. Prescaler setup or release time relative to its modulus control signal.
 - Propagation time from f_{in} to the modulus control output for the MC145152.

A sometimes useful simplification in the MC145152 programming code can be achieved by choosing the values for P of 8, 16, 32 or 64. For these cases, the desired value for N_{total} will result when N_{total} in binary is used as the program code to the \pm N and \pm A counters treated in the following manner:

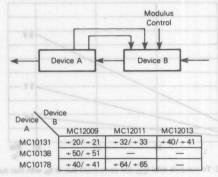
- A. Assume the + A counter contains "b" bits where 2^b = P.
- B. Always program all higher order + A counter bits above "b" to zero.
- C. Assume the + N counter and the + A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of + N and the LSB is to correspond to the LSB of + A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10+b bit counter.

FIGURE 7 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145152

MC12009	+5/+6	440 MHz
MC12011	+8/+9	500 MHz
MC12013	+10/+11	500 MHz
°MC3393	+ 15/ + 16	140 MHz

*Proposed introduction in 1980

By using two devices several dual modulus values are achievable:



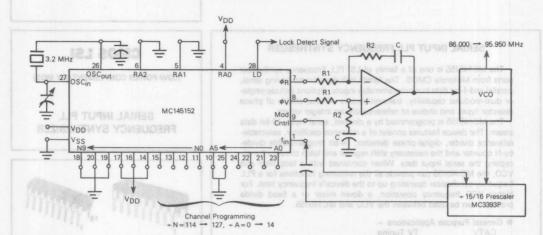
NOTE: MC12009, MC12011 and MC12013 are pin equivalent



8 Usar Selectable Reference Divider Values — 16, 512, 1024, 2049.

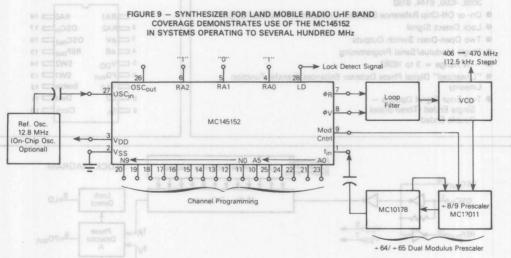


FIGURE 8 — AIRCRAFT NAV RECEIVER SYNTHESIZER DEMONSTRATES A LOW COST DUAL MODULUS SYSTEM EMPLOYING THE MC145152



NOTES:

- 1. f_R = 50 kHz, + R = 64; 22.0 MHz low side injection; N_{TOTAL} = 1720 → 1919.
 - 2. Using 22.0 MHz for the receiver I.F. demonstrates how the choice of I.F. value can sometimes reduce the number of + N bits that must be programmed. Using the more common 21.4 MHz I.F. would require six rather than four + N programming inputs.



NOTES:

- 1. NTOTAL = No64 + A = 32480 to 37600; N = 507 to 587; A = 0 to 63.
- 2. fR = 12.5 kHz, +R = 1024 (code 101).
- The prescaling approach can be chosen for the application to enhance economy e.g., single chip MC3393P to approximately 100 MHz. MC12011 or MC12013 with dual flip flop to approximately 250 MHz. MC12011 or MC12013 with MC10178 to over 500 MHz.

MC145155

2

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

A LOW COST DUAL MODULUS SYSTEM EMPLOYING THE MC145152

The MC145155 is one of a family of LSI PLL Frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

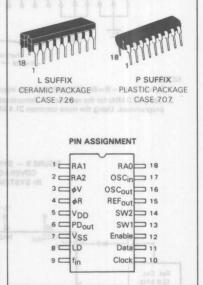
The MC145155 is programmed by a clocked, serial input, 16-bit data steam. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145155 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145155.

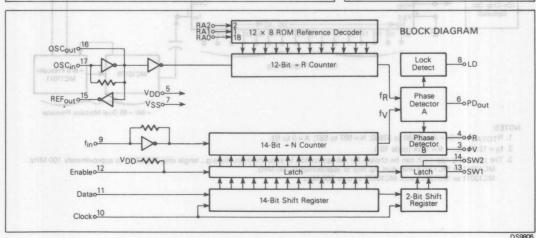
- General Purpose Applications —
 CATV TV Tuning
 AM/FM Radios Scanning Receivers
 Two-Way Radios Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Single Modulus/Serial Programming
- + N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options Single Ended (Three-State) Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL
FREQUENCY SYNTHESIZER





MAXIMUM RATINGS (Voltages Referenced to VSS)

atinU se Rating gyT nit/	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to +10	Vdc
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc
DC Current Drain Per Pin	1 8	10	mA
DC Current Drain VDD or VSS Pins	115	30	mA
Operating Temperature Range	TA	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

80 001 Ch	aracte	rietio			Symbol	VDD	TLO	w		25°C		TH	igh	Units
08	aracter	IBUC			Зуппооп	⋄ DD	Min	Max	Min	Тур	Max	Min	Max	Office
Power Supply Voltage	ge Ran	ge	-	3	VDD	-	3	9	3	-	9	3	9	Vdc
35 (15	+		100	0	UST	3	_	0.05	-	0	0.05	- 75	0.05	100
Output Voltage			- () Level	VOL	- 5		0.05	-	0	0.05	-	0.05	
$V_{in} = V_{DD}$ or 0					0.	9	-	0.05	-	0	0.05	-	0.05	Vdc
40 04				0	UST I	3	2.95	_	2.95	3	-	2.95	-	.vac
Vin = 0 or VDD		-		1 Level	VOH	5	4.95	_	4.95	5	_	4.95	-	1
					011	9	8.95	-	8.95	9		8.95	emi	Hold
Input Voltage	ő		() Level	117									
$V_0 = 2.5 \text{ or } 0.5$					N.	3	-	0.9	-	1.35	0.9	Ribiv	0.9	untu0
$V_0 = 4.5 \text{ or } 0.5$					VIL	5	-	1.5	-	2.25	1.5	n al	1.5	l mh
$V_0 = 8.5 \text{ or } 1.5$			30		- (φ)HW	9	-	2.7	-	4.05	2.7	- 1	2.7	Vdc
$V_0 = 0.5 \text{ or } 2.5$			_	1 Level		3	2.10	-	2.10	1.65	-	2.10	-	
$V_0 = 0.5 \text{ or } 4.5$				8	VIH.	5	3.5	-	3.5	2.75	_ 80	3.5	mA_esil	hoger.
$V_0 = 1.5 \text{ or } 8.5$					JHTI	9	6.3	-	6.3	4.95	-	6.3	nd mi	080
Reverse Breakdown	Voltag	е	SW1,	SW2	V _{BDSO}	3-9	15	-	15	24	-	15		٧
Output Current	20			Source	(9)1							Manif	nd m	086
VOH = 2.7					10Н	3	-0.44	-	-0.35		-	-0.22	100 -100	
$V_{OH} = 4.6$					10H	5	-0.64	-	-0.51	-0.88	RETTO/	-0.36	Y SWE	UD3FI
$V_{OH} = 8.5$						9	-1.3	-	-1.0	-1.3	-	-0.7	-	mAdo
$V_{OL} = 0.3$				Sink	M GG	3	0.44	-	0.35	0.66	nnd)	0.22	-	
$V_{OL} = 0.4$					IOL	5	0.64	-	0.51	0.88	-	0.36		Орега
$V_{OL} = 0.5$	14				- 0	9	1.3	-	1.0	1.3	-	0.7	per <u>il</u> pr	2000
Output Current	SI	N1, SV	V2	Sink	0	2000		iv - da	THEORY	Je - Judin				Alle see
$V_{OL} = 0.3$					1	3	0.48	-10-000	0.8	1.6	-	0.24	-	mA
$V_{OL} = 0.4$					IOL	5 .	0.90	SALF COS	1.5	15 = 3ndu	-	0.45	-	11111
V _{OL} = 0.5	N	.34	-		- 9	9	2.1	-	3.5	7	-	1.1	-	
Input Current	77		Other	r Inputs	- 6	9	-	±0.3	-	±0.00001	±0.1	-	±1.0	
			-	Enable	IL	9		-110	-	-50	-100	12081	-40	Umego
		30		oscin	- 0	9	1 - 38	±15	SHEW	± 5	±10	-	±8	μAdo
- 22				OSCin	11н	9	-	± 15	-	±5	±10	-	±8	
0 -	7	15	Other	Inputs	- IH E	9	- 0	±0.3	DVEVV	±0.00001	±0.1	-	±1.0	
Input Capacitance	15	16		81	Cin	3-9	-	10	-	6	10	-	10	pF
Output Capacitance	01	16		17	Cout	3-9		10	-	6	10	-	10	pF
						3	-	800	-	200	800	-	1600	= 400
Quiescent Current					IDD	5	_	1200	-	300	1200	-	2400	
			Alexander of the last			9	-	1600	-	400	1600	-	3200	μAdc
	rent	- Charles	Carl Constitution of	PDout	11	9		±0.1		+0.0001	±0.1		±3.0	"Adc

NOTE: $T_{low} = -40$ °C $T_{high} = 85$ °C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

		Characteris	tic				Symbol	VDD	Min	Тур	Max	Units
					Vác	07 4	-0.6 to	3	-	100	200	das 1
Output Rise Time							V TLH	5 V	-	50	100	ns
				-			07	9	-	40	80	nu3?
							30	3	Zn/9 :	100	200	muð l
Output Fall Time							THL	5	-	50	100	ns
					-		V/ Y	9	-	40	80	
						U01 4	01 00	3		70	140	-6
D D.I. T.							tPLH	5	-	50	100	ns
Propagation Delay Tim								9	eoire	40	80	RTO
Enable to SW1, SW	2						1.	3		70	140	
							tPHL	5 9	_ = =	50	100	ns
Min Max	Max	- CVT	Min	xald	000	-		-				-
Setup Times Data To Clock							ggV	3 5	-	10	40 35	191/4
Data To Clock							t _{su}	9		0	30	ns
							- 40K	3	_	30	50	F OV
Enable To Clock								5	_	20	40	ns
Lilable 10 Clock							tsu	9		20	40	113
Hold Time	100	- 0	26.9		00.4	- 9	1907	3	_	10	40	10
Data To Clock							th	5	_	4	35	ns
							111	9	_	0	30	by huc
Output Pulse Width	B.0.	d£,1	1 -1	6'0		1 8	иV	3	70	120	170	- 04
φR, φV with fR in						8	tWH(ø)	5	50	100	150	ns
Phase With fy							VVIII.	9	30	80	130	- QV
Innut Disa And Fall Tie		00.4	2.19		01.5			3	-	-	5	- 01
Input Rise And Fall Tin							tTLH	5	-	-	8.4 40 8.0	μS
OSC _{in} , fin	-	4.95	8.8		6.3		tTHL	9	_	_	8.8 20 6.1	- QV
Input Pulse Width							Vapso	3	40	30	dreak_down	0.0389
OSCin, fin, Clock							tw	5	35	20	#1911U	ns
COOIN, IIN , CIOCK		88.0-	38.0-		55.0-			9	25	15	2.7-	1403

			Ch	E.I -		Symbol	V _{DD}	Tlow		25°C			Thigh		U.V.
		0.22	Char	acteristic	44 - 0.35			Min	Max	Min	Тур	Max	Min	Max	Units
Operati	ing Freq	uency			10.0	1 6	3	-	17	-	27	14	-	12	24
OSCin				Input = S	SQ Wave VDD - VSS	fmax	5	-	33	-00	55	27	70	21	MHz
					00 - 00	0 0	. 9	-	35	-	65	35	-	33	de
				Input = 3	Sin Wave 500 mVp-p	5 0	3	-	11	-	21	10	-	9	dV
						fmax	5	-	20	-	34	17	-	.015	MHz
	0.00		100	toppop a		R	9	-	17	ust)	34	17	-	15	hion
Operati	ing Freq	uency				8	3	-	9	-	15	8	-	7	
fina				Input = S	Q Wave VDD - VSS	fmax	5	-	19	ni-	30	15	-	15	MHz
						0	9	-	31	nit-	52	26	-	22	
				Input = 3	Sin Wave 500 mV p-p	9	3	-	10	Othe	15	7	-	6	
						fmax	5	-	18	-	31	15	ettins	15	MHz
						1 00	9	-	21	-	31	15	- Total	15	June 1

T_{low} = -40°C
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23-State Lesicage Current

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MOTE $T_{low} = -40^{\circ}C$ $T_{high} = 85^{\circ}C$

PIN DESCRIPTIONS

RAO, RA1, RA2 (Pins 18, 1, and 2) — These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Refe	Reference Address Code								
RA2	RA1	RA0	Value 16						
0	0	0							
0	0	1 1 -	512						
0	111	500	1024						
0	1	1	2048						
1	0	0	3668						
1	0	1	4096						
1	1	0	6144						
1	1	1	8192						

 $\phi_{V},\,\phi_{R}$ (Pins 3 and 4) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PDout).

If frequency fy is greater than fp or if the phase of fy is leading, then error information is provided by ϕ_V pulsing low. ϕ_P remains essentially high.

If the frequency fy is less than f_R or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

VDD (Pin 5) - Positive power supply.

PD_{out} (Pin 6) — Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

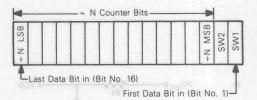
Frequency fy > fR or fy Leading: Negative Pulses. Frequency fy < fR or fy Lagging: Positive Pulses. Frequency fy = fR and Phase Coincidence: High-Impedance State.

Vss (Pin 7) - Circuit Ground.

LD (Pin 8) — Lock detector signal. High level when loop is locked (f $_{\rm R}$, f $_{\rm V}$ of same phase and frequency). Pulses low when loop is out of lock.

fin (Pin 9) — Input to + N portion of synthesizer. fin is typically derived from loop VCO and is AC coupled into Pin 9. For larger amplitude signals (standard CMOS Logic levels) DC coupling may be used.

CLOCK, DATA (Pins 10 and 11) — Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 16-bit shift register. The data is presented on the DATA input at the time of the positive clock transition. The DATA input provides programming information for the 14-bit + N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE (Pin 12) — When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pull-up establishes a continuously high level for ENABLE when no external signal is applied to Pin 12.

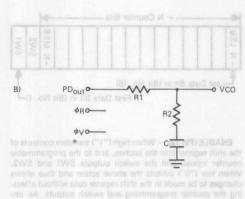
SW1, SW2 (Pins 13 and 14) — SW1 and SW2 provide latched open drain outputs corresponding to data bits numbers one and two. These will typically be used for band switch functions. A logic one will cause the output to assume a high-impedance state, while a logic zero will cause an output logic zero.

REF_{out} (Pin 15) — Buffered output of on-chip reference oscillator or externally provided reference-input signal.

OSC_{out}, OSC_{in} (Pins 16 and 17) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

101

 $K_{\phi} = V_{DD}/2\pi$ for ϕ_{V} and ϕ_{R}



epitorio QWZ bins TWZ — (&T bins &T emit) XWZ , TWZ stid stab of pribringermon studio misto nego bartorist con a contract of the stab of pribring and the stab of pribring

 $\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NRTC}}$ $f = 0.5 \omega_{N} (N/K_{\phi}K_{VCO})$ $F(s) = \frac{1}{R1CS + 1}$

RAO, RA1, RA2 (Pine 18, 1, and 2) - These three inputs

$$\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NC(R1 + R2)}}$$

at VI to search of $\zeta = 0.5 \omega_N (R2C + N/K_{\phi}K_{VCO})$

φy. φη (Pins 3 a

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

low. ϕ_V remains essentially high. If the frequency of $f_V=f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum.

$$\omega_{N} = \sqrt{\frac{\kappa_{\phi}\kappa_{VCO}}{\kappa_{CR1}}} = (6.49) \text{ ggV}$$
and the strength of th

and
$$y = \frac{\omega_N R2C}{2}$$
 of the state of elds level and $y = \frac{\omega_N R2C}{2}$ of the state of elds level.

Assuming gain A is very large, then:

$$F(s) = \frac{R2CS + 1}{R1CS} - (T mill) ggV$$

fin (Pin 8) - Input to + N portion of synthesizer, fin is

NOTE: Sometimes R1 is split into two series resistors each R1 + 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R . The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N .

DEFINITIONS: N = Total Division Ratio in feedback loop

 $K_{\phi} = V_{DD}/4\pi$ for PD_{out}

 $K_{\phi} = V_{DD}/2\pi$ for ϕ_V and ϕ_R

 $K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design $\omega_N \cong (2\pi/10)$ f_r (at phase detector input) $t \cong 1$

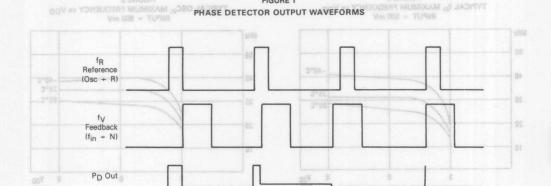


FIGURE 1

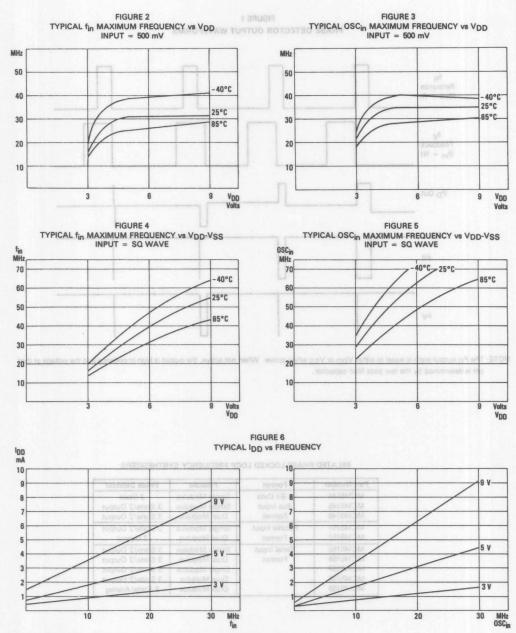


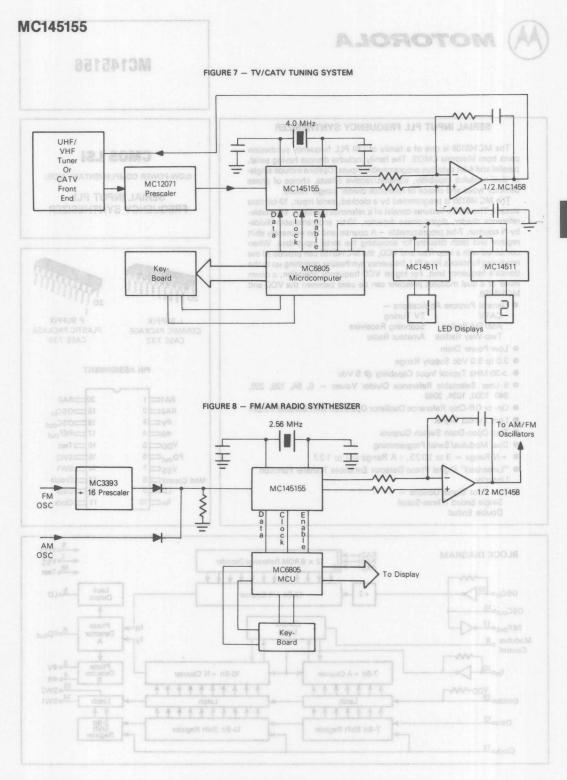
NOTE: The PD output state is equal to either VDD or VSS when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

NOTE: To compute total IDD add component due to fin with that due to OSCin

A 8	Part Number	Format	Prescale	Phase Detector		
	MC145144 MC145145 MC145146	4-Bit Data Bus Input Format	Single Modulus Single Modulus Dual Modulus	3 State 3 State/2 Output 3 State/2 Output		
	MC145151 MC145152	Parallel Input Format	Single Modulus Dual Modulus	3 State/2 Output 2 Output		
V 8	MC145155 MC145156 MC145157 MC145158 MC145159	Serial Input Format	Single Modulus Dual Modulus Single Modulus Dual Modulus Dual Modulus	3 State/2 Output 3 State/2 Output 3 State/2 Output 3 State/2 Output 3 State/Analog		





MC145156

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single-or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

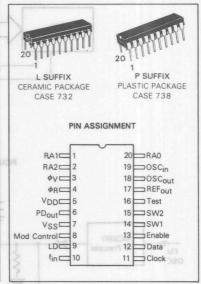
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable + A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156

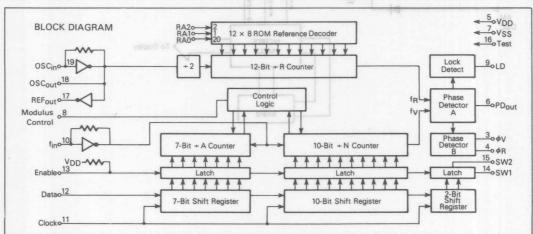
- General Purpose Applications —
 CATV TV Tuning
 AM/FM Radios Scanning Receivers
 Two-Way Radios Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values 8, 64, 128, 256, 640 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
 - Dual Modulus/Serial Programming
 - + N Range = 3 to 1023, + A Range = 0 to 127
 - "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
 - Two Error Signal Options Single Ended (Three-State)
 Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL
FREQUENCY SYNTHESIZER





 $T_{\rm low} \approx -40^{\circ} \rm C$ $T_{\rm high} = 55^{\circ} \rm C$

ssinU Rating qyT nill	Symbol	Value	Unit	
DC Supply Voltage	V _{DD} -0.5 to +10		Vdc	
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	Vdc	Output Rise Time
DC Current Drain Per Pin	- 1	10	mA	
DC Current Drain VDD or VSS Pins	1 %	30	mA	
Operating Temperature Range	TA	-40 to +85	°C	
Storage Temperature Range	T _{stq}	-65 to +150	°C	

ELECTRICAL CHARACTERISTICS

Characteristic					Symbol	V _{DD}	TLow		25°C			THigh		Units
an 001 1 00 - 0				Min Ma			Min	Тур	Max	Min	Max			
Power Supply Voltag	e Rang	je			VDD		3	9	3		9	3	9	Vdc
Vin = VDD or 0	80		-	0 Level	VOL	3 5 9	=	0.05 0.05 0.05	-	0 0 0	0.05 0.05 0.05	miTysis	0.05 0.05 0.05	Vdc
V _{in} = 0 or V _{DD}	50 30			1 Level	Voн	3 45 9	2.95 4.95 8.95		2.95 4.95 8.95	3 5 9	-	2.95 4.95 8.95	-	Vuc
Input Voltage V _O = 2.5 or 0.5 V _O = 4.5 or 0.5 V _O = 8.5 or 1.5	å 0 00		-	0 Level	VIL	3 5 9	=	0.9 1.5 2.7	=	1.35 2.75 4.05	0.9 1.5 2.7	- alo	0.9 1.5 2.7	Vdc
$V_O = 0.5 \text{ or } 2.5$ $V_O = 0.5 \text{ or } 4.5$ $V_O = 1.5 \text{ or } 8.5$				1 Level	VIH	3 5 9	2.10 3.5 6.3	-	2.10 3.5 6.3	1.65 2.75 4.95	=	2.10 3.5 6.3	emi	bloH
Reverse Breakdown	Voltage	9	SW1,	SW2	VBDSO	3-9	15	-	15	24	-	15	00 01	V
Output Current VOH = 2.7 VOH = 4.6 VOH = 8.5	120 100 80		70 60 30	Source	ЮНМ	3 5 9	-0.44 -0.64 -1.3	-	-0.35 -0.51 -1.0	-0.66 -0.88 -1.3	-	-0.22 -0.36 -0.7	Pulse V dvy with se With	mAd
V _{OL} = 0.3 V _{OL} = 0.4 V _{OL} = 0.5	1		-	Sink	IOLT	3 5 9	0.44 0.64 1.3	-	0.35 0.51 1.0	0.66 0.88 1.3	- 80 -	0.22 0.36 0.7	nit -ni	OS6
Output Current Mo VOH = 2.7 VOH = 4.6 VOH = 8.5	odulus	Contro	25	Source	ЮН	3 5 9	0.15 0.45 0.75	-	0.25 0.75 1.25	0.5 1.5 2.5	- 0.00	0.08 0.23 0.38	vilse VV	mAc
Output Current SV VOL = 0.3 VOL = 0.4 VOL = 0.5	W1, SW	/2, Mc	dulus (Control Sink	INOLO	3 5 9	0.48 0.90 2.10	-	0.8 1.5 3.5	1.6 3 7	Chara	0.24 0.45 1.05	- Ing frac	mA
Input Current	27 35 10	55 65 21	fin,	Inputs Enable OSCin	- IL 8	9 9	- a	±0.3 -110 ±15	V av e W 0 - LavaTM in	±0.00001 -50 ±5	±0.1 -100 ±10	-	±1.0 -40 ±8	р Ац
- 15 MHz		34		OSC _{in} Inputs	- IIH	9	p) [± 15 ± 0.3	_	±5 ±0.00001	±10 ±0.1	_	±8 ±1.0	
Input Capacitance	n i	at.		0	Cin	3-9	-	10	-	6	10	<u> </u>	10	pF
Output Capacitance	31	OS.		BI	Cout	3-9	a F 20	10	V etraVI	6	10		10	pF
Quiescent Current				91	lop	3 5 9		800 1200 1600	l evaW n	200 300 400	800 1200 1600	-	1600 2400 3200	μAd
3-State Leakage Curr	ent	31	-	PDout	- 11 8	9	-	±0.1	-	±0.0001	±0.1	-	±3.0	μAd

NOTE: $T_{low} = -40$ °C $T_{high} = 85$ °C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

SWITCHING CHARACTERISTICS (TA = 25°C, CL = 50 pF)

		Characteris	tic		Sint3		Symbol	VDD	Min	Тур	Max	Unit
	-				obV	00	-0.5 to -	3	-	100	200	ggu2
Output Rise Time						0+	TLH	5	-	50	100	ns
						3	751	9	-	40	80	San D
					TOTAL TOTAL		000	3	Eni9 g	100	200	
Output Fall Time						-	THL	5	E1817 8	50	100	ns
						CB.		9		40	80	2110019
					3"	Old I	+ 01 00 -	3	-	70	140	- Albair
							tPLH	5	-	50	100	ns
Propagation Delay Time								9	series	40	80	DIRTO
Enable to SW1, SW2								3	-	70	140	
						1 00	tPHL	5	_ 96	50	100	ns
	- 6		-		-		Transaction of the last of the	9		40	80	2
				70.0		1	Gió.	3	_	80	160	-
						1 3	tPLH	5) -	50	100	ns
Propagation Delay Time	CULU					1 3	30x	9	-	30	60	in mi
Clock to Modulus Co	ntrol					1-3		3	-	80	160	
						1 3	tPHL	5	-	50	100	ns
						1 3	A HON	9	-	30	60	A WILL
Setup Times				-	-			3	_	10	40	
Data To Clock							tsu	5	-	4	35	ns
						1 3	JIV.	9	-	0	30	1 0
						1 3		3	-	30	50	- 70
Enable To Clock						1	tsu	5	_	20	40	ns
						1.3		9	-	20	40	- 6
Hold Time		4.95	6.3	12	8.8		-	3	-	10	40	= 01
Data To Clock						1 1	th	5	SW1,	4	35	ns
- GI		*X			-	1	0508	9	11440	0	30	E COLUMN
Output Pulse Width		88.0-	-0.35		88.0-			3	70	120	170	0.100
φR, φV with tR in						1 3	tWH(6)	5	50	100	150	ns
Phase With fy								9	30	80	130	a La
Input Rise And Fall Tim	00	88.0	0.35		100		terre	3 5	-	-	5	- 1
	65		12.0			3	tTLH		-	-	4	μS
OSCin, fin		00.0	0.7		1 81	1	tTHL	9	-	-	2	-74
Input Pulse Width								3 5	40	30	M Trient	2 110
OSC _{in} , f _{in} , Clock						1	tw		35	20	-10	ns
Oodin, in , clock		4.	20.0		25.0		and the second	9	25	15	-	

FREQUENCY CHARACTERISTICS

			-	1.01 80 - 8	0 0 0		T	ow		25°C		Th	igh	vev
Am	-	0.45	Cha	racteristic	Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Unit
Operati	ng Frequ	uency	-	3.5 7	9 2 2 10	3	-	17	-	27	14	_	12	TOA
OSCin				Input = SQ Wave VDD - VSS	fmax	5	_	33	ne <u>dt</u> O	55	27	-	21	MHZ
				- 08- - 077-	6	9	-	35	-	65	35	-	33	
pAdc.				Input = Sin Wave 500 mVp-p		3		11	113	21	10	-	9	
				± 15 - ± 5	fmax	5	-	20	will.	34	17	-	15	MH
	0.13		1:02		-	9	_	17	isdi0	34	17	-	15	
Operati	ng Frequ	uency	OF.	0 - 01	8.6	3	2_	9	_	15	8	COUR	7	A STATE
fin				Input = SQ Wave VDD - VSS	fmax	5	2_	19	_	30	15	90 <u>0</u> 68	15	MH
				800 - 200	-	9	-	31	-	52	26	-	22	
				Input = Sin Wave 500 mVp-p	- 6	3	-	10	-	15	7	Trien	6	Desiru
				. 609 - 6091	fmax	5	_	18	_	31	15		15	MHz
					- 1100	9	-	21	-	31	15	ge <u>C</u> us	15	Statu

 $T_{low} = -40$ °C $T_{high} = 85$ °C

PIN DESCRIPTIONS

RAO, RA1, RA2 (Pins 20, 1, and 2) — These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Refe	rence Ad	Total Pivide Value	
RA2	RA2 RA1 RA0		Divide Value
0	0	0	Me 8 0 = 8
0	0	1	64
0	1	0	128
0	1	1 7	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	. 1	2048

 ϕ V, ϕ R (Pins 3 and 4) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{Out}).

If frequency fy is greater than f_R or if the phase of fy is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency fy is less than f_R or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V=f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

VDD (Pin 5) - Positive power supply.

 PD_{out} (Pin 6) — Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency fy > fR or fy Leading: Negative Pulses Frequency fy < fR or fy Lagging: Positive Pulses Frequency fy = fR and Phase Coincidence: High-Impedance State

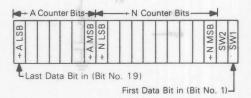
Vss (Pin 7) - Circuit Ground.

MODULUS CONTROL (Pin 8) - Signal generated by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the + A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the + N counter has counted the rest of the way down from its programmed value (N - A additional counts since both + N and + A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (NT) = N • P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the + N counter and A the number programmed into the + A counter.

LD (Pin 9) — Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

f_{in} (Pin 10) — Input to the positive edge triggers + N and + A counters. **f**_{in} is typically derived from a dual modulus prescaler and is AC coupled into Pin 10. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used

CLOCK, DATA (Pins 11 and 12) — Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 19-bit shift register. The data is presented on the DATA input at the time of the positive clock transition. The DATA input provides programming information for the 10-bit + N counter, the 7-bit +A counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE (Pin 13) — When high ("1") transfers contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low ("0") inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An onchip pull-up establishes a continuously high level for ENABLE when no external signal is applied to Pin 13.

SW1, SW2 (Pins 14 and 15) — SW1 and SW2 provide latched open drain outputs corresponding to data bits numbers one and two. These will typically be used for band switch functions. A logic one will cause the output to assume a high-impedance state, while a logic zero will cause an output logic zero.

TEST (Pin 16) — Used in manufacturing. Must be left open or tied to V_{SS} .

REFout (Pin 17) — Buffered output of on-chip reference oscillator, or externally provided reference-input signal.

OSC_{out}, OSC_{in} (Pins 18 and 19) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

si gool nertwievel rigiH, langis porosis. PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

 $\omega_{N} = \sqrt{\frac{K_{\phi}K_{VCO}}{NR1C}}$ $\xi = 0.5 \omega_{N} (N/K_{\phi}K_{VCO})$ $F(s) = \frac{1}{R1CS + 1}$

RAO RA1, RA2 (Pins 20, 1, and 2) - These times inputs

PD_{out} VCO

 $\omega_{N} = \sqrt{\frac{\kappa_{\phi} \kappa_{VCO}}{\kappa_{C(R1 + R2)}}}$

 $\zeta = 0.5 \omega_N (R2C + N/K_\phi K_{VCO})$

 $F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$

PD_{out} O R1

PR O R1

PR O VCO

 $\omega_{N} = \sqrt{\frac{K_{\phi}KVCO}{NCR1}}$ $\xi = \frac{\omega_{N}R2C}{2}$

Assuming gain A is very large, then:

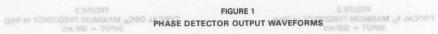
 $F(s) = \frac{R2CS + 1}{R1CS}$

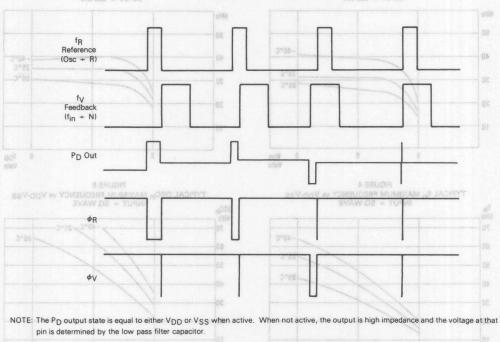
NOTE: Sometimes R1 is split into two series resistors each R1 + 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R . The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N .

mort betoennoo ed teum e DEFINITIONS: N = Total Division Ratio in feedback loop ammapong syllose

calls very microscopic to $K_{\phi} = V_{DD}/4\pi$ for PD_{out} and set of se

 $K_{\phi} = V_{DD}/2\pi$ for ϕ_V and $\phi_{DD}/2\pi$ for ϕ_V and ϕ_V

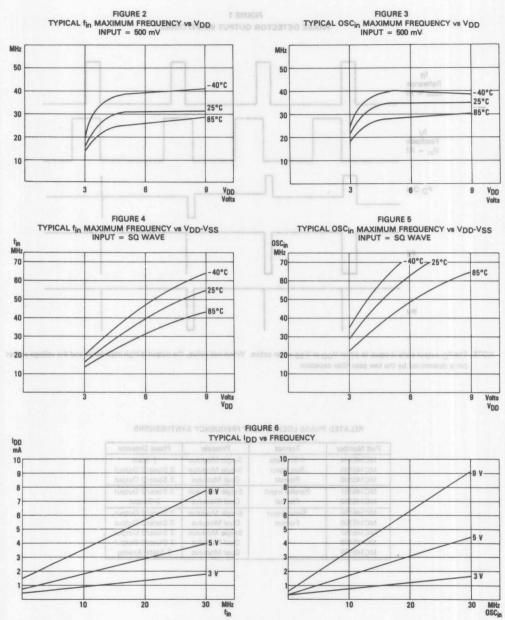
but something the set of the set of for a typical design $\omega_N \cong (2\pi/10)$ for the set of




NOTE: To compute total IDD add component due to Im with that due to OSCin.

RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

Part Number	Format	Prescale	Phase Detector	
MC145144	4-Bit Data	Single Modulus	3 State	
MC145145	Bus Input	Single Modulus	3 State/2 Output	
MC145146	Format	Dual Modulus	3 State/2 Output	
MC145151	Parallel Input	Single Modulus	'3 State/2 Output	
MC145152	Format	Dual Modulus	2 Output	
MC145155	Serial Input	Single Modulus	3 State/2 Output	
MC145156	Format	Dual Modulus	3 State/2 Output	
MC145157		Single Modulus	3 State/2 Output	
MC145158		Dual Modulus	3 State/2 Output	
MC145159		Dual Modulus	3 State/Analog	
		V 6		
	-			



NOTE: To compute total IDD add component due to fin with that due to OSCin.

2

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). The MC145156 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of +3/+4 to +128/+129 can be controlled by the MC145156

Several dual modulus prescaler approaches suitable for use with the MC145156 are given in Figure 7. The approaches range from the low cost +15/+16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz. Synthesizers featuring the MC145156 and dual modulus prescaling are shown in Figures 8 and 9 for two typical applications.

DESIGN GUIDELINES APPLICABLE TO THE MC145156

The system total divide value (N_{total}) will be dictated by the application, i.e.

N_{total} =
$$\frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

N is the number programmed into the + N counter; A is the number programmed into the + A counter. P and P+1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of Ntotal values in sequence, the + A counter is programmed from zero through P-1 for a particular value N in the divide N counter. N is then incremented to N+1 and the + A is sequenced from zero through P-1 again.

There are minimum and maximum values that can be achieved for $N_{total}.$ These values are a function of P and the size of the +N and +A counters. The constraint N>A always applies. If $A_{max}=P-1$ then $N_{min}>P-1.$ Then $N_{total-min}=(P-1)$ P+A or (P-1) P since A is free to assume the value of zero.

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler (F_{VCO} max), the value used for P must be large enough such that:

- A. F_{VCO} max divided by P may not exceed the frequency capability of Pin 10 of the MC145156.
- B. The period of F_{VCO}, divided by P, must be greater than the sum of the times:
 - a. Propagation delay through the dual modulus prescaler.
 - Prescaler setup or release time relative to its modulus control signal.
 - Propagation time from f_{in} to the modulus control output for the MC145156.

A sometimes useful simplification in the MC145156 programming code can be achieved by choosing the values for P of 8, 16, 32, 64 or 128. For these cases, the desired value for Ntotal will result when Ntotal in binary is used as the program code to the +N and +A counters treated in the following manner:

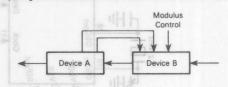
- A. Assume the + A counter contains "b" bits where 2^b = P
- B. Always program all higher order + A counter bits above "b" to zero.
- C. Assume the + N counter and the + A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+ b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of + N and the LSB is to correspond to the LSB of + A. The system divide value, N_{10tal}, now results when the value of N_{10tal} in binary is used to program the "New" 10+ b bit counter.

FIGURE 7 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145156

MC12009	+5/+6	440 MHz
MC12011	+8/+9	500 MHz
MC12013	+ 10/+11	500 MHz
*MC3393	+ 15/ + 16	140 MHz

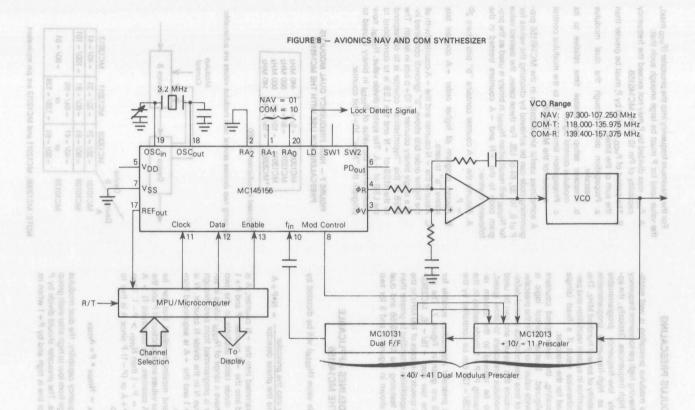
*Proposed introduction in 1980

By using two devices several dual modulus values are achievable:



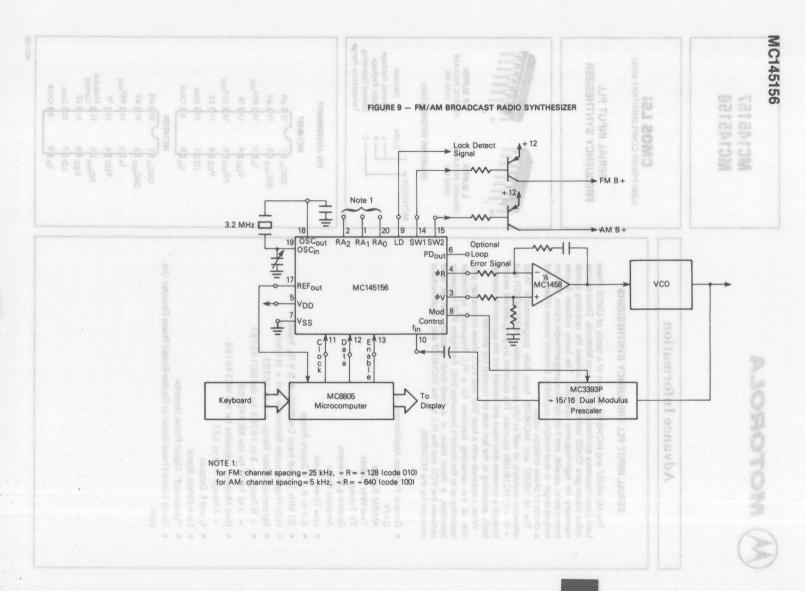
Device B	MC12009	MC12011	MC12013
MC10131	+20/+21	+32/+33	+40/+41
MC10138	+50/+51	+80/+81	+ 100/ + 101
MC10178	+40/+41 or +80/+81	+64/+65 or +128/+129	+80/+81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent



NOTES:

- 1) for NAV: F_R = 50 kHz, + R = 64 using 10.7 MHz lowside injection, N_{total} = 1946-2145 for COM-T F_R = 25 kHz, + R = 128 using 21.4 MHz highside injection, N_{total} = 4720-5439 for COM-R F_R = 25 kHz, + R = 128 using 21.4 MHz highside injection, N_{total} = 5576-6295
 2) A + 32/ + 33 dual modulus approach is provided by substituting an MC12011 (+8/+9) for the MC12013. The devices are pin equivalent.
 3) A 6.4 MHz oscillator crystal can be used by selecting + R = 128 (code 010) for NAV and + R = 256 (code 011) for COM



MC145157 MC145158

acter ton

Advance Information

SERIAL INPUT PLL FREQUENCY SYNTHESIZERS

The MC145157 and MC145158 are part of a family of CMOS Phase Lock Loop frequency synthesizer devices from Motorola. These devices utilize silicon-gate CMOS technology to achieve the operating speeds necessary for high-frequency operation. The family includes devices having serial, parallel, and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, and a choice of phase detector types.

The MC145157 and MC145158 have fully programmable 14-bit reference counters, as well as fully programmable + N (MC145157) and ÷ N/ ÷ A (MC145158) counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed-divide prescaler can be used between the VCO and the PLL for the MC145157 and a dual-modulus prescaler for the MC145158.

· General Purpose Applications -CATV

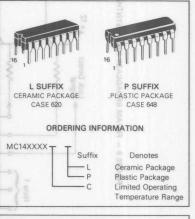
AM/FM Radios Two-Way Radios TV Tuning Scanning Receivers Amateur Radio

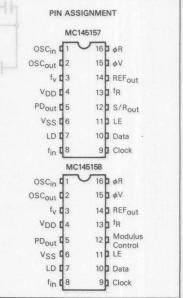
- Low Power Drain
- 3.0 to 9.0 V Supply Range
- 30 MHz Typical Input Capability @ 5 V (fin Input)
- Fully Programmable Reference and ÷ N Counters
- Reference Divider Range = 3 to 16383
- + N Range = 3 to 16383 for the MC145157
 - = 3 to 1023 for the MC145158
- Dual Modulus Capability for the MC145158
 - + A Range = 0 to 127
- f_v and f_r Outputs
- Lock Detect Signal
- · "Linearized" Digital Phase Detector
- Single Ended (Three-State) or Double-Ended Phase Detector Out-

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER





ADI-900

MAXIMUM RATINGS (Voltages Referenced to VSS)

Rating	Symbol	Value	Unit
DC Supply Voltage	VDD	-0.5 to $+10$	V
Input Voltage, All Inputs	Vin	-0.5 to V _{DD} +0.5	V
DC Current Drain Per Pin	1	10	mA
DC Current Drain VDD or VSS Pins	F	30	mA
Operating Temperature Range	TA	- 40 to +85	°C
Storage Temperature Range	T _{stq}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Vout\SVCC.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC).

ELECTRICAL CHARACTERISTICS

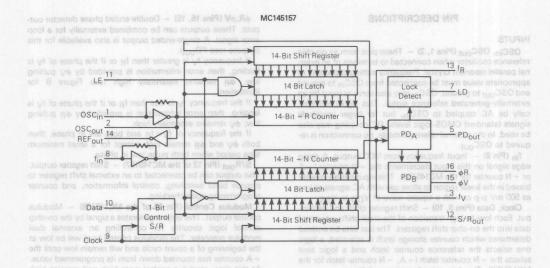
Character	detic	Symbol	V	TL	.ow		25°C		TH	ligh	
Character	ristic	Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Volta	ge Range	VDD		- 3	9	3	-	9	3	9	V
Output Voltage	0 Level		3	-	0.05	-	0	0.05	PET TE TOWN	0.05	10.101 (1)
$V_{in} = V_{DD}$ or 0	OE O LEVEL	VOL	5		0.05	-	0	0.05	-	0.05	
- U6		100	9	-	0.05		0	0.05		0.05	V
	US		3	2.95	_	2.95	3	_	2.95	(DetD)	all on
Vin=0 or VDD	1 Level	Voн	5	4.95	-	4.95	5	-	4.95	NODED :	T stal
		01.6	9	8.95	-	8.95	9	-	8.95	-	
Input Voltage	0 Level							18.00	autha dave	Seat also	3 rinte
$V_0 = 2.5 \text{ or } 0.5$	8 O Level	1 3	3	-	0.9	-	1.35	0.9	mBias your	0.9	D ITLOR
$V_0 = 4.5 \text{ or } 0.5$		VIL	5		1.5		2.75	1.5	_	1.5	-
$V_0 = 8.5 \text{ or } 1.5$		8	9	-	2.7	-	4.05	2.7	-	2.7	V
$V_{O} = 0.5 \text{ or } 2.5$	1 Level		3	2.10	-	2.10	1.65	-	2.10	-	618
$V_0 = 0.5 \text{ or } 4.5$		VIH	5	3.5		3.5	2.75		3.5	-	-
$V_0 = 1.5 \text{ or } 8.5$		1 1 3	9	6.3	_	6.3	4.95	_	6.3	Midth!	out Pt
Output Current	Source		1071	P			10 511	Ken Aun	BAA OSDILLA	to the sures	100
V _{OH} =2.7			3	-0.44		-0.35	-0.66		-0.22	-	
V _{OH} = 4.6		ЮН	5	-0.64	-	-0.51	-0.88	-	-0.36	And Fall	sala tia
V _{OH} =8.5			9	-1.3	-	-1.0	-1.3	-	-0.7	A 502/	m
V _{OL} = 0.3	Sink		3	0.44		0.35	0.66		0.22	_	
V _{OL} = 0.4		IOL	5	0.64	_	0.51	0.88	-	0.36	_	
V _{OL} = 0.5		9	9	1.3	-	1.0	1.3	Clack (Fig	0.7	O IUDIVV a	elus h
Output Current Mc	dulus Control										
	Source										
$V_{OH} = 2.7$			3	-0.25	-	-0.15	-0.5	-	-0.08	-	
$V_{OH} = 4.6$		IOH	5	-0.75		-0.45	-1.5	HS FICS	-0.23	ICY-CHI	m/
V _{OH} =8.5			9	- 1.25	7	-0.75	-2.5	-	-0.38	-	
	Iodulus Control	T V		V loca				acteristic	Cha		
V _{OL} =0.3	XEM Sink	Max M	3	0.8	-	0.48	1.6	-	0.24	-	
$V_{OL} = 0.4$	9 01	OL	-5	1.5	-	0.90	3	-	0.45	Cuermen 4	m/
V _{OL} =0.5	20 10	18.	-9	3.5	Vss+ F	2.10	V6V/7.12 =	lugr d	1.05	-	nie
Input Current	Other Inputs	87	9	-	±0.3	-	± 0.00001	± 0.1	-	±1.0	
	Enable	III 3	9	-	- 60	m (0 93) by	- 25	-50	- "	- 35	
	fin, OSCin	8	9	- X88	± 15	-	±5	± 10	-	±8	μΑ
	fin, OSCin	IH.	9	-	± 15	-	±5	±10	-	±8	-
8 -	Other Inputs	14	9	-	±0.3	-	±0.00001	±0.1	_	±1.0	gridin
Input Capacitance	30 22	Cin	3-9	- x80	10	01 (55.5)	6	10	-	10	pF
Output Capacitance		Cout	3-9	-	10	-	6	10	-	10	pF
0 1 - 1	THE WORLD		3	-	800	un bout ex	200	800	-	1600	
Quiescent Current		IDD	5	_ 354	1200	-	300	1200	-	2400	μΑ
		37.7	9		1600		400	1600	-	3200	

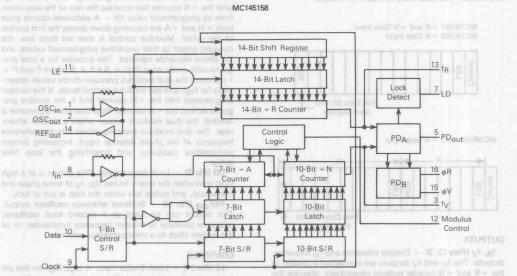
NOTE: T_{low}= -40°C T_{high}=85°C SWITCHING CHARACTERISTICS (TA = 25°C, CL = 50 pF)

contains accultry to protect the	Characte	ristic	mau		8018	Symbol	VDD	Min	Тур	Max	Units
st damage due to nigh stand	thisgis sin	odkar	- V	1 0	1 07	10-	3	-	100	200	ados a
Output Rise Time, Modulus Co	ntrol (Fig	ure 2)	V			TTLH	5	-	50	100	ns
				1			9	-	40	80	smuð D
nero serigal opinios ma to nea	exulta n	Pro .	Am	1	DE		3	5 Pie	50	100	error of
Output Fall Time, Modulus Cor	ntrol (Figu	ure 2)	30	+		tTHL	5	-	25	50	ns
ar it not proper operation to a	ONO BUTE					00	9	-	20	40	a mine di
the cape ONG-NA	of beni	61/2	Linne				3	-	140	280	76000
Output Rise Time, LD, fy, fR (Figure 2)					tTLH	5	-	90	180	ns
							9	-	80	160	
ogic voltage level laig., either							3	-	140	280	
Output Fall Time, LD, fy, fR (F	Figure 2)					tTHL	5	-	90	180	ns
							9	ISTICS	80	160	ECTRIC
4.07		25°C		901	T.		3	-	100	200	
						tPLH	5	18	50	80	ns
Propagation Delay Time							9		30	50	5 5 10
fin to Modulus Control (Figur						-	3		80	200	
90.0						tPHL	5	leve.	50	80	ns
						1 9	9		30	50	A HUIS
Setup Times				49.0			3	-	20	50	
Data To Clock						tsu	5	-	10	25	ns
Data To Clock							9	/ Iswau	8	20	a-ma
							3	Tove	25	60	
Latch Enable To Clock (Figur	re 4)					t _{su}	5	1040	8	15	ns
						1 0	9	-	5	10	2-04
Hold Time	2.7	4.05		2.7		0	3	- 3	50	80	a=nv
Data To Clock (Figure 4)						th	5	- Invest	30	50	ns
							9	leveu	10	25	a-av
Output Pulse Width		4.85	6.3		1 6	0	3	100	200	300	1 mov
φR, φV with fR in Phase Wit	h fy (Fig	ure 5)				tW(d)	5	50	100	150	ns
							9	40	70	100	t = sugar
36.0		88.G-	-0.51		1.64	- 2	3 5	-	-	5	-HOY
Input Rise And Fall Times						tTLH,		-	-	4	μS
Clock, OSCin, fin (Figure 6)						tTHL	9	1000	-	2	De HOV
90.0		89.0	18.0		1.85	0 2	3	40	30		0 = 10 V
Input Pulse Width OSCin, fin,	Clock (Fig	gure 7)				tw	5	35	20	- 8	ns
777							9	25	15		400

Characteristic						Symbol	Later V	T _{low} *		25°C			Thigh*		Units
		0.24	racteristic	8.1		Symbol	VDD	Min	Max	Min	Тур	Max	Min	Max	Unit
Operating	Frequency	0.46	-	3	08.0 -	1.5	3	č-	6	-	10	5	-	4	10V
OSCin			Input	= SQ Wave	e (VDD to VSS)	fmax	5	6-	13	-	20	10	-	8	MHz
							9	6-	18	- 8	32	16	-	13	Jugn
			□ □ Inpu	t = Sin Wa	ve (500 mVp-p)		3	8-	5	- 6	9	4	-	3	
						fmax	5	0-	8	40	13	6	-	5	MHz
	B±		01 +	da I	at		9	(-	9	7.0	14	7	-	6	
Operating	Frequency						3	6-	14	- 8	17	111	-	8	
in	10		Input	= SQ Wave	(VDD to VSS)	fmax	5	8.8	30	-	30	22	(mina	18	MHz
							9	0.5	30	-	49	41	a dieta	31	pond
			Inpu	t = Sin Wa	ve (500 mVp-p)		3	-	14	-	17	11	-	8	
					- 1000	fmax	5	-	29	-	30	22	17Terr	17	MHz
							9	-	37	-	40	30	-	24	

^{*}T_{low}= -40°C T_{high}=85°C





DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well estab-

PIN DESCRIPTIONS

INPUTS

OSC_{in}, OSC_{out} (Pins 1, 2) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

fin (Pin 8) — Input frequency from VCO output. A rising edge signal on this input decrements the +N counter (+A or +N counter for the MC145158). This input has an inverter biased in the linear region to allow use with AC signals as low as 500 mV p-p or with a square wave of Vpp to Vss.

Clock, Data (Pins 9, 10) — Shift register clock and data input. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the +N counter latch (+A, +N counter latch for the MC145158). The data entry format is as follows:

MC145157 + R and + N Data Input
MC145158 + R Data Input

Base Sylvariant Street
Shift Register

MC145158 + A, + N Data Input



OUTPUTS

 $f_{R},\,f_{V}$ (Pins 13, 3) — Divided reference and f_{1n} frequency outputs. The f_{R} and f_{V} outputs are connected internally to the + R and + N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

PD_{out} (Pin 5) — Single ended (three-state) phase detector output. This output produces a loop error signal that is used with a loop filter to control a VCO. This phase detector output is described below and illustrated in Figure 8.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance

ΦR,ΦV (Pins 16, 15) — Double-ended phase detector outputs. These outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{Out}).

If frequency fv is greater than f_R or if the phase of fv is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high (see Figure 8 for illustration).

If the frequency fy is less than f_R or if the phase of fy is lagging, then error information is provided by ϕ_R pulsing low; ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

S/R_{out} (Pin 12 of the MC145157) — Shift register output. This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

Modulus Control (Pin 12 of the MC145158) - Modulus control output. This output generates a signal by the on-chip control logic circuitry for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the + A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the + N counter has counted the rest of the way down from its programmed value (N - A additional counts since both + N and + A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (NT) = N • P + A where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the + N counter and A the number programmed into the + A counter. Note that when a prescaler is needed, the dual modulus version offers a distinct advantage. The dual modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter

LD (Pin 7) — Lock detect signal. This output is at a high logic level when the loop is locked (fR, fy of same phase and frequency), and pulses low when the loop is out of lock.

REFout (Pin 14) — Buffered reference oscillator output. This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

CONTROLS

LE (Pin 11) — Latch Enable Input. A logic high on this pin latches the data from the shift register into the reference divider or +N, +A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the +N, +A latches are activated if the control bit is at a logic low. A logic low on the LE pin allows the user to change the data in the shift registers without affecting the counters.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high performance frequency

2

synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). The MC145158 contains this feature and can be used with a variety of dual modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of $\pm 3/\pm 4$ to $\pm 128/\pm 129$ can be controlled by the MC145158.

Several dual modulus prescaler approaches suitable for use with the MC145158 are given in Figure 1. The approaches range from the low cost +15/+16, MC3393P device capable of system speeds in excess of 100 MHz to the MC12000 series having capabilities extending to greater than 500 MHz.

DESIGN GUIDELINES APPLICABLE TO THE MC145158

The system total divide value $(N_{\mbox{total}})$ will be dictated by the application, i.e.

$$N_{total} = \frac{frequency\ into\ the\ prescaler}{frequency\ into\ the\ phase\ detector} = N^{\bullet}P + A$$

N is the number programmed into the + N counter; A is the number programmed into the + A counter. P and P+1 are the two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the + A counter is programmed from zero through P-1 for a particular value N in the + N counter. N is then incremented to N+1 and the + A is sequenced from zero through P-1 again.

There are minimum and maximum values that can be achieved for N_{total} . These values are a function of P and the size of the + N and + A counters. the constraint N \geq A always applies. If $A_{max} = P-1$ the $N_{min} \geq P-1$. Then $N_{total-min} = (P-1)$ P + A or (P-1) P since A is free to assume the value of zero.

$$N(total - max) = N_{max} P + A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler (F_{VCO} max), the value used for P must be large enough such that:

- A. F_{VCO} max divided by P may not exceed the frequency capability of Pin 8 of the MC145158.
- The period of F_{vco(max)}, divided by P, must be greater than the sum of the times:
 - a. Propagation delay through the dual modulus prescaler.

- synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable modulus control signal.
 - c. Propagation time from f_{in} to the modulus control output for the MC145158.

A sometimes useful simplification in the MC145158 programming code can be achieved by choosing the values for P of 8, 16, 32, 64 or 128. For these cases, the desired value for Ntotal will result when Ntotal in binary is used as the program code to the +N and +A counters treated in the following manner:

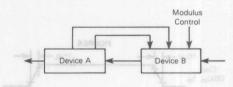
- A. Assume the \div A counter contains "b" bits where $2^b = P$
- B. Always program all higher order + A counter bits above "b" to zero.
- C. Assume the + N counter and the + A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+ b bits in length. The MSB of this "hypothetical" counter is to correspond to the MSB of + N and the LSB is to correspond to the LSB of + A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "New" 10+b bit counter.

FIGURE 1 — HIGH FREQUENCY DUAL MODULUS PRESCALERS FOR USE WITH THE MC145158

1	MC12009	+5/+6	440 MHz Min
	MC12011	+8/+9	500 MHz Min
	MC12013	+10/+11	500 MHz Min
	MC12015	+32/+33	225 MHz Min
	MC12016	+40/+41	225 MHz Min
	MC12017	+64/+65	225 MHz Min
	* MC12018	+ 128/ + 129	520 MHz Min
	MC3393	+ 15/ + 16	140 MHz Typ

^{*}Proposed Introduction 1983

By using two devices several dual modulus values are achievable:

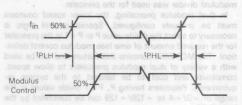


ice B	MC12009	MC12011	MC12013
MC10131	+20/+21	+ 32/ + 33	+40/+41
MC10138	+50/+51	+80/+81	+ 100/ + 101
MC10154	+ 40/ + 41 or + 80/ + 81	+ 64/ + 65 or + 128/ + 129	+80/+81

NOTE: MC12009, MC12011 and MC12013 are pin equivalent. MC12015, MC12016, and MC12017 are pin equivalent.

by the second at high frequencies, Best at New SWITCHING WAVEFORMS. Prescalar setup or release time relative in

signiel boxil a li sluser sell'FIGURE3 wow tent sonamot



MC12000 series havin ESPURIFICATION extending to greater than

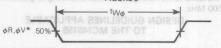
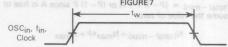
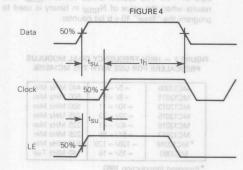


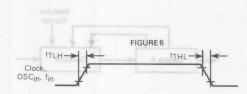
FIGURE 7



9 tot seulev arti prizodno vd baveFIGURE 2 so aboo onimmess THIT 128 For these CHITTER Value for Any Output

to the MSB of + N and the LSB is to correspond to the





*fr in phase	with f _V	Davice

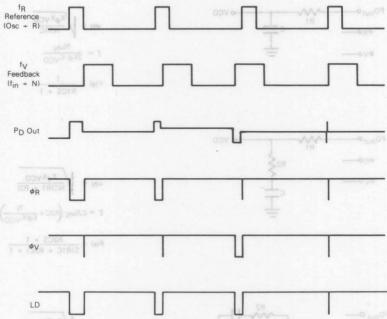


FIGURE 8
PHASE DETECTOR OUTPUT WAVEFORMS

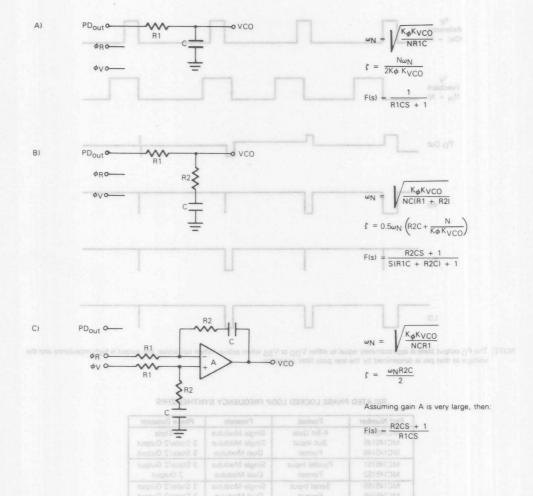
NOTE: The PD output state is approximately equal to either VDD or VSS when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

RELATED PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS

Part Number	Format	Prescale	Phase Detector	
MC145144	4-Bit Data	Single Modulus	3 State	1 0 3 45 0 M S
MC145145	Bus Input	Single Modulus	3 State/2 Output	
MC145146	Format	Dual Modulus	3 State/2 Output	
MC145151	Parallel Input	Single Modulus	3 State/2 Output	
MC145152	Format	Dual Modulus	2 Output	
MC145155	Serial Input	Single Modulus	3 State/2 Output	
MC145156	Format	Dual Modulus	3 State/2 Output	
MC145157		Single Modulus	3 State/2 Output	Sometimes R 1 is split into
MC145158		Dual Modulus	3 State/2 Output	eg. The value for Co she
MC145159		Dual Modulus	3 State/Analog	The same same same

 $K_{\Phi} = V_{DD}/4\kappa$ for PD_{Out} $K_{\Phi} = V_{DD}/2\kappa$ for ϕ_{V} and ϕ_{R} 2

PHASE LOCKED LOOP - LOW PASS FILTER DESIGN



NOTE: Sometimes R1 is split into two series resistors each R1 + 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R . The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N .

DEFINITIONS: N = Total Division Ratio in feedback loop
$$\begin{split} K_{\phi} &= V_{DD}/4\pi \text{ for PD}_{Out} \\ K_{\phi} &= V_{DD}/2\pi \text{ for } \phi_{V} \text{ and } \phi_{R} \\ K_{VCO} &= \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}} \\ \text{for a typical design } \omega_{N} & \equiv \frac{2\pi \text{ fr}}{10} \text{ (at phase detector input)} \\ \xi & \cong 1 \end{split}$$

MOTOROLA



Product Preview

SERIAL INPUT PLL FREQUENCY SYNTHESIZERS WITH ANALOG PHASE DETECTOR

The MC145159 is part of a family of CMOS Phase Lock Loop frequency synthesizer devices from Motorola. This device utilizes silicon-gate CMOS technology to achieve the operating speeds necessary for high-frequency operation. The family includes devices having serial, parallel, and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, and a choice of phase detector types.

The MC145159 has a fully programmable 14-bit reference counter, as well as fully programmable + N/+ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

When combined with a loop filter and VCO, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed-divide prescaler can be used between the VCO and the PLL.

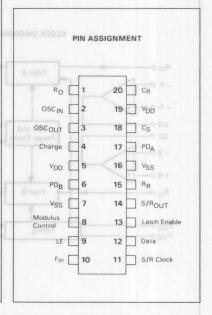
- General Purpose Applications CATV
 AM/FM Radios
 Two-Way Radios
 TV Tuning
 Scanning Receivers
 Amateur Radio
- Low Power Drain
- 3.0 to 9.0 V Supply Range
- > 30 MHz Typical Input Capability @ 5 V
- Fully Programmable Reference and ÷N/÷ A Counters
- Reference Divider Range = 3 to 16383
- ÷N Range = 3 to 1023
- Dual Modulus Capability
- ÷A range = 0 to 127
- Lock Detect Signal
- "Linearized" Digital Phase Detector
- Single Ended (Three-State) or Analog Phase Detector Outputs.

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

L SUFFIX
CERAMIC PACKAGE
CASE 732

P SUFFIX
PLASTIC PACKAGE
CASE 738





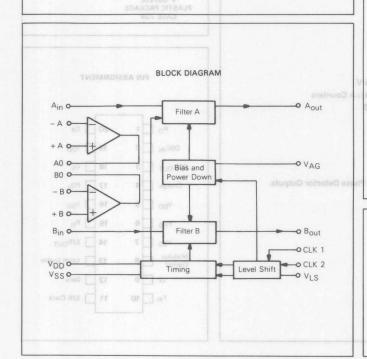
MC145414

MOTOROL

DUAL TUNEABLE LOW PASS SAMPLED DATA FILTERS

The MC145414 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two totally uncommitted op amps for use elsewhere in the system as I to V converters, gain adjust buffers, etc.

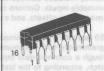
- Two General Purpose 5th Order Elliptic Low Pass Filters
- Low Operating Power Consumption 30 mW (Typical)
- Power Down Capability 1 mW (Maximum)
- ±5 to ±8 Volt Power Supply Ranges
- TTL or CMOS Compatible Inputs Using VLS Pin
- Two Operational Amplifiers Available to Reduce Component Count
 - Useful in LPC or CVSD Speech Applications
 - Passband Edges Tuneable With Clock Frequency From 1.25 kHz to 10 kHz



CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL TUNEABLE LOW PASS SAMPLED DATA FILTERS





L SUFFIX CERAMIC PACKAGE CASE 620 P SUFFIX PLASTIC PACKAGE CASE 648

PIN ASSIGNMENT

VAG	100	16	VDD
+ A [2 90/6	15	Ain
- A [3	14	Aout
A0	4 oil	13	Bin
B0 [5 minns	12	Bout
- B C	6	11	CLK 1
+ B [7	10	CLK 2
VSS	8	9	VLS

ORDERING INFORMATION

MC14XXXX

L Ceramic Package
P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{Out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either VSS or VDD).

DS-9557

25°C	Rating	Symbol	Value	Unit
DC Supply Voltage	(40)	V _{DD} -V _{SS}	-0.5 to 18	٧
Input Voltage, All Pins	A _{in} , B _{in}	V _{in}	-0.5 to V _{DD} +0.5	V
DC Current Drain per Pin (Excluding V	DD, VSS)	1	10 memu O	mA
Operating Temperature Range	A _{in} , e _{in} 2	TA	0 to 85	°C
Storage Temperature Range	A _{in} , B _{in} , +A, -A, +B, -B V	T _{stg}	- 65 to 150	°C
An - Of ± - GI	+ A te - A, + 8 to - B		Offset Current	tugn

vm u/ ± 0/ ± -	Parameter	Symbol	Min	Тур	Max	Unit
DC Supply Voltage	AU, BU, Agut, Bout	V _{DD} -V _{SS}	10	12	16	V
Clock 1, 2 Frequency	ROV	fCL	50	128	400	kHz

	0 1 1	VDD		25°C	bearing 1	Unit
Characteristic	Symbol	Vdc	Min	Тур	Max	Uni
Operating Current C = 2 OP OB OA DOS ON OR OF THE COLUMN A COLUM	IDD	12	-	2.0	4.0	mA
Power-Down Current (PDI=VSS) — 08.0A	IPD	12	-	10	40 60	μΑ
Input Capacitance	Cin	12	-	5.0	-	pF
MODE CONTROL LOGI	C LEVELS			DULGITADES	mann a	a moder o
VLS Power-Down Mode (g-g V \$,0m8bc + = siese	VIH	12 15	11.5 14.5	11 13	V 91=39V	V
VLS TTL Mode qvT niM	airain <u>o</u> raen	12 15	4.0 5.0		8 9	٧
VLS CMOS Mode	VIL	12 15	- (g)-i	 350 Hz≟ó 3000	0.8	٧
VAG Power-Down Mode	VIH	12 15	11.5 14.5	10.5 13.5	Bend Resi O Hz –	o iv
VAG Analog-Ground Mode	VIL	12 15	_		7.0 9.0	V
Combb N DN - 12008 of let CMOS LOGIC LEVELS (V _{LS} =V _{SS})			(=VAC)	AFeliol4.t	uquu
Input Current Clock 1, 2 "1" Level (Internal Pulldown Resistors) "0" Level	lin	12 12	_	50 - 0.00001	100 -0.3	μA
Input Voltage Clock 1, 2 "0" Level	VIL	12 15	-	5.25 6.75	3.0 3.5	V
"1" Level	VIH	12 15	9.0 11.5	6.75 8.25	13 2 <u>7</u> 00 kH	V
TTL LOGIC LEVELS (VLS =	V, VSS=	0 V)	treature Deep F			15000
Input Current Clock 1, 2 "1" Level (Internal Pulldown Resistor) "0" Level	lin	12 12	_	50 - 0.00001	100 -0.3	μ
Input Voltage Clock 1, 2 mgbs a sleep lint ombb 0 = 10" Level "1" Level	VIL	12	- V _{LS} + 2.0	PICATIONS	VLS+0.8	

Cheracteratio	niM		
lesponse 3400 Hz 3400 Hz 3 3000 Hz 4500 Hz 4600 Hz 4s kHz			
	79		
itferential Group Delay 1150 to 2300 KHz Delay 100 to 2500 KHz Delay 800 to 2700 KHz Delay			84

ANALOG ELECTRICAL CHARACTERISTICS (VDD = 12 V)

Value Unit		odmy8				0		25°C		11-14
-0.6 to 18 V			Characteris	tic		Symbol	Min	Тур	Max	Unit
Input Current	0-	niV			A _{in} , B _{in}	lin	-	±0.00001	±1.0	μΑ
Input Current		. 1			VAG	ddin	(E43)	±0.00001	±10	μА
AC Input Impedance (1 kHz)	AT			A _{in} , B _{in}	Zin	42 08	2	911	MΩ
Input Common Mode	Voltage	Range			$A_{in}, B_{in}, +A, -A, +B, -B$	VICR	2.0	parat u e ha	10.0	V
Input Offset Current					+ A to - A, + B to - B	IID	-	± 10	-	nA
Input Bias Current					+ A, - A, + B, - B	IB	STEELE	±0.10	± 1.0	nA
Input Offset Voltage	355 A	admir2	1		+ A to - A, + B to - B	VID	-	± 10	±70	mV
Output Voltage Range $(R_L = 20 \text{ k}\Omega \text{ to VAG})$ $(R_L = 600 \Omega \text{ to VAG})$ $(R_L = 900 \Omega \text{ to VAG})$	i, R _B = 0 i, R _B = 1	.6 $k\Omega$ to	00		A0, B0, A _{out} , B _{out}	VOR	1.5 3.0 2.5	y <u>on</u> oups —	10.5 8.3 9.0	8 00 V
Small Signal Output Ir	npedano	e (1 kHz)			A _{out} B _{out}	Zo	18 <u>A</u> H	50 50	TET.	Ω
Output Current (V _O = 10.5 V)	Typ	nili nili		Symbol	A _{out} , B _{out} , A0, B0	Іон	- 200	- 400	-	μА
$(V_0 = 1.5 V)$	2.0	1	181	_ggl_	A _{out} , B _{out} , A0, B0	IOL	5	7.5	D en	mA
Unity Gain Output No	ise	-	12	0.91	A0, B0	-	12¥=1	15	(New)	μVrms

FILTER A SPECIFICATIONS

(VDD - VEE = 12 V, f_{Cl. 1}, f_{Cl. 2} = 128 kHz, V_{in} = 0 dBm0, full scale = +3dBm0, 7 V p-p)

	0.8	OL.					25°C		Unit
		Ch	aracteristi			Min	Тур	Max	Unit
Gain (1020 Hz)	T	12				17.4	18	18.6	dB
Passband Ripple (50 Hz to 300	00 Hz)	15	Tia			-	0.24	1.0	dB
Out of Band Response 3400 Hz 4000 Hz-4600 Hz	11.5 14.6	12	HIV			_ - 10	- 0.8 - 15.5	10.00	dB
4600 Hz-64 kHz						- 25	- 33.0	DOMESTIC STATE	nA DAV
Output Noise (Ain = VAG)			lasV=a	CMOS LOGIC LEVELS IVI	ref to 900 Ω	-	10	17	dBrnc0
Dynamic Range	1	121	T	leve i "I"		76	83	D Then	dB
Differential Group Delay		1,2	THE PARTY	laveJ "0"	0	notaia	9-owo	allus In	(loten
1150 to 2300 kHz Delay						-	Jaco	O Figer	μS
1000 to 2500 kHz Delay						-	-	_	-
800 to 2700 kHz Delay						-	-	-	
Power Supply Rejection Ratio	(VDD = 12)	V + 0.1	VRMS @	1 kHz)		-	36	-	dB
Crosstalk (A _{in} = VAG, B _{in} = 0	dBm0 Outpi	ut at Ao	ut at 3 kH	z)		-	76		dB
2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1 31		1372.7		_	2 7 1 1 1 1 1 1	02.751211	201527 17 17

FILTER B SPECIFICATIONS (VDD - VEE = 12 V, f_{CL 1}, f_{CL 2} = 128 kHz, V_{in} = 0 dBm0, full scale = +3dBm0, 7 V p-p)

Characteristic		25°C		Unit
Characteristic	Min	Тур	Max	Unit
Gain (1020 Hz)	-0.7	±0.15	+0.7	dB
Passband Ripple (300 Hz to 3000 Hz)	-	0.22	1.0	dB
Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz	- - 10 - 28	-0.8 -15.5 -33.0	-	dB
Output Noise (300 Hz-3400 Hz)	-	8	14	dBrnc
Dynamic Range (7 V p-p Max)	79	87	-	dB
Differential Group Delay 1150 to 2300 kHz Delay 1000 to 2500 kHz Delay 800 to 2700 kHz Delay	-			μS
Crosstalk (Bin = VAG, Ain = 0dBm0 @ 3 kHz Output at LPO @ 3 kHz)	-	76	-	dB
Power Supply Rejection Ratio	-	36	-	dB

SWITCHING CHARACTERISTICS (VDD - VSS = 10 V, TA = 25°C)

AND 2 AT 128 KHZ	Characteristics	SHX PO TA	Combat	0	Units		
	Characteristics		Symbol	Min	Тур	Max	Units
Input Rise Time Input Fall Time	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Clock 1, 2	tTLH tTHL		-	4	μS
Pulse Width	0f - p	Clock 1, 2	tWH	200	-	-	ns
Clock Frequency	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Clock 1, 2	fCL	50	1+1	400	kHz
Clock 1, 2 Duty Cycle			H	40	-	60	%

FUNCTIONAL DESCRIPTION OF PINS

Pin 1 - VAG (Analog Ground)

This pin should be held at approximately (VDD-VEE)/2. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1.0 V of VDD, the chip will be powered down.

Pin 2 - + A

Non-inverting input of op-amp A.

Pin 3 - - A

Inverting input of op-amp A.

Pin 4 - A0

Output of uncommitted op-amp A.

Pin 5 - B0

Output of uncommitted op-amp B.

Pin 6 - - B

Inverting input of op-amp B.

Pin 7 - + B

Non-inverting input of op-amp B.

Pin 8 - Vss

This is the most negative supply pin and digital ground for the package.

Pin 9 - VLS (Logic Shift Voltage)

The voltage on this pin determines the logic compatibility

for the Clock 1, 2 inputs. If V_{LS} is within 0.8 V of VSS, the thresholds will be for CMOS operating between V_{DD} and VSS. If VLS is within 1.0 V of VDD, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at Clock 1, 2 will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 - Clock 1

Always tie clock 1 and clock 2 together.

Pin 11 - Clock 2

Always tie clock 1 and clock 2 together.

Pin 12 - Bout (Lowpass Filter B)

This is the output of B lowpass filter.

Pin 13 - Bin (Lowpass Filter B)

This is the input to filter B.

Pin 14 - Aout (Low pass Filter A)

This pin is the output to filter A.

Pin 15 - Ain (Lowpass Filter A)

This is the input to filter A.

Pin 16 - VDD

Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance inputs.

FILTER DESCRIPTION

FILTER A DESCRIPTION

Filter A of the MC145414 is a 5-pole elliptic tuneable lowpass filter operating at a sampling rate determined by clock 1 and clock 2. This filter provides band limiting that is a direct function of clock 1 and clock 2. With a 128 kHz clock, the band limiting frequency is 3.6 kHz. By dividing the clock in half to 64 kHz, the band limiting frequency is cut in half to 1.8 kHz (as illustrated in Figure 1). Likewise by doubling the clock, the cutoff point will double (as illustrated in Figures 3 and 4). The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 db. Because the MC145414 is a switch capacitance filter, the sampled output signal will have switching noise present near multiples of the switching frequency; a single-pole RC filter may be required to reduce this.

To provide 50/60 Hz and 15 Hz rejection, a 3-pole Chebychev highpass filter can be externally realized with the MC145414 by using the uncommitted op-amps as an active filter. This is shown in Figure 5 and 6.

FILTER B DESCRIPTION

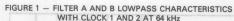
Filter B in the MC145414 consists of a 5-pole elliptic tuneable lowpass filter operating at a sampled rate determined by clock 1 and clock 2. Filter B is functionally similar to filter A, except filter B has unity gain.

Clock 1 and 2

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, VLS. Clock 1, 2 pins should be tied together.

Power Down

The MC145414 may be powered down by bringing VAG to within 1.7 V of VCC or by bringing VLS to within 1.7 V of VDD



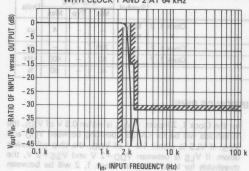
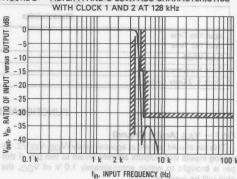


FIGURE 2 - FILTER A AND B LOWPASS CHARACTERISTICS



Pin 11 — Clock 2

Absence the glock 1 and clock 2 together.

TICS

Pin 10 - Clock |

FIGURE 4 — FILTER A AND B LOWPASS CHARACTERISTICS
WITH CLOCK 1 AND 2 AT 400 kHz

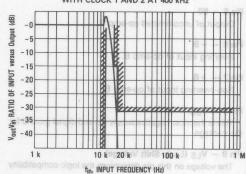
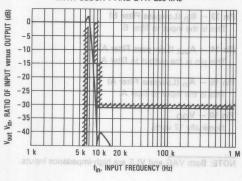


FIGURE 3 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 256 kHz



EUTER DESCRIPTION

FILTER & DESCRIPTION

Filter B in the MC146414 consists of a 5-pole elliptic tuneable lowpass filter operating at a sampled rate determined by clock 1 and clock 2. Filter B is functionally similar to filter A, except filter B has unity gain.

Clock 1 and 2

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, when the stied together.

Power Down

The MC145414 may be powered down by bringing VAG to within 1.7 V of VCC or by bringing VLS to within 1.7 V of

PLIER A DESCRIPTION

Filter A of the MC145414 is a 5-pole elliptic tuneable lowpass filter operating at a sampling rate determined by clock 1 and clock 2. This filter provides band limiting treat function of clock 1 and clock 2. With a 128 kHz clock, the band limiting frequency is 3.6 kHz. By dividing the clock in half to 1.8 kHz tas illustrated in Figure 1). Likewise by doubling the clock, the cutoff point will double is illustrated in Figures 3 and 4). The clock frequency can be varied from 65 kHz to 400 kHz. Filter A, unlike filter 8, has a gain of 18 campled output signal will have switching noise present near multiples of the switching frequency; a single-pole RC litter

To provide 50/80 Hz and 15 Hz rejection, a 3-pole Chebychev highpess filter can be externally realized with the MC145414 by using the uncommitted op-amps as an active filter. This is shown to figure 5 and 6.

FIGURE 5 - FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECT FILTER

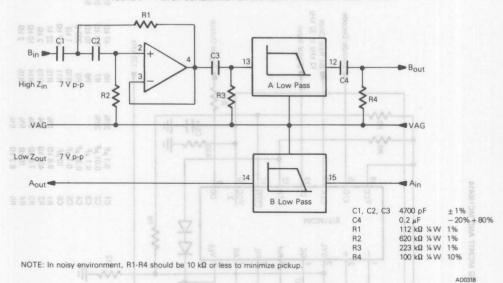
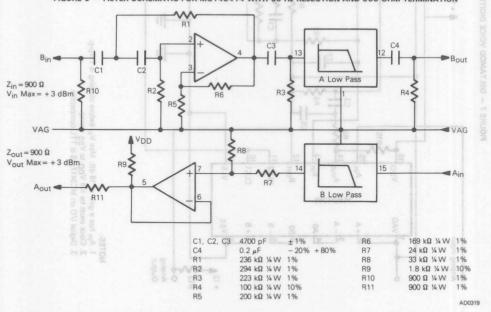
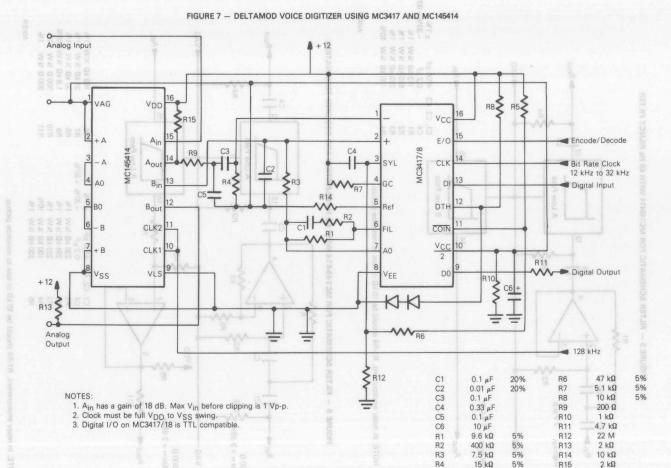


FIGURE 6 - FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECTION AND 900 OHM TERMINATION



NOTE: In noisy environment, R1-R4 should be 10 $k\Omega$ or less to minimize pickup.



R5

5%

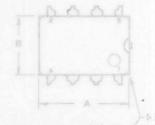
 $8.2~k\Omega$

Mechanical Data

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

S-PIN PACKAGE

P SUFFIX PLASTIC PACKAGE CASE 626





Mechanical Data



			A			
388		2.5				

NOTES

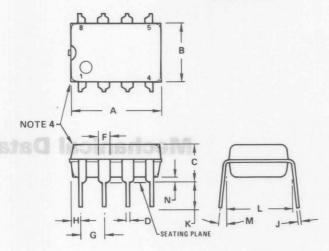
- 1. LEADS WITHIN 0.13 mm (6,005) RADIUS OF TRUE POSITION AT SEATING PLANE ANAXIMUM MATERIAL CONDITION LEADS WHEN FORMED PARALLEL.
- 3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

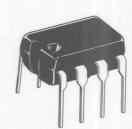
Mechanical Data

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

8-PIN PACKAGE

P SUFFIX PLASTIC PACKAGE CASE 626



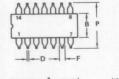


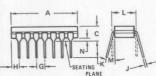
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.40	10.16	0.370	0.400
В	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
Н	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	_	100	-	10 ⁰
N	0.51	0.76	0.020	0.030

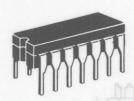
NOTES:

- LEADS WITHIN 0.13 mm
 (0.005) RADIUS OF TRUE
 POSITION AT SEATING
 PLANE AT MAXIMUM
 MATERIAL CONDITION.
- 2." DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

2







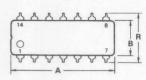
MILLIMETERS INCHES DIM MIN MAX MIN MAX A 19.05 19.94 0.750 0.785 В 6 10 7.49 0.240 0.295 0.200 C 5.08 _ D 0.58 0.015 0.023 0.38 F 1.77 0.055 0.070 1.40 2.54 BSC G 0.100 BSC 1.9 2.29 0.075 0.090 J 0.20 0.38 0.008 0.015 K 3.18 5.08 0.125 0.200 L 7.62 BSC 0.300 BSC M _ 15° _ 15° 1.02 0.020 0.040 N 0.51

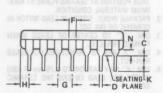
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAX-
- INUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

 2. DIMENSION "L" TO CENTER OF LEADS
 WHEN FORMED PARALLEL.

 3. DIMENSIONS "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.

P SUFFIX PLASTIC PACKAGE **CASE 646**

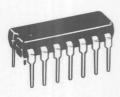






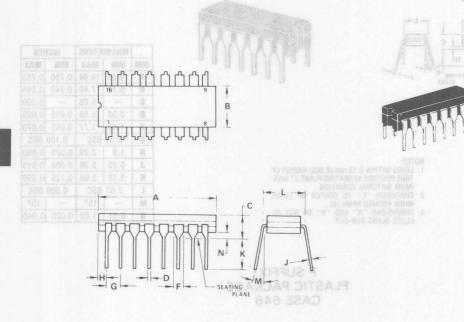
NOTES:

- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. 2. DIMENSION "L" TO CENTER OF LEADS
- WHEN FORMED PARALLEL.
- 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- 4. ROUNDED CORNERS OPTIONAL



	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	18.16	19.56	0.715	0.770
В	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
Н	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62	7.62 BSC		BSC
M	00	10°	0°	10°
N	0.51	1.02	0.020	0.040

L SUFFIX CERAMIC PACKAGE **CASE 620**









	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
В	6.10	7.49	0.240	0.295
C	_	5.08	_	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
Н	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62	BSC	0.300	BSC
M	JOHI TO	15°	AL MOTE	15°
N	0.51	1.02	0.020	0.040



- NOTES:

 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

- IMUM MATERIAL CONDITION.

 2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.

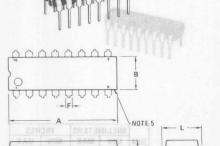
 3. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

 4. DIM. "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.

 5. DIM "E" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

16-PIN PACKAGES (continued)

P SUFFIX PLASTIC PACKAGE **CASE 648**



D SEATING

NOTE 5

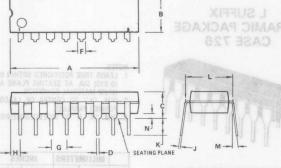
- G -

A 18 B 6	3.80 .10	MAX 21.34	MIN 0.740	MAX	POSITION AT SEATING PLANE AT MAXIMUM
A 18	3.80	21.34			PLANE AT MAXIMUM
B 6	.10		0.740		
		0.00	0.770	0.840	MATERIAL CONDITION.
C 4		6.60	0.240	0.260	2. DIMENSION "L" TO
	.06	5.08	0.160	0.200	CENTER OF LEADS
D 0	.38	0.53	0.015	0.021	WHEN FORMED
F 1	.02	1.78	0.040	0.070	PARALLEL.
G	2.54	BSC	0.100	BSC	3. DIMENSION "B" DOES NOT
H 0	.38	2.41	0.015	0.095	INCLUDE MOLD FLASH
J 0	.20	0.38	0.008	0.015	4. "F" DIMENSION IS FOR FUL
K 2	.92	3.43	0.115	0.135	LEADS. "HALF" LEADS ARE
L	7.62	BSC	0.300	BSC	OPTIONAL AT LEAD POSITI
M	00	100	00	100	MAJE 1, 8, 9, and 16). DITAJBR
NO	.51	1.02	0.020	0.040	5. ROUNDED CORNERS OPTIO

NOTES:

- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH. 2370M
- 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS MA 141, 8, 9, and 16). DITA
 - 5. ROUNDED CORNERS OPTIONAL.

P SUFFIX PLASTIC PACKAGE CASE 648B



	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	18.80	21.34	0.740	0.840
В	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
Н	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	00	100	00	100
N	0.51	1.02	0.020	0.040



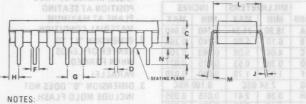
NOTES:

- 1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED
- PARALLEL. 3. DIMENSION "B" DOES NOT
- INCLUDE MOLD FLASH. 4. ROUNDED CORNERS OPTIONAL.
- 5. EXTERNAL LEAD CONNECTION, BETWEEN 15 AND 16 AS SHOWN.

■ 18-PIN PACKAGES I

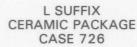
P SUFFIX PLASTIC PACKAGE **CASE 707**

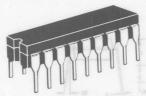


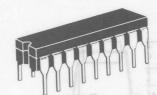


- 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
 - 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIN	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
В	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54	BSC	0.100 BSC	
Н	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62	BSC	0.300 BSC	
M	00	150	00	150
N	0.51	1.02	0.020	0.040







LATING PLANE PLANE PLANE DISTRICT AND A PLANE PL	V V V V V V V V V S I OM					
THATATA NO CONTRACTOR NO CONTR	RADIUS OF TRUE POSITION A SEATING PLANE OF MAXIMUM LATERIAL ECADHION 2. DIMENSION "L" TO CENTER OF					
	(3.11464)	Cae0.0	0.100	14.5	0.38	1

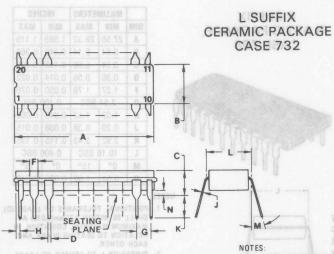
- NOTES:

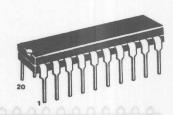
 1. LEADS TRUE POSITIONED WITHIN 0.25 mm
 (0.010) DIA. AT SEATING PLANE AT MAXIMMUM MATERIAL CONDITION.

 2. DIM. "L" TO CENTER OF LEADS WHEN
 FORMED PARALLEL.

 3. DIM. "A" & "B" INCLUDES MENISCUS.

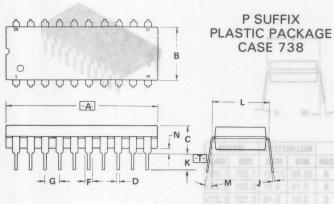
	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	22.35	23.11	0.880	0.910
В	6.10	7.49	0.240	0.295
C	-	5.08	-	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
Н	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	_	15°	-	15°
N	0.51	1.02	0.020	0.040

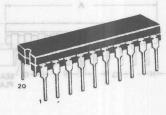




	MILLIN	METERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
A	23.88	25.15	0.940	0.990	
В	6.60	7.49	0.260	0.295	
C	3.81	5.08	0.150	0.200	
D	0.38	0.56	0.015	0.022	
F	1.40	1.65	0.055	0.065	
G	2.54	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050	
J	0.20	0.30	0.008	0.012	
K	3.18	4.06	0.125	0.160	
L		7.62 BSC		BSC	
M	00	150	00	150	
N	0.25	1.02	0.010	0.040	

- 1. LEADS WITHIN 0.25 mm (0.010)
 DIA, TRUE POSITION AT
 SEATING PLANE, AT MAXIMUM
 MATERIAL CONDITION.
- 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 3. DIM A AND B INCLUDES MENISCUS.





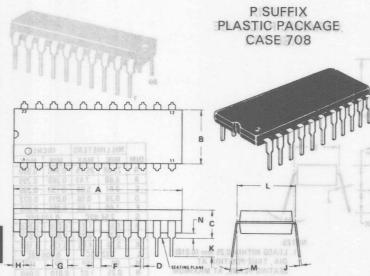
NOTES:

- 1. DIM A. IS DATUM.
- 2. POSITIONAL TOL FOR LEADS;

♦ Ø 0.25 (0.010)MT AM

- 3. T. IS SEATING PLANE.
- 4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
- 5. DIM L. TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

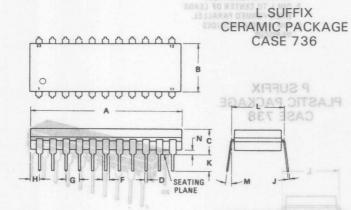
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	25.65	27.18	1.010	1.070
В	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100	BSC
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	00	150	00	150
N	0.51	1.02	0.020	0.040

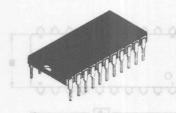


	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	27.56	28.32	1.085	1.115
В	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:

- 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 - 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

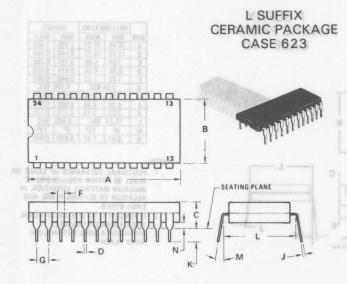




		MILLIMETERS	
	XAM	MIN	
	4 BSC		
			DI.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	26.80	27.81	1.055	1.095
В	9.14	9.91	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
Н	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	9.91	10.41	0.390	0.410
M	168000	15°	JAHA	15°
N	0.25	0.89	0.010	0.035

- 1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE AT MAX-IMUM MATERIAL CONDITION (DIM "D"). 2. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



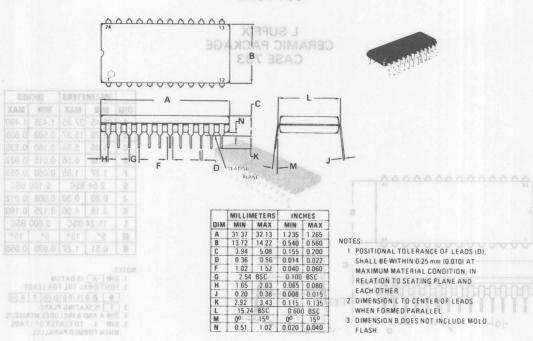
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
В	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	00	15°	00	15°
N	0.51	1.27	0.020	0.050

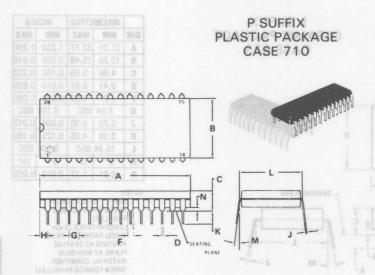
NOTES

- 1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONBITION. (WHEN FORMED PARALLEL)

3

P SUFFIX PLASTIC PACKAGE CASE 709



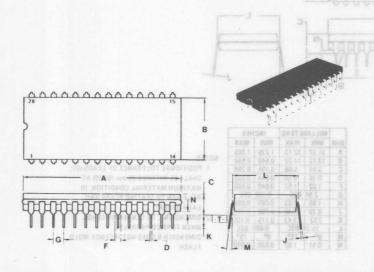


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
0	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
Н	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600	BSC
M	00	150	00	150
N	0.51	1.02	0 020	0.040

- 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- 2. DIMENSION L TO CENTER OF LEADS
- WHEN FORMED PARALLEL.

 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

L SUFFIX CERAMIC PACKAGE **CASE 733**



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.85	1.435	1.490
В	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

- 1. DIM A IS DATUM.
 2. POSITIONAL TOL FOR LEADS:

- Ø 0.25 (0.010)

 Ø 1 A

 Ø 0.25 (0.010)

 T I A

 Ø 0.25 (0.010)

 T I A

 Ø 0.25 (0.010)

 Ø 1 A

 Ø 0.25 (0.010)

 Ø 0.25 (0.010)

 Ø 1 A

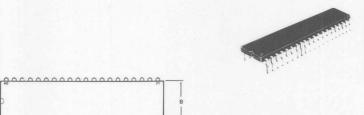
 Ø 0.25 (0.010)

 Ø 0.25 (0.

-G-

40-PIN PACKAGES

P SUFFIX PLASTIC PACKAGE CASE 711

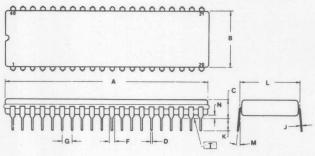


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
В	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
Н	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600	BSC
M	00	150	00	150
N	0.51	1.02	0.020	0.040

NOTES:

- 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
- 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.

L SUFFIX CERAMIC PACKAGE CASE 734



SEATING PLANE

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
В	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	50	150	50	150
N	0.51	1.27	0.020	0.050

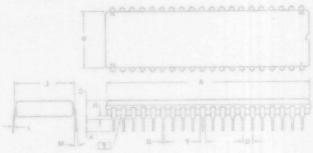
NOTES:

- 1. DIM -A- IS DATUM.
- 2. POSITIONAL TOLERANCE FOR LEADS:
- **♦** Ø 0.25(0.010) ⊗ T A ⊗

 3. T. IS SEATING PLANE.
- 4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 5. DIMENSIONS A AND B INCLUDE MENISCUS.







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			9
		2.54	
	4.06		35
	*328		
		0.51	



- 3. T IS SEATING PLANE.
 4. OIM L TO CENTER OF LEADS WHEN

Handling Procedures for CMOS Devices

Motorola CMOS devices have diode input protection against adverse electrical environments such as electrostatic discharge. In regards to this, the following statement is included on each data sheet:

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in} \text{ or } V_{out}) \leqslant V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Unfortunately, severe electrical transient voltages can be generated during handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially dangerous when discharged into a CMOS input, considering the energy stored in the capacity (≈ 300 pF) of the human body at these voltage levels.

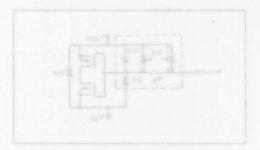
Present CMOS gate protection structures can generally protect against overvoltages. This is usually sufficient except in the severe cases.

The input protection circuit, while adding some delay time, provides protection by clamping positive and negative potentials to Vpp and Vss respectively. Figure 1 shows the internal circuitry for the diede-resistor protection.

The input protection circuit consists of a series isolation resistor RS, whose typical value is 1.5 k Ω , and diodes D1 and D2, which clamp the input voltages between the power supply pins Vpp and Vss. Diode D3 is a distributed structure resulting from the

Handling Precautions

PIGURE 1 - SCHEMATIC DIAGRAM, DIODE-RESISTOR IMPUT PROTECTION



In addition to the internal protection network, the following steps are recommended to further reduce damage to CMOS integrated circuits due to improper handling.

 All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

Handling Procedures for CMOS Devices

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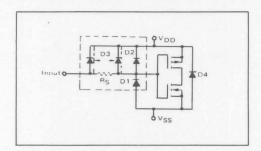
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FIGURE 1 — SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION

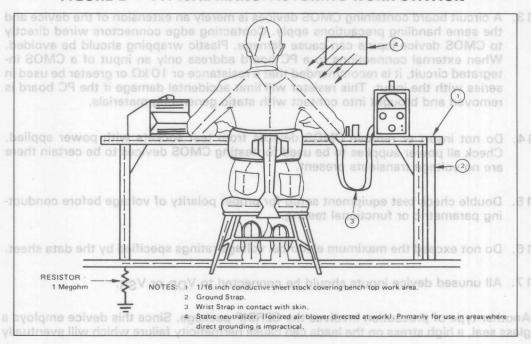


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 All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

- 2. The shipping rails are antistatically treated inside and outside. They provide adequate protection during storage and test/assembly handling operations, but should not be re-cycled as continuous use will cause deterioration of the antistatic coating.
- 3. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
- Nylon or other static generating materials should not come in contact with CMOS circuits.
- 5. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices or boards. Avoid this by grounding suspect areas and/or by the use of ionized air blowers, and/or air humidifiers.
- 6. Cold chambers using CO₂ for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
- 7. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
- 8. The following steps should be observed during wave solder operations.
 - The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.

FIGURE 2 - TYPICAL MANUFACTURING WORK STATION



- b. The loading and unloading work benches should have conductive tops which have grounded to an earth ground.
- oils c. Operators must comply with precautions previously explained.
 - d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
- 9. The following steps should be observed during board cleaning operation.
- a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
 - b. Brush or spray cleaning should not be used.
- c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
- d. Cleaned assemblies should be placed in antistatic container immediately after removal from the cleaning basket.
- e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
- 10. The use of static detection meters for line surveillance is highly recommended.
- 11. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
- 12. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.

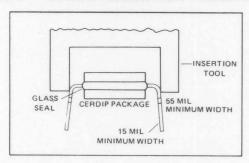
FIGURE 2 - TYPICAL MANUFACTURING WORK STATION

- 13. A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to CMOS device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address only an input of a CMOS integrated circuit, it is recommended that a resistance or 10 k Ω or greater be used in series with the input. This resistor will limit accidental damage if the PC board is removed and brought into contact with static generating materials.
- 14. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing CMOS devices to be certain there are no voltage transients present.
- 15. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
- 16. Do not exceed the maximum electrical voltage ratings specified by the data sheet.
- All unused device inputs should be connected to VDD or VSS.

Another type of precaution involves the CERDIP package. Since this device employs a glass seal, a high stress on the leads can cause hermeticity failure which will eventually

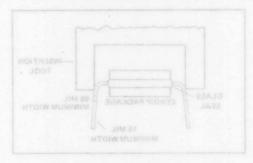
result in aluminum corrosion on the die. To avoid this, the leads should never be flexed above the seating plane. All insertion tools or automated equipment should contact the lead at its narrowest dimension allowing it to bend without affecting the wide portion above the seating plane.

FIGURE 3 - CERDIP INSERTION PRECAUTIONS



above the seating plane.

FIGURE 3 - CERDIP INSERTION PRECAUTIONS



Reliability and Quality Assurance

Motorola has an active Quality Improvement Program with the objective of improving failure rates and permitting tighter AQLs. At the time of writing — 83Q2 — the following data was applicable. For current data, please contact your Motorola Sales Office or franchised Motorola distributor.

OUTGOING QUALITY

Functional/Parametric Combined 0.10% AQL Level II

FAILURE RATES

TABLE 1 - FAILURE RATES FOR PLASTIC AND CERAMIC PACKAGES

	e Rate in %/1000 h imblent Temperatur		Package
85°C	70°C	50°C	
0.0109	0.0027	0.0003	Plastic Ceramic

The Motorola Philosophy

Our objective is to further improve our position as the quality leader in the supply of semiconductor products.

Our strategies are:

- 1. Actively promote a quality conscious attitude and quality environment in all pro-Reliability and
 - Quality Assurance
- Maintain and improve programmes for the continuous improvement of outgoing quality and reliability.
 - 4. Constantly measure and provide product reliability data.
 - 5. Support and develop the Motorola world-wide P.P.M. culture.
 - 6. Provide a fast responsive service for investigating customer related problems.
- Further improve good working relationships with customers' quality/engineering operations.

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OUTGOING QUALITY

Functional/Parametric Combined 0.10% AQL Level II Visual/Mechanical Combined 0.15% AQL Level II

FAILURE RATES

TABLE 1 — FAILURE RATES FOR PLASTIC AND CERAMIC PACKAGES

Package		re Rate in %/1000 h Ambient Temperatur	
	50°C	70°C	85°C
Plastic	0.0003	0.0027	0.0109
Ceramic	0.0001	0.0006	0.0025

The Motorola Philosophy

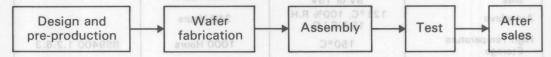
Our objective is to further improve our position as the quality leader in the supply of semiconductor products.

Our strategies are:

- Actively promote a quality conscious attitude and quality environment in all process, manufacturing and support operations.
- 2. Actively promote quality improvement plans.
- 3. Maintain and improve programmes for the continuous improvement of outgoing quality and reliability.
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- 7. Further improve good working relationships with customers' quality/engineering operations.

Reliability and Quality Assurance Activities 2338A7

In order to assure conformance to specifications, and to assure high levels of quality and reliability, there are R & QA activities in all parts of the production cycle.



Supporting all these activities is our product analysis group and providing supplementary support is our Hi-Rel operations group.

1. PRE-PRODUCTION

Reference

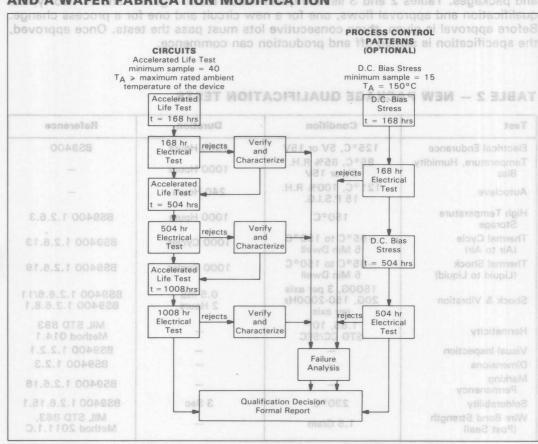
Quality Assurance starts before production commences. Within Motorola, all new production related activities and modifications thereto must be specified, qualified and approved prior to implementation. The form of control is defined by the change, and different controls are used for suppliers, raw materials, processes, equipments, designs and packages. Tables 2 and 3 list the qualification tests. Figure 1 shows two typical qualification and approval flows, one for a new circuit and one for a process change. Before approval is given, three consecutive lots must pass the tests. Once approved, the specification is signed off and production can commence.

TABLE 2 - NEW PACKAGE QUALIFICATION TESTS

		ZesT etil	
Test	Condition	Duration	Reference
Electrical Endurance	125°C, 5V or 15V	1000 Hours	BS9400
Temperature, Humidity Bias	85°C, 85% R.H. 5V or 15V	1000 Hours	-
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	240 Hours	
High Temperature Storage	150°C	1000 Hours	BS9400 1.2.6.3
Thermal Cycle (Air to Air)	-65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.13
Thermal Shock (Liquid to Liquid)	-65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.19
Shock & Vibration	1500G, 3 per axis 20G, 150-2000Hz per axis	0.5 mS 2 Hours	BS9400 1.2.6.6/11 BS9400 1.2.6.8.1
Hermeticity	1.85, 10 ⁻⁸ STD CC/SEC	Electrical Test	MIL STD 883 Method 014.1
Visual Inspection		_	BS9400 1.2.2.1
Dimensions	Failura	_	BS9400 1.2.3
Marking Permanency	-		BS9400 1.2.6.18
Solderability	230°C loed notted tilsuC	3 Sec	BS9400 1.2.6.15.1
Wire Bond Strength (Post Seal)	1.5 Gram		MIL STD 883, Method 2011.1.C

Test	Condition	Duration	Reference
Electrical Endurance	125°C, 5V or 15V	1000 Hours	BS9400
Temperature, Humidity Bias	85°C, 85% R.H. 5V or 15V	1000 Hours	
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High Temperature Storage	150°C	1000 Hours	BS9400 1.2.6.3
Thermal Cycle (Air to Air)	-65°C to 150°C	1000 Cycles	BS9400 1.2.6.13
Thermal Shock (Liquid to Liquid)	-65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.19
Shock & Vibration	1500G, 3 per axis 150-2000Hz, 20G, per axis	0.5 mS 2 Hours	BS9400 1.2.6.6/11 BS9400 1.2.6.8.1
Data Retention Bake (Non Volatile Memories)	200/250°C nidtiW .eonmmoon	1000 Hours	Quality Assurance at

FIGURE 1 — QUALIFICATION AND APPROVAL FLOW FOR A NEW CIRCUIT AND A WAFER FABRICATION MODIFICATION of 8 best selection and approval flow of selection and approval flow for a new circuit.



2. WAFER FABRICATION

The Wafer fabrication process is a complex one, involving small geometries, physics, chemistry and ultra high levels of purity and cleanliness. Figure 2 depicts the process flow and highlights the major process steps. The quality assurance activities are designed to give process control at each major process step, and to perform real time evaluation of the process at intermediate points within the process. The process control activities are:

- 1. Incoming inspection of raw materials.
- 2. Incoming inspection of masks.
- 3. Capacitance Voltage Drifts on Tubes/Product/Evaporator.
- 4. Oxide thickness/sheet resistance.
- Vapox Chemical Vapour Deposition (Doped/Undoped), thickness, % Phosphorous and Integrity.
- 6. Gate oxide breakdown (Furnaces/Lomac).
- 7. Source bubbler monitor.
- 8. Gas bottle pressures.
- 9. Implant evaluation.
- 10. Furnace temp. profiles.
- 11. 4 Pt. Probe calibration check.
- 12. Spin Drier.
- 13. De-ionized water/bacteria monitor.
- 14. Mask clean inspection.
- 15. Photoresist equipment check, Resist thickness monitor, Pinhole check.
- 16. Scanning Electron Microscope Surface profiles, Junction depth.
- 17. Final visual inspection.
- Shutter leakage, Metal thickness, Reflectivity, Sheet resistance and Monitors on evaporators.
- 19. Fab environmental monitor clean room and work stations.
- 20. Perkin Elmer aligner checks.
- 21. Junction depth monitor.
- 22. Oxidation induced stacking faults.
- 23. Quartzware check.
- 24. Monitor incoming acid quality.
- 25. Mylar burn and gas spectrum check on implanter.
- 26. Wafer analysis.
- 27. Electrical probe monitor.

These activities not only measure the characteristics of each lot, but also measure trends within the process from which extrapolations are made to give forewarning of potential problems. This feedback avoids reliability and quality problems and maintains optimum operation of the Wafer fabrication facility.

2. WAFER FABRICATION

solaying a FIGURE 2 - CMOS WAFER FABRICATION (SIMPLIFIED) and Ward flow and highlights the major p Inspect Oxidation Mask he process control activities are 1. Incoming inspection of raw materials. P-Implant P+ Deposition Oxidation & & Oxidation Drive-In N+ Deposition Mask Mask Oxidation & Drive-In Mask clean inspection. Photoresist equipment check, Resist thickness monitor, Pinhole check. Gate Implant Gate Oxidation and Anneal and Anneal Agnitors on Metal thickness, Reflectivity, Sheet resistance Aluminium Evaporation Mask Passivation Mask trends with forewarning of potential problems. This feedback avoids reliability and quality problems and maintains Responsible operation of the Wafer fabrication facility. Inspection Q.A. Backlap + Gold Evap. Mask Visual Insp. In-Process Inspection

3. ASSEMBLY AMBREA RINGALO GRYANDSTMI JACISYT - E BRUDIA

Assembly is highly automated — which benefits reliability and quality. In addition to the 100% screens, there are the following assembly quality activities:

- 1. Incoming inspection of raw materials.
- 2. Scribe audit.
- 3. Die high power visual inspection.
- 4. Die bond inspection.
- 5. Wire bond inspection.
- 6. Pre-cap inspection.
- 7. Hermeticity inspection.
- 8. Plating inspection.
- 9. Solderability.
- 10. Terminal strength.
- 11. Dimensions monitor.
- 12. Visual/mechanical inspection for flaws to body/leads.
- 13. Calibration monitor.
- 14. Moisture monitor.

An integral part of the assembly operation is to give every device a coded marking which defines the assembly location, the Wafer fabrication lot and the assembly lot. Thus it is possible to trace the history of every device.

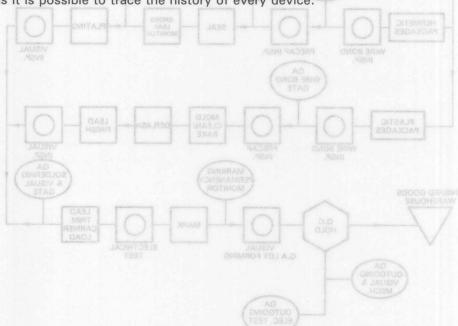
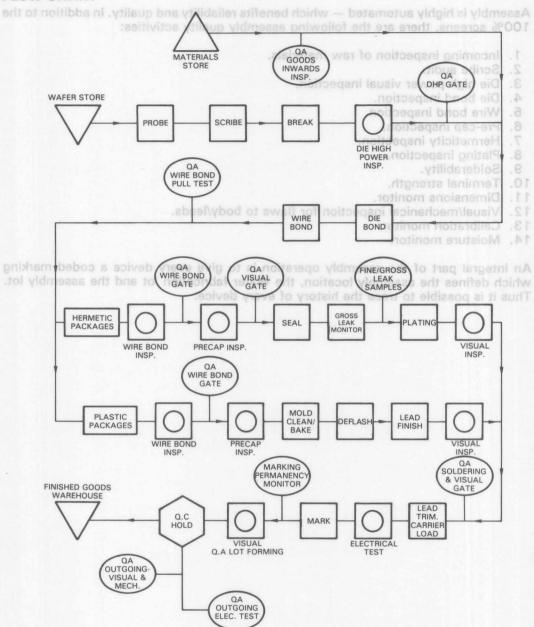


FIGURE 3 — TYPICAL INTEGRATED CIRCUITS ASSEMBLY & FINAL TEST FLOW CHART



CERAMIC vs PLASTIC

The most significant test is high temperature electrical endurance which is DTST d.

After 100% electrical test, there is a final inspection before the product is shipped to the warehouse. The inspection is

Functional/parametric combined 0.10% AQL Level II* Visual/mechanical combined 100 0.15% AQL Level II*

Electrical parameters include all parameters on the data sheet. Visual/mechanical includes marking legibility, plating, dimensions, etc. We even include the orientation of the devices within the tube! TABLE 4 - HIGH TEMPERATURE ELECTRICAL E

We believe these are the best AQLs for standard CMOS product in the Semiconductor Industry, and our objective is to maintain this position.

In	addition, Motorola h	nas a series o	of wee	ekly audits as	follows:	No. of Davices	No. of Batches
	Finished goods. Marking/marking p	ermanency.		Hours at 85°C	Hours at 125°C		
	Hermeticity.	0.0003		86.31M (9,850 years)	3.33M (380 years)		

- 5. Outgoing shipments.
- 6. Specifications/procedures of solutions of the failure rate at 85°C of 0.0109% / 1.000 hours for a salution of the failure rate at 85°C of 0.0109% / 1.000 hours for a salution of the failure rate at 85°C of 0.0109% / 1.000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 85°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the failure rate at 80°C of 0.0109% / 2000 hours for a salution of the 60°C of 0.0109% / 2000 hours for a salution of 0.0109% / 2000 hours for a saluti
- 7. Static protection: jis graphed in Figure 4 and compares favourably withnoisestation 7.047 years) is graphed in Figure 4 and compares favourably withnoisestation.
- 8. General housekeeping.
- 9. Calibration.

The combination of audits and lot inspection is designed to give maximum protection to our customers. Feedback from our customers shows that they find a reject rate of typically less than 200 PPM, i.e. 1 failure in every 5,000 parts supplied. At this low level, incoming inspection is not cost efficient and it is possible to reduce or eliminate incoming inspection.

Of equal importance to incoming quality is product reliability. Motorola has a comprehensive reliability program which assesses all aspects of product reliability. The program comprises the following periodic tests which are designed to provide mechanical. environmental and electrical stresses which will accelerate the life cycle into a short The failure rate at 85°C of 0.003% / 1,000 hours (or a mean time between

- 3,805 years) is graphed in Figure 4 and is impressingly low whenothered in Figure 4 and is impressingly low whenothered in Figure 4 and is impressingly low when the company of the company is graphed in Figure 4 and is impressingly low when the company is graphed in Figure 4.
- Dimensions.
- Marking permanency.
- Resistance to cleaning fluids. Studies of the prize of
- Solderability and plating.

 Acceleration

 Acceleration
- Acceleration.
- Wire bond.
- Hermeticity.
- Thermal shock.
- Temperature cycling.
- Mechanical shock and vibration. It is recommended that hermetic ceramic product be used in extrem
- Flammability.
- High temperature storage. Splyong like toubong pitself stnemnonivne viibimud to
- High temperature electrical endurance. The property of the second of t
- Temperature/humidity/bias.mad-non vilspianintal era sepiveb bepsalas pitasia IIA
- the lead frame/package seal interface or diffuse throughdimental package seal interface or diffuse through seal package seal interface or diffuse through seal package seal interface or diffuse through seal package seal packa
- * Correct as of 8302, and diddly supported blood about multimula edit to nois

The most significant test is high temperature electrical endurance which is performed at 125°C with the application of a 15V static bias in accordance with the truth table of the individual device. This test accelerates any inherent die related failure mechanisms.

Electrical tests to Motorola Data Sheet specifications are used to measure the performance of the devices. The number of failures at the 1,008 hour readout (including both parametric downgrades and catastrophics) are extrapolated to a lower temperature to provide a failure rate at 85 °C. The mathematical models employed to predict this are detailed in the appendix to this chapter.

TABLE 4 — HIGH TEMPERATURE ELECTRICAL ENDURANCE RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	No. of Device Hours at 125°C	Equivalent Device Hours at 85°C	No. of Failures		Failure Rate / 1,000 hou Temperature 70°C	rs
35	3,302	3.33M (380 years)	86.31M (9,850 years)	8	0.0003	0.0027	0.0109

The failure rate at 85 °C of 0.0109% / 1,000 hours (or a mean time between failures of 1,047 years) is graphed in Figure 4 and compares favourably with our 1981 standard of 0.030% / 1,000 hours.

TABLE 5 — HIGH TEMPERATURE ELECTRICAL ENDURANCE RESULTS FOR CERAMIC PACKAGES (1982)

No. of Batches	No. of Devices	No. of Device Hours at 150°C	Equivalent Device Hours at 85°C	No. of Failures	%	Failure Rate / 1,000 hou Temperature 70°C	rs Incom
Tresoro	2,394	2.41M (275 years)	350.15M (39,971 years)	ch reses	0.0001	0.0007 91	0.003

The failure rate at 85° C of 0.003% / 1,000 hours (or a mean time between failures of 3,805 years) is graphed in Figure 4 and is impressingly low when compared with our 1981 standard of 0.014% / 1,000 hours.

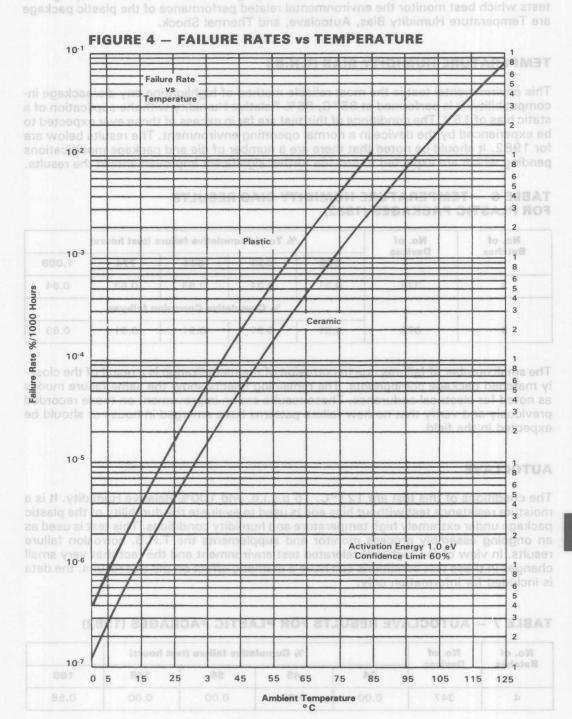
The steady reduction of plastic and ceramic failure rates reflects Motorola's commitment to reliability and quality improvement. The improvements are such that many customers who previously purchased burnt-in components now achieve the same or better reliability using Motorola CMOS without burn-in.

CERAMIC vs PLASTIC

It is recommended that hermetic ceramic product be used in extreme high temperature or humidity environments. Plastic product will provide similarly excellent reliability for lower cost in more normal operating conditions.

All plastic packaged devices are intrinsically non-hermetic as moisture can penetrate the lead frame/package seal interface or diffuse through the bulk of the plastic. If water reaches the surface of the chip and a bias is applied, an electrolytic cell is set up. Corrosion of the aluminium tracks/bond pads can occur which can downgrade the device





parameters and lead to catastrophic (open metal) failures. This phenomenon is accelerated by the presence of contaminants and Motorola is careful to minimize this effect by the use of quality grade materials/packaging and meticulous housekeeping. The tests which best monitor the environmental related performance of the plastic package are Temperature Humidity Bias, Autoclave, and Thermal Shock.

FIGURE 4 - FAILURE RATES VS TEMPERATURE

TEMPERATURE HUMIDITY BIAS (T.H.B.)

This environmental test is the most reliable method of highlighting any die/package incompatibility. It is performed at 85°C, 85% Relative Humidity with the application of a static bias of 15V. The conditions of this test are far in excess of those ever expected to be experienced by the device in a normal operating environment. The results below are for 1982. It should be noted that there are a number of die and package modifications pending which are expected to provide further significant improvements in the results.

TABLE 6 — TEMPERATURE HUMIDITY BIAS RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches		No. of Devices	1 1	% Total Cum	ulative failur	e (test hours)
batches	Devices	168	336	504	774	1,008	
a 3	378	0.31	0.31	0.63	0.63	0.94	
ε			% Cumul	ative Corrosi	on failures		
5 3	378	0.31	0.31	0.31	0.31	0.63	

The small number of failures due to corrosion of the metallization is a result of the closely matched package components. The remaining rejects show the same failure modes as noted for electrical endurance. These results are an improvement on those recorded previously and verify that no new failure patterns have emerged in house or should be expected in the field.

AUTOCLAVE

The conditions of this test are 121°C, 15 p.s.i.g. and 100% Relative Humidity. It is a moisture resistance test without bias and is used to evaluate the durability of the plastic package under extremely high temperature and humidity conditions. This test is used as an ongoing assembly process monitor and supplements the T.H.B. corrosion failure results. In view of the highly accelerated test environment and the fact that very small changes in these test conditions can have a dramatic effect on the end results, the data is included for information only.

TABLE 7 - AUTOCLAVE RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	% Cumulative failure (test hours)				100
125	105 115	24	48	96	148	168
4	347	0.00	0.00 A	0.00	0.00	0.58

The Autoclave results augment those recorded for T.H.B. performance and demonstrate the moisture resistant nature of the Motorola plastic encapsulated devices under extreme conditions.

THERMAL SHOCK

Thermal shock provides a quick and severe method of stress and is a liquid to liquid cycle between -65° C to $+150^{\circ}$ C with a dwell of five minutes at each temperature.

TABLE 8 — THERMAL SHOCK RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	% Cumulative failure (test cycles)		
Datolies	Devices	200	1,000	
2	250	c package 00.0	0.00	

The results verify the plastic mould compound, bond wires and lead frames have closely matched coefficients of expansion. This benefit reduces the potential of moisture ingress (e.g. during the T.H.B. test) within the package ensuring a stable encapsulant for the die.

There is one further important source of quality and reliability data—feedback from our customers!

5. AFTER SALES

CUSTOMER FEEDBACK ENSURES QUALITY IMPROVEMENT

Customer feedback is obtained from incoming inspection and qualification results and from returned defective product.

- a) With certain customers who use large quantities of CMOS, Motorola has reached agreement on joint quality improvement programs. These programs are basically an exchange of information. Our customers provide feedback by device type on the quality and reliability of our product. Analysis of this feedback highlights problems not previously apparent, and corrective action is implemented. Both Motorola and all our customers have benefitted from these programs. The incoming quality level as reported by these customers is typically less than 200 PPM.
- b) Due to the high quality of our product, it is possible to analyse every return of defective product. Approximately 40% of these are in fact non-defective and are the result of correlation problems. Some of the returns have been mishandled (see Chapter 4), the remainder are analysed to determine where action can be taken to improve the outgoing quality.

6. PRODUCT ANALYSIS

Product analysis is used at all stages of manufacturing—from pre-production to after sales—to determine failure mechanisms and how to avoid them. Various techniques are

used and our failure analysis laboratory is well equipped with a variety of equipment including scanning electron microscopes, X-ray analysers and micromanipulative probers. Figure 5 shows the flow used for finished product.

7. HI-RELtiensh vtilidadora laitnenogxe na awollof noitudirtaib star erulisf ent tant

Motorola's Hi-Rel programs—for avionic, space and military applications—has indirectly provided a considerable contribution to our commercial products. The Hi-Rel programs set the standards for the control of quality and the assessment of reliability, and at Motorola we use these standards for our commercial product as well as our Hi-Rel product. At the time of writing, Motorola has the following approvals for CMOS product:

DEF STAN 05/31 — MOD Registration 1G9M01
DEF STAN 05/21 — MOD Registration 1G9M01
BSI App. No. 1085 M

CECC App. No. M0070/CECC/UK 1085 M

CONCLUSION

With design and manufacturing facilities in the U.S.A., Japan and Europe, Motorola's experience in CMOS is unsurpassed. In Europe alone, Motorola has shipped over 500,000,000 CMOS devices. The levels of quality and reliability which we have achieved are extremely high. Through our quality improvement program, we will achieve even higher levels for the benefit of you, our customer.

used and our failure analysis laboratory is well equipped with a variety XIDNAPPA

FAILURE RATE CALCULATIONS: risinit not beau walt and shows 5 and Figure 5

Two mathematical models are employed to predict the failure rate. Firstly it is assumed that the failure rate distribution follows an exponential probability density function.

Motorola's Hi-Rel programs – for
$$(t, -1, -1)$$
 is $\lambda = \lambda \in F(X)$ litery applications – has indirect-

where F(X) = probability density function $\lambda_{0.28}$ = failure rate

product. At the time of writing, Motorola has the following aremit alse for CNIOS pro-

Since reliability evaluations usually involve random samples of a population, a point estimation for the failure rate is calculated using the Chi-squared distribution.

$$\lambda = \frac{\chi^2 (\alpha, 2r + 2)}{2nt}, \quad \alpha = \frac{(100 - CL)}{100}$$

where χ^2 = tabulated value

CL = confidence limit in percent bearings and a company of rejects and a company of confidence limit in percent bearings and a company of confidence limit in percent bearings and a company of confidence limit in percent bearings and confidenc

wn me = number of devices loup number of dev

t = duration of the test

A confidence limit of 60% is employed in the formula.

The second model uses the Arrhenius Equation to relate the failure rate at test temperature to that expected at normal operating conditions.

$$R(T) = Ro EXP (E_a / kT)$$

where R(T) = reaction rate at normal temperatures

Ro = a constant

 $E_a = activation energy (1eV)$

Boltzmann's constant

T junction temperature

The use of junction temperatures rather than ambient (lifetest) temperature provides a more accurate failure rate. The junction temperature is computed using the equation below:

$$T(J) = T(A) + (P \times \theta_{JA})$$

5-16

where T(J) = junction temperature (°C)

T(A) = ambient temperature (°C)

P = power (Watts)

 θ_{JA} = average junction to ambient thermal resistance (°C/W)

Data Books, Brochures and Selection Guides

Additional information on CMOS products can be found in the following publications available at your nearest Motorola Sales Office or Distributor.

DATA BOOKS

8001 A/D and D/A Conversion Manual

8002A CMOS Data Manual, Volume 1, Standard Logic

3002C CMOS Data Manual, Volume 3, High Speed CMOS

B003A Home Electronics / Integrated Circuits

8011 Memory Data Manual

8025 The Furopean Master Selection

8039 Telecommunications Data Manual

BROCHURES AND SELECTION GUIDES

F045 Telecommunications, A System Approach

FOSS High Speed CMOS Function Selector Guide

-060 - Catalog of Technical Literature

F062 CMOS Standard Logic Reliability Report

FO72 Macrocell Arrays and CAE

OZE CMOS Eurotion Salactor Guide

FO77 High Speed CMOS Life Test

APPLICATION NOTES

A complete list of Application Notes can be found in the Catalog of Technical Literature (Reference F060).

AN-471 Analog-to-Digital Conversion Techniques

The subject of A/D conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms, from a system point of view, and is intended to assist the reader in determining which conversion technique is best suited for a given application.

Publications and Applications

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DATA BOOKS

B001 A/D and D/A Conversion Manual
B002A CMOS Data Manual, Volume 1, Standard Logic
B002C CMOS Data Manual, Volume 3, High Speed CMOS
B003A Home Electronics / Integrated Circuits
B011 Memory Data Manual
B025 The European Master Selection
B039 Telecommunications Data Manual

BROCHURES AND SELECTION GUIDES

F045 Telecommunications, A System Approach
F055 High Speed CMOS Function Selector Guide
F060 Catalog of Technical Literature
F062 CMOS Standard Logic Reliability Report
F072 Macrocell Arrays and CAD
F075 CMOS Function Selector Guide
F077 High Speed CMOS Life Test

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AN-535 Phase-Locked Loop Design Fundamentals.

The fundamental design concepts for phase-locked loops implemented with integrated circuits are outlined. The necessary equations are given in conjuction with a brief design example.

AN-716 Successive Approximation A/D Conversion. Successive Approximation A/D Conversion.

This Application Note concerns the successive approximation type of A/D Converter. The questions of why, how and where to use the successive approximation technique are discussed along with the basic theory of operation.

AN-741 Interface Considerations for Numeric Display Systems.

This note describes several methods of multiplexing multi-digit, sevensegment. LCD, LED, GAS discharge, incandescent and fluorescent displays. Interfaces and interface considerations are described in detail.

AN-759 A CMOS Keyboard Data Entry System for BUS Oriented Memory Systems.

This Application Note describes a keypad to binary data entry system for use with CMOS or NMOS memories, either in minicomputer/microprocessor application or as a part of any logic system containing random access memory. Manual data entry using a keyboard avoids the use of a binary format, offering increased speed and accuracy of manual direct memory accessing.

AN-769 Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter.

This Application Note describes an autoranging DMM using the MC14433. The multimeter includes AC and DC voltage ranges from 200mV to 200V, AC and DC current from 2mA to 2A full scale, and resistance ranges from $2k\Omega$ to $2M\Omega$ full scale.

AN-770 Data Acquisition Networks with NMOS and CMOS.

This article describes an eight-channel data acquisition network using the MC14433 A/D Converter and the MC6800 Microprocessor family. The A/D conversion technique is a modified dual ramp featuring auto-zero, auto-polarity, and high input impedance. Both hardware and MC6800 software are shown.

AN-806 Operation of the MC14469

The MC14469 is an addressable asynchronous receiver/transmitter that finds applications in control of remote devices, transfer of data to and from remote locations on a shared wire and as an interface from remote sensors to a central processor.

AN-874 Macrocell Arrays: Concept-Features-CAD Interface.

High technology array based products offer the advantages of custom circuits, yet overcome the problems of high costs and long design cycles. Recent developments in array technology make use of Macrocell building blocks rather than primitive gates for easier design and higher performance. Additional developments in computer-aided-design customer interface systems simplify the job of developing array circuit options. This note examines Motorola's Macrocell array concept with special emphasis on the CAD user interface.

AN-889 An Easy-to-Use Development System for the Engineer Utilising a Microprocessor in a System Design.

This application note describes such a system for the MC14500B industrial control unit. The system features keyboard Data/Address entry, 256 program steps, 7-segment readout and all CMOS construction, with flexibility for expansion and modification.

AN-741 Interface Considerations for Numeric Display Systems.

HANDBOOKS

HB-209 MC14500B Industrial Control Unit Handbook

Design and application manual for the MC14500B. Contains chapters on software, hardware and systems.

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